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Implementation of OFDM transmitter and receiver on FPGA with Verilog using Mixed Radix8-2 Algorithms

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Abstract:

OFDM is a multi-carrier modulation technique with densely spaced sub-carriers that has gained a lot of popularity among the broadband community in the last few years. Orthogonal frequency division multiplexing (OFDM) is an established technique for wireless communication applications. We study the performance of OFDM, including the power spectral density, BER, through intensive Xilinx design and implementation of OFDM simulation. In this paper, system will be illustrated along with detailed simulation of the OFDM system to study the effect of various design parameters. OFDM transceiver will be implemented using FPGA Spartan 6 kit. All modules are designed with Verilog programming language. Verilog be used for RTL description and FPGA synthesis tools will be used for performance analysis of the proposed core. ISIM Xilinx Edition will be used for functional simulation and verification. Xilinx ISE will be used for synthesis. The Xilinx's Chip scope tool will of results be used for verifying the results on Spartan 6 FPGA. The most effective and efficient algorithm used here provides enhancement in system performance.

Index Terms: *Orthogonal Frequency Division Multiplexing (OFDM); Field Programmable Gate Array (FPGA); Inverse Fast Fourier Transform (IFFT); Fast Fourier Transform (FFT).*

1. INTRODUCTION

Due to rapid growth of wireless and multimedia communication, there is a tremendous need for high-speed data transmission. Telecommunication industry provides variety of services ranging from voice to multimedia data transmissions, in which speed ranges several Kbps to Mbps. Existing system, may fail to support high speed efficient data transmission. To improve the speed and maximum amount of data transmission Orthogonal Frequency Division Multiplexing (OFDM) system may be used [1]. Orthogonal Frequency Division Multiplexing (OFDM) was first developed in the 1950's [2]. OFDM is a method of encoding digital data on to a numerous carrier frequencies. It has developed into a very popular scheme for wideband digital communication systems. Many researchers shown OFDM can be used in applications such as audio broadcasting [3], digital television [4], power line networks [5], wireless networks and 4G mobile communications [6]. In OFDM
A large number of thoroughly spaced sub carriers are used to convey data on to several parallel data streams. Each sub carrier is modulated with modulation techniques such as Quadrature Amplitude Modulation (QAM), Quadrature Phase Shift Keying (QPSK) or Binary Phase Shift Keying (BPSK) at a lesser symbol rate. In this paper implementation of OFDM transmitter and receiver on Spartan 6 FPGA board has been carried out using radix 8-2 algorithm for the first time . This work involves designing of 48-point IFFT and 48-point FFT blocks using mixed radix 8-2 algorithm. Using these IFFT and FFT blocks, OFDM transmitter and receiver blocks are constructed. Rest of the paper is organized as follows. In section 2 related works is discussed. In section 3 overview of OFDM is discussed. OFDM transmitter and OFDM receiver details are given in section 4 and 5 respectively. Implementation and simulation results are discussed in section 6. Conclusion.

2. RELATED WORK

Many researchers were contributed their work towards FPGA implementation of Orthogonal Frequency Division Multiplexing (OFDM) transceiver. In [1] designing of OFDM system was performed using VHDL. They used radix-2 8-Point Decimation In Frequency (DIF) IFFT/FFT blocks. In [2] various design parameters of OFDM system was performed using Matlab. They implemented OFDM transceiver on Spartan 3A kit using VHDL programming language. In [8] designing of OFDM Transmitter and Receiver was performed using Quartus II tool. Altera Modalism was used for simulation and every component of OFDM Transceiver was designed using Verilog. In [12] designing of OFDM system was performed using Verilog with radix-2 8-Point Decimation In Frequency (DIF) FFT and IFFT. In [13] designing of OFDM system was performed using VHDL and Xilinx's Chip scope tool was used for validating results on Spartan 3E kit. In [14] OFDM system was implemented on Virtex-2using Xilinx ISE 10.1.In [15]designing of OFDM system was performed using VHDL and Xilinx's Chip scope tool is used for verifying the results on Spartan 3E kit. In [17] designing of OFDM system was implemented using Xilinx on Spartan-3 FPGA. In this work FFT/IFFT module was implemented using CORDIC algorithms as an alternate for multipliers. In [18] 16 bit Quadrature Amplitude Modulation (QAM)was simulated using Simulink and VHDL code was generated using system generator tool. This work focused on designing core processing blocks of OFDM transmitter and receiver. Design has been coded in VERILOG. Timing simulation is analyzed using Xilinx ISE 12.2 And ModelSim

6.3f. Design of OFDM transceiver is synthesized and it is implemented on Vertex 4 FPGA.

3. OVERVIEW OF OFDM using radix 8-2

Orthogonal Frequency Division Multiplexing (OFDM) is a modulation scheme having multicarrier transmission technique [7]. In OFDM, spectrum is divided into abundant carriers each one being modulated at lower data rates. Fig.1 shows spectrum of Frequency Division Multiplexing (FDM). In FDM subcarriers are non-overlapping, hence requires more bandwidth. Fig.2 shows spectrum of OFDM overlapping subcarriers. Saving of bandwidth in OFDM is shown in Fig.2. OFDM is analogous to FDM but much more spectrally effective by positioning the sub-channels much closer together. This is done by selecting the frequencies that are orthogonal and by letting the spectrum of each sub channel to overlay another without interfering with it. Fig.3 shows spectrum overlap in OFDM. It is observed from Fig.3 that, at any instance only main lobe of one signal is high and all lobes of other signals are zero. Hence necessary band width is significantly reduced by removing guard bands and this allows signals to overlap [7].

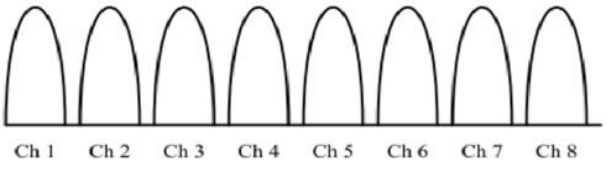

Fig.1 Required Bandwidth

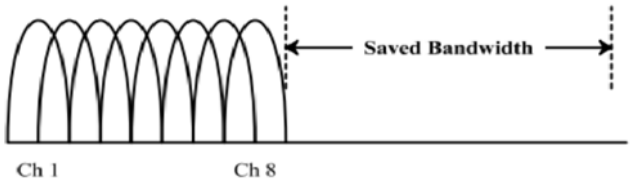

Fig.2 bandwidth saving

4. Implementation

4.1 OFDM TRANSMITTER

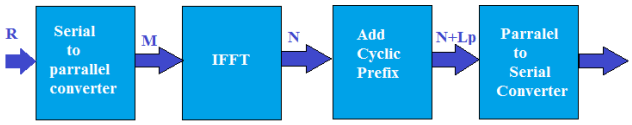

Fig.3 OFDM Transmitter

Fig. 3 shows the block diagram of OFDM transmitter. OFDM transmitter generates a modulated data. It consists of blocks such as, 16 bit QAM, symbol generator, zero padding, IFFT, cyclic prefix and output module blocks. Input to the QAM is 4 bit binary data. The output of QAM consists of 16 bit In-phase and quadrature components. Output of QAM is given to the symbol generator. Symbol generator gives a 64 bit output by concatenating each component of QAM output by four times. The output of symbol generator is given to zero padding blocks. At zero padding block 32 bits of

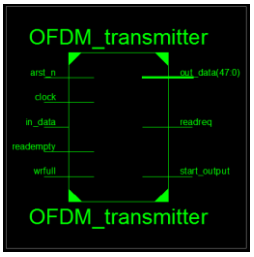

Fig.4 Top module of Transmitter

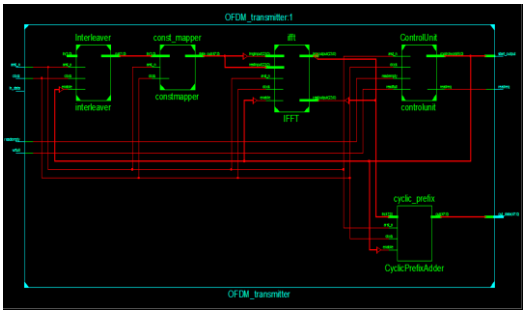

Fig.5 RTL view of Transmitter

Zeros are added at the beginning and at the end of the symbol generator output, which gives 128 bit output. Inverse Fast Fourier Transform [IIFT] converts a spectrum consisting of both amplitude and phase of each component in frequency domain to a time domain signal. 8-point 16 bit radix 8-2 IFFT is used. In this work two IFFT modules, one for the real component and the other for the imaginary component is used. The output of IFFT is given to cyclic prefix block. The word cyclic prefix refers to the preceding of symbol with a replication of the end. It serves as a guard interval, which eliminates inter-symbol interference from previous symbol. Cyclic prefix is frequently used in coincidence with modulation in order to recollect sinusoid properties in multipath channels. The output of cyclic prefix block is given to output module block. The purpose of output module block is to have a 16 bit data as the OFDM transmitter output. Individual blocks of OFDM transmitter are discussed below.

4.2 OFDM Receivers

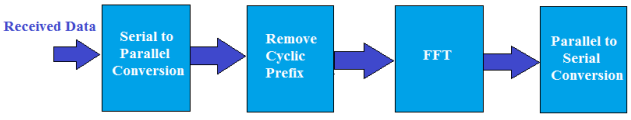

Fig.6 OFDM Receiver

The main blocks of OFDM receiver are observed inFig.4.1thereceived signal goes through the cyclic prefix removal and a serial-to-parallel converter [2]. After that, the signals are passed through an N-point fast Fourier transform to convert the signal to frequency domain. The output of the FFT is formed from the first M samples of the output. The demodulation can be made by DFT, or better, by FFT, that is it efficient implementation that can be used reducing the

time of processing and the used hardware. FFT calculates DFT with a great reduction in the amount of Operations, leaving several existent redundancies in the direct calculation of DFT [4].

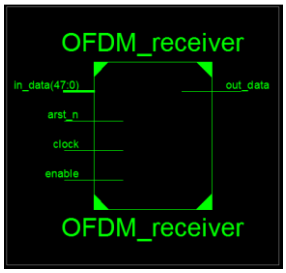

Fig.7 Top module of Receiver

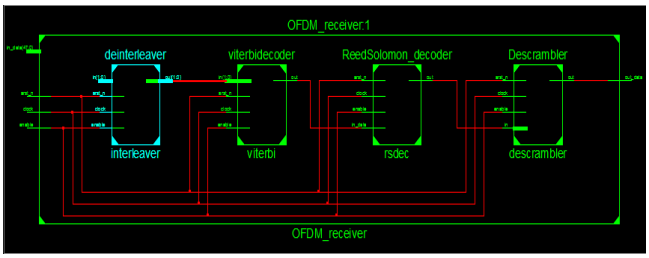

Fig.8 RTL view of Receiver

5. Simulation and results

By using the Redix8-2 algorithm in OFDM transmitter and receiver we minimize the transmitter and receiver processing time up to 4.114ns and power consumption also reduced up to 81mW.

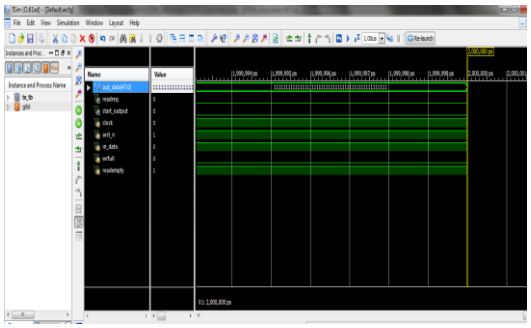

Fig.9 simulation result of OFDM Transmitter

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	78	11440	0%
Number of Slice LUTs	113	5720	1%
Number of fully used LUT-FF pairs	77	114	67%
Number of bonded IOBs	54	102	52%
Number of BUFG/BUFGCTRLs	1	16	6%

Fig.10 OFDM Transmitter logic utilizations

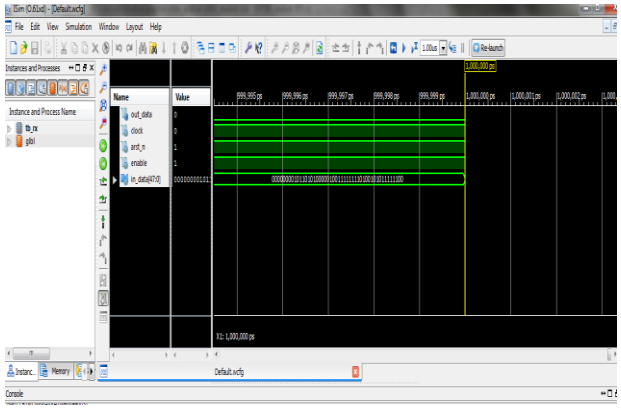

Fig.11 Simulation result of OFDM Receiver

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	30	11440	0%
Number of Slice LUTs	34	5720	0%
Number of fully used LUT-FF pairs	29	35	82%
Number of bonded IOBs	4	102	3%
Number of BUFG/BUFGCTRLs	1	16	6%

Fig.12 OFDM Receiver logic utilizations

6. CONCLUSION

In this paper, we designed an OFDM transmitter and receiver with different FFT algorithms and they are implemented using VLSI design process. It was found that many blocks need complex multipliers and adders and therefore special attention needs to be given to optimize these circuits and maximize reusability. In particular, the models have been applied to analyze the performance of mixed-radix FFT architectures used in OFDM. Actual hardware resource requirements were presented and simulation results were given for the synthesized design. The 48-point Mixed-Radix 8-2 FFT based OFDM architecture was found to have a good balance between its performance and its hardware requirements and is therefore suitable for use in OFDM system

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