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A comprehensive study on Applications of Vedic Multipliers in signal processing

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Abstract: Digital Signal Processing (DSP) operations are very important part of engineering as well as medical discipline. Designing of DSP operations have many approaches. For the designing of DSP operations, multiplication plays an important role to perform signal processing operations such as convolution and correlation. The new approach of this implementation is easy to calculate DSP operations for small length of sequences. In this paper a fast method for DSP operations based on ancient Vedic mathematics is contemplated. The implementation of high speed DSP UrdhavaTriyagbhayam Sutra operations of two finite length sequences using Vedic Urdhava-Triyagbhayam Multiplication Sutra (approach/method) is done. It is very efficient multiplication formula applicable for all types of multiplication. This algorithm is implemented in MATLAB and all the operation is performed in single Graphical User Interface (GUI) window. Vedic mathematics based DSP operations reduce the processing time as compared to inbuilt function of MATLAB. It reduces the 40-60% time from inbuilt function and this algorithm operates in concept of Vedic multiplier on is the heart of the mobile communication and satellite communication system.

Keywords: Vedic sutras, Vedic Multipliers

1. Introduction

Convolution plays a preciously role in digital signal Processing and image Processing. It is used for designing of digital filter and correlation application. The linear convolution effectively can be designed by using simple Vedic multipliers. Convolution is basic concept to design the finite impulse response filter, discrete Fourier Transform (DFT) and fast Fourier Transform (FFT) [1]. Linear convolution of two finite length sequence normally computed by using the application of Discrete Fourier Transform [2,3] .Design of all DSP operations with the help of high speed Vedic multipliers which increase the efficiency of system and reduces the processing time. This DSP implementation can be designed in Matlab with GUI, which is user friendly and easy to use.

2. VEDIC MATHEMATICS

Vedic mathematics is an ancient fast calculation mathematics technique which provides the unique technique of mental calculation with the help of simple rules and principles. Veda rediscovered by the holiness Jagad Guru Shree Bharti Krishna Tirtha JiMaharaj (1884-1960) in between 1911-1918. According to Swami-Ji all Vedic mathematics is based on 16-Sutra (Algorithm) and 16- up-sutra (Sub-algorithm) after broadly research in Atharva Veda [4]. It computes all the basic as well as complex mathematical operation easily and quickly also provides a powerful technique. It is more consistent than modern mathematics and provides an expeditious solution.. It is based on sixteen sutras which transact different branches of mathematics i.e.

algebra, geometry, arithmetics . Modern mathematics is an integral part of the technical education in most of the engineering system designand is based on the various mathematical approaches. The necessity for expeditious processing speed used following Vedic mathematics algorithm.

2.1 VEDIC SUTRAS

The Vedic multiplier is based on the Vedic multiplication formulae (Sutras). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. The same ideas can be used to the binary number system too.

2.2 URDHVA TIRYAKBHYAM SUTRA

UrdhvaTiryakbhyam (Vertically and Crosswise), deals with the multiplication of numbers. This Sutra has been traditionally used for the multiplication of two numbers in the decimal number system. In this paper, we apply the same idea to the binary number system to make it compatible with the digital hardware. Let us first illustrate this Sutra with the help of an example in which two decimal numbers are multiplied.

Example:
234
*316

61724
1222---carry

73944
Steps:
1) 4 X 6 = 24: 2, the carried over digit is placed below the
second digit.
2) (3 X 6) + (4 x 1) = 18 + 4 = 22; 2, the carried over digit is
placed below third digit.
3) (2 X 6) + (3 X 1) + (4 X 3) = 12 + 3 + 12 = 27; 2, the carried over digit is placed below fourth digit.
4) (2 X 1) + (3 X 3) = 2 + 9 = 11; 1, the carried over digit is
placed below fifth digit.
5) (2X3) =6
6) Respective digits are added

Line diagram for the multiplication of two numbers (234× 316) is shown in Fig. 1. The digits on the two ends of the line are multiplied and the result is added with the previous carry. When there are more lines in one step, all the results are added to the previous carry. The least significant digit of the number thus obtained acts as one of the result

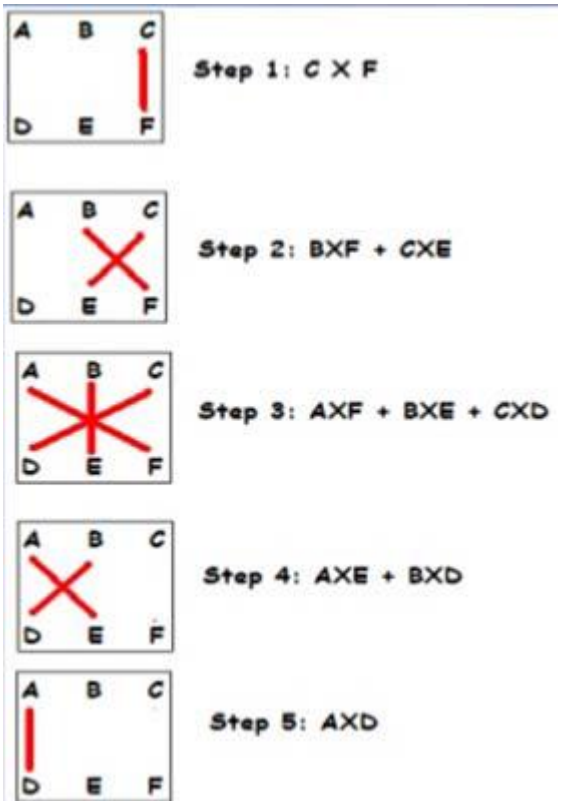


Figure 2.1

3. Usage of Vedic multiplier in convolution

Vedic multipliers can also be used in the most fundamental operation known as convolution.

3.1. Convolution

It is a mathematical way of combining two signals to form a third signal [5]. For two finite discrete sequences of length Nx and Nh, the linear or a periodic convolution sum takes on a slightly different form.

3.2 Implementation of sutra in convolution

i)The power and area for this design can be evaluated after designing original convolution algorithm using conventional multiplier and adder units.

ii)The original design can be redesigned to reduce the number of multiplier needed using cyclic data flow and the power, and area for this design can be evaluated

iv) The original design can be redesigned to reduce the number of adder needed using cyclic dataflow and power and area for this design can be evaluated..

v)By redesigning the original design with pipeline structure by incorporating latches in critical path, power and area for this design can be evaluated..[6,7]

3.3. Usage of Vedic multiplier in convolution operation

Type I

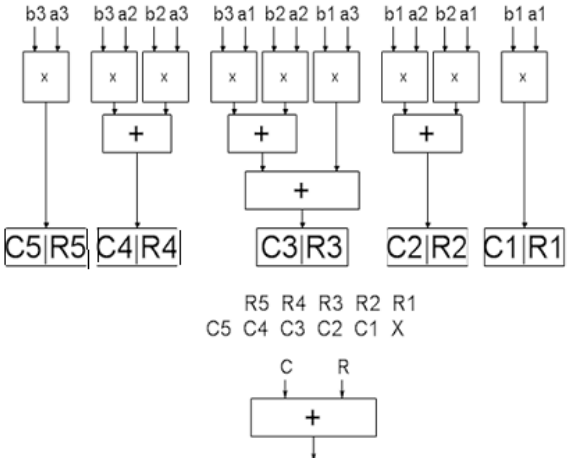
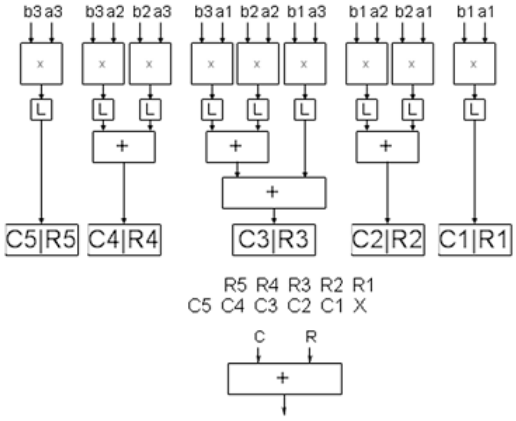


Figure:3.1

In this architecture 9 multipliers each of 4 bits, 4 adders of 8bits and 9 bits are used respectively

Type II



In this architecture pipeline approach has been implemented and latches have been used. Latches are used to stabilize the initial state Type III

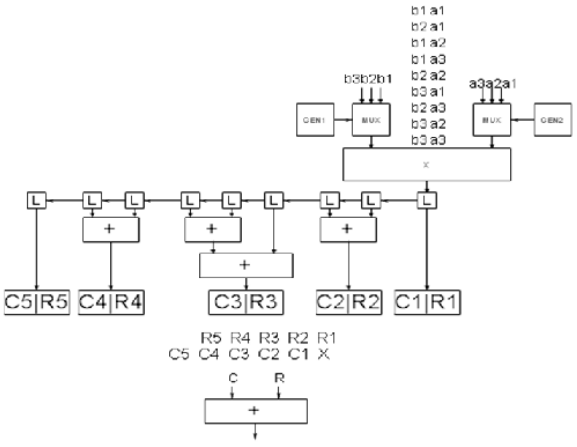


Figure :3.2

In this architecture 1 multiplier is used as compared to 9multipliers in type I and II respectively.

A multiplier is a very important element in any processor design and a processor spends considerable amount of time in performing multiplication and generally the most area consuming. Hence, optimizing the speed and area of the multiplier is a major design issue. An

improvement in multiplication speed by using new techniques can greatly improve system performance.

4 .Fast Fourier Transform(FFT)

Digital signal processing is an area of science and engineering that has developed rapidly over the past 30 years. The digital computers and associated digital hardware of three decades ago were relatively large and expensive and, as a consequence, their use was limited to general-purpose non-real-time (off-line) scientific computations and business applications. These inexpensive and relatively fast digital circuits have made it possible to construct highly sophisticated digital systems capable of performing complex digital signal processing functions and tasks, which are usually too difficult and/or too expensive to be performed by analog circuitry or analog signal processing systems. Hence many of the signal processing tasks that were conventionally performed by analog means are realized today by less expensive and often more reliable digital hardware. 4x4 Urdhva Tiryakbhayam multiplier can be used in computation of
FFT.

4.1 Usage of vedic multiplier in FFT

The Reversible 4X4 Urdhva Tiryakbhayam Multiplier design emanates from the 2X2 multiplier. The block diagram of the 4X4 Vedic Multiplier is presented in the figure 4. It consists of four 2X2 Multipliers each of which procures four bits as inputs; two bits from the multiplicand and two bits from the multiplier. The lower two bits of the output of the first 2X2 multiplier are entrapped as the lowest two bits of the final result of multiplication. Two zeros are concatenated with the upper two bits and given as input to the ripple carry adder and obtained from the second 2X2 multiplier. Likewise the outputs of the third and the terminal 2X2 multipliers are given as inputs to the second four bit ripple carry adder. The outputs of these four bit ripple carry adders are in 5 bit each which need to be summed up. [8]

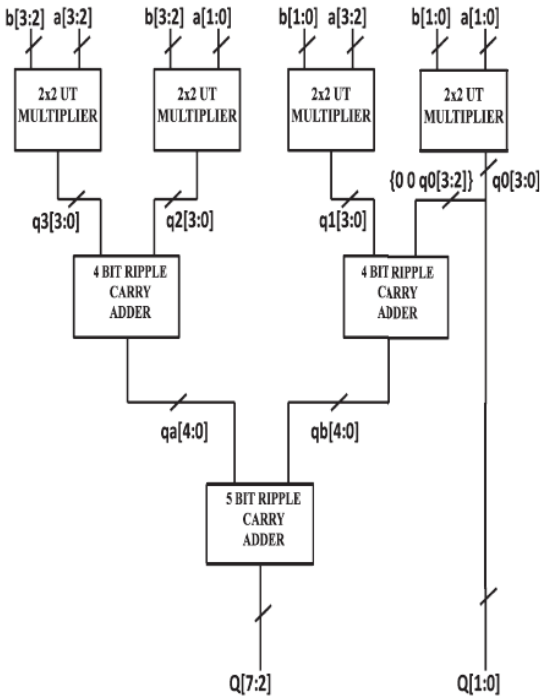


Figure 4.1

5. MAC unit

Today in digital technology the ever increasing demand in enhancing the ability of processors to handle the complex and challenging processes has resulted in the integration of a number of processor cores into one chip. Still the load on the processor is not less in generic system. This load is reduced by supplementing the main processor with Co-Processors, which are designed to work upon specific type of functions like numeric computation, Signal Processing, Graphics etc. in which MAC Unit is most dominant Co-Processor and work as heart of digital signal processors. Faster Operations are of extreme importance in MAC Unit. The speed of MAC Unit depends greatly on the multiplier; after deep study and analysis it was found that the efficiency of Urdhva Triyakbhyam-Vedic method for multiplication is much better in the comparison to other conventional multipliers, which strikes a difference in the actual process of multiplication

itself. It enables parallel generation of in termed Urdhvaiate products

5.1 Design of MAC unit using vedic multipliers

A combination of Urdhva Triyakbhyam sutra with unique addition tree structure similar to Wallace for multiplication can be used. Conventional Vedic multiplier for design of 2x2 bit multiplier and for higher level multiplier [9] can replace the Conventional Adder which is required during the Partial Product generation with unique addition tree structure similar to Wallace addition tree structure It can be found that this design is better than conventional Vedic multiplication hardware in terms of speed[10]

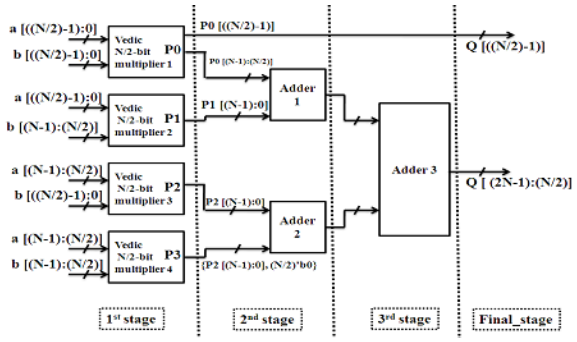


Figure 5.1: NxN bit Vedic multiplier architecture

6. Conclusion

In this paper, we have analyzed and discussed the importance of vedic multipliers in various signal processing applications. Vedic multiplication procedures are quite simple and efficient compared to the conventional multiplications. Many vedic sutras can be implemented in such applications which in turn will be very much cost effective and will be useful in designing high speed processors.

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