International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 03 Issue: 01 | Jan-2016 www.irjet.net p-ISSN: 2395-0072

An Enhanced Performance Pipelined Bus Invert Coding For Power Optimization Of Data Bus

Anukriti Kulshrestha [1], Ghanshyam Jangid [2]

[1]*Research Scholar, Suresh Gyan Vihar University, Jagatpura, (Jaipur)*
[2]*Co- Author (Assistant Professor), Suresh Gyan Vihar University, Jagatpura, (Jaipur)*

ABSTRACT- *Power dissipation is an important design constraint in today's CMOS VLSI design and is addressed widely by the researchers across the globe. Switching activity is one of the factors that affect dynamic power in a chip and several publications have suggested various techniques to reduce the same. In this paper, we propose a technique for bus encoding, which, reduces the number of transitions on the bus and performs better than the existing methods such as bus invert coding and shift invert coding for random data in terms of switching activity. we modify the bus-invert coding method to maximize the power consumption reduction of data bus.The proposed circuit in this paper is far better than its previous versions in terms of delay, number of transitions and hardware complexity. The proposed design is designed and implemented using verilog HDL in XILINX 9.2iversion.Experimental results demonstrate that the proposed circuit is faster and less number of transitions than its previous versions.*

Keywords – Partitioned Bus-Invert coding; Bus-switching; Low power , pipeline, FPGA.

1. INTRODUCTION

Power dissipation in CMOS circuits is a major concern for VLSI design. The power dissipation in CMOS can be classified in to two types, namely, dynamic and static power dissipation. While the static power dissipation is caused by leakage currents in transistors the major components of dynamic power dissipation is switching power and short circuit power. Switching power is dissipated when there is a transition from 1 to 0 or from 0 to 1. The probability of such transition is called switching activity. The Gray code [2] and the T0 code [3] is designed for instruction address bus which is assumed to be consecutive in value, while the bus-invert code [4] is design for data bus which is generally assumed to be random in value. The partial bus-invert [5] method is designed for data address which is assumed to be less random than data and less consecutive than instruction address. The segmental bus-invert coding [1] method is design for instruction memory data bus, which is assumed to be not evenly distributed. Other than add extra bus, extra information patterns is added to the tail of the original data packet for the reduction of switching active in data bus [6]. We have shown this concept in sections. Each and every section describes some specific points about the topic. Section I shows the introduction section II shows information about bus invert encoding section III & IV shows proposed work. Section V shows results and comparison and section VI gives details of conclusion and future.

2. BUS INVERT CODING

Bus-Invert method is used to coding and decoding the I/O which lowers the bus activity and thus decreases the I/O peak power dissipation by 50% and the I/O average power dissipation by up to 25% [1]. This happens because buses most have very large capacitances associated with them and consequently dissipate a lot of power. The peak power dissipation can then be decreased by half by coding the I/O as follows (Bus-Invert method):

i.Compute the Hamming distance (the number of bits in which they differ) between the present bus value (also counting the present invert line) and the next data value by using the majority voter logic circuit.

ii. If the Hamming distance is larger than n/2, set invert = 1 and make the next bus value equal to the inverted next data value.

iii. Otherwise let invert = 0 and let the next bus value equal to the next data value.

iv. At the receiver side the contents of the bus must be conditionally inverted according to the invert line, unless the data is not stored encoded as it is.

Mathematical Representation:

$$(Bus^t, Invert^t) = \{(bus^t,0) , Hamm.^t < N/2\}$$
$$\{(inv.\ bus^t,1) , Hamm.^t > N/2\}$$
$$\{(inv.\ bus^t,1) , Hamm.^t = N/2$$
$$(bus^t,0) , Hamm.^t = N/2\}$$

Where Bus^t stands for bus value at time t; $Invert^t$ stands for invert line value at time t; bus^t stands for data value at time t; $Hamm.^t$ stands for hamming distance between data value and bus value at time t.

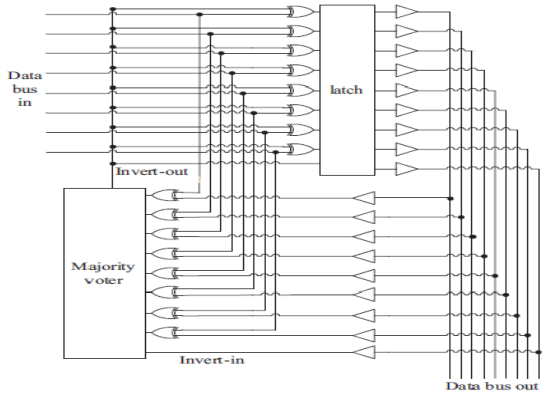

Fig 1- Bus Invert Encoder

The majority voter circuit can be implemented with a tree of full adders.

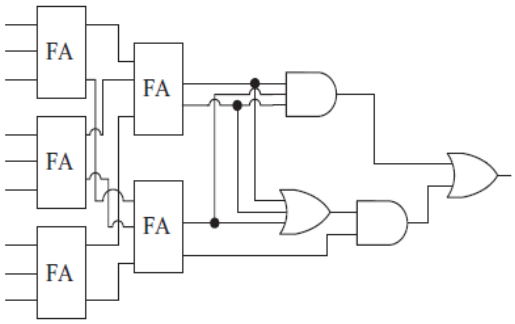

Fig 2- majority voter

3. PROPOSED WORK

We have proposed a new bus encoder which is more efficient than convention bus encoder. The proposed bus encoder is consisting of a comparator; two majority voters along with a multiplexer. The data input is comprising of 8-bits and its obvious to obtain 8-bit data as output too. A comparison is held between each bit of D_{in} and D_{out} respectively. So, the comparator will generate the certain sequence of compared bits of inputs and outputs, which then forwarded to the two majority voters. These majority voters will generate selective control signals based upon the data sequences which were inserted into them. Finally the whole will be multiplexed using multiplexer and at the end the output is taken and also it will be inserted again at the transmitting end for further comparison.

The proposed bus encoder architecture and algorithm are little bit same to bus invert encoder. The comparator and working of majority voter are same but architecture is different.

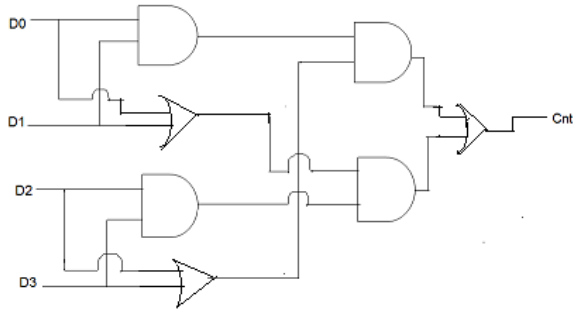

Fig 3- proposed majority voter circuit.

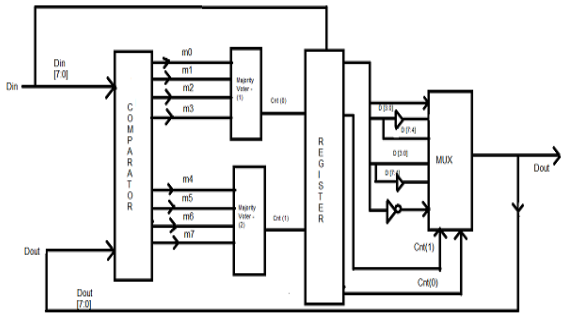

Fig 4- proposed pipelined bus encoder.

4. RESULTS AND CONCLUSION

In this paper, we evaluate the performance of conventional and proposed bus encoders and implement them on Spartan – 3 FPGA families. For Design Entry and delay report we synthesize these using Xilinx ISE 9.2i. We use verilog as hardware description language. This paper also gives the simulation or we can say the synthesis report obtained from the implementations of past and proposed works which clearly represents the better performance of our proposed work from the past works as there is a noticeable reduction in delay as well as power consumption parameters.

Table 1- switching comparison of past and proposed work.

Sr. No.	Bus encoder	No. of switching = 4	No. of switching = 3
1.	Bus invert encoder	5	4
2.	Proposed Bus invert encoder	1	**2**

Table 2- delay comparison of past and proposed work.

Sr. No.	Bus encoder	Delay
1.	Bus invert encoder	7.760ns
2.	Proposed pipelined Bus invert encoder	6.306ns

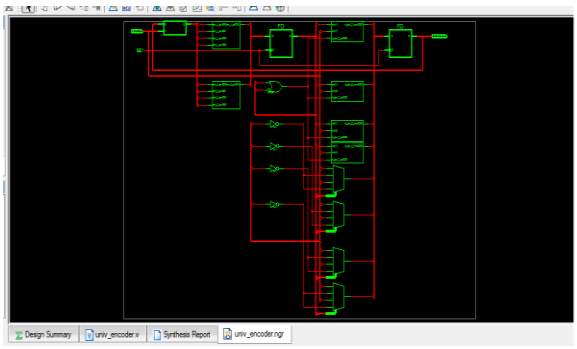

Fig 5- RTL view of proposed pipelined bus encoder.

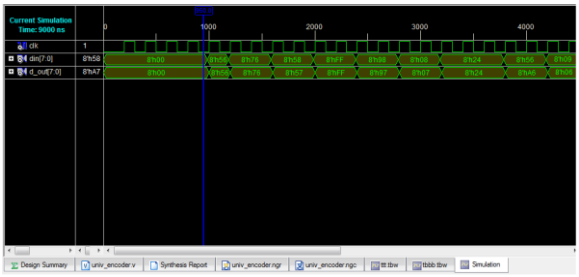

Fig 6- waveforms for proposed pipelined bus encoder.

5. CONCLUSION AND FUTURE WORKS

Here, in our proposed work, we have used the basic concepts of 'bus invert coding' and 'pipelining' to design a newer and better partitioned bus invert encoder, which is surely better than the previous ones in a number of circuit performance aspects.We have proposed a better design for 8-bit data bus. In the end, we can say that our work is better than the previous works and also efficient in terms of power consumption. This whole concept can further be used to attain more better results in future. We can also use state machine approach to increase the speed state machine is a sequential circuit which can reduced delay path.

REFERENCES

[1] M.R. Stan and W.P. Burleson, "Bus-invert coding for low-power I/O," IEEE Transactions on VLSI Systems, vol.3, no.1, pp.49-58, 1995.

[2] Sungpack Hong, Narayanan, Ki-Seok Chung and Taewhan Kim, "Bus-invert coding for low-power I/O – a decomposition approach," Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems, Lansing, MI , USA, vol.2, pp750-753, 2000.

[3] Y. Shin, S. Chae and K. Choi, "Partial bus-invert coding for power optimization od application specific system," IEEE Transaction on VLSI System, vo1.9, no.2, pp.377-383, 2000.

[4] Chih-Hung Kuo, Wey-Bang Wu, Yi-Jang Wu and Jia-Hung Lin, "Serial low power bus coding for VLSI," IEEE International Conference on Communications Circuits and Systems, Gui Lin, China,pp2449-2453, 2006.

[5] H Guo and Y Zhou, "A Segmental Bus-Invert Coding Method for Instruction Memory Data Bus Power Efficiency," Proceeding of the 2009 IEEE International Symposium on Circuits and Systems (ISCAS 2009), Taipei, Taiwan, pp137-140, 2009.

[6] Song Yu-yun, Hu Qing-sheng "A 0.18micrometer Pipelined 8BIOB Encoder for a High speed SerDes" 978-1-4244-6871-3/10/$26.00 ©2010 IEEE

[7] Junkai Sun and Anping Jiang, "Partitioned Bus-Invert Coding for Power Consumption Optimization of Data Bus," 978-1-61284-840-2/11/$26.00 ©2011 IEEE.