Analysis of different multiplication algorithm and FPGA implementation of recursive barrel shifter method for multiplication

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Abstract - ***Many of the today's real time signal processing algorithm included multiplication as its processing heart. In case of signal and image processing, it mostly used functional unit. In this review paper we are introducing logically new, fast and more efficient multiplication algorithm that seem to fulfilled fast processing requirement. This paper introduces how effectively we can use barrel shifter for implementation of multiplication method. Further work will carried comparative study of different multiplier with respect to some parameters like cost, power consumption, area and speed. For implementation and parametric analysis, we are using XC3S400 FPGA hardware platform, VHDL coding language for hardware description. Xilinx ISE-simulation tool has many inbuilt compatible tools for parameter analysis like XPE for power estimation that we are using here. Paper comprises description of current scenario, existed multiplication methods and our proposed algorithm.***

Key Words*: recursive barrel shifter, Karatsuba, binary one counter, Power predictor (PP), Vedic math.*

1. INTRODUCTION

Now days, for many application specific processor implementations such as real time signal processing, image processing, encryption, data manipulation requires high speed integrated circuit. Many signal processing algorithm make use of math-multiplier. There are different multiplication algorithm presently available and have implemented on SOC. Booth multiplier, Wallace tree multiplier, Karatsuba multiplier, Braun algorithm are more popular multiplication algorithm [2]. But many of them having their own restriction in terms of speed, on chip area, use of logic gates, energy, cost per cell, so in our project we are analyzing these many parameters and going to introduced one modified multiplication algorithm based on barrel shifter.

Barrel shifter has ability to shift any number to left or right (as per requirement) by N-position within only one clock cycle [1]. If we analyze this convenient barrel shifter behavior can used to implement multiplier that can multiply multiplicand number with multiplier number which should be perfect representation in power of 2 [3].

We are proposing new method based on barrel shifter used for multiplication of numbers which are not perfect two power representation.

1.1 Overview of existed algorithms

Multiplication methods that many of processors are using today are inspired by Vedic multiplier introduced in Indian Vedas with different 16 sutras. Vedic multiplier uses bit-wise multiplication with simultaneous product term finding and it's column-wise addition. It is one of the best benchmark for fast multiplication algorithm. Vedic math have introduces commonly used two methods as vertical crosswise multiplication and Nikhilam method [4].

Array multiplier is one of the bit-by-bit multiplication implementation approaches. Partial products are first generated and stored in memory from where it given to array of summation. As it performs operation on data in array form, so dedicated memory space is first prior to its implementation. Broun has described array multiplication with carry propagation adder [2].

Shift and add algorithm takes use of serial shifter and parallel adder. Both multiplicand and multiplier have dedicated or overlapped memory locations. This has improved at many stages to decreases size required to store multiplicand, multiplier and result. It checks for each bit of multiplier and take decision about what to do with multiplicand [2].

Another fast and more popular multiplication algorithm is Karatsuba algorithm which was named after Russian mathematician Anatolii Alexeevitch Karatsuba. Basic idea was to split the numbers into its two halves and find three auxiliary product terms u, v and w as below

$X = PQ = 10*P+Q$
$Y = RS = 10*R+S,$

Result = X*Y
= (10*P+Q) * (10*R+S)
= (P*R)*100 + ((Q*R) + (P*S))*10 + (Q*S)
= U*100 + middle*10 +W
V = (Q-P) * (S-R)
Middle term = U + W – V = (Q*R) + (P*S)

Thus, for N-bit number multiplication, the above same process can be use with multiple repetitions, but N should be the perfect representation in power of two [5].

Many of the above discussed multiplication algorithms seems to be reducing addition array size, but Wallace tree multiplier having ability to reduce number of total partial product terms as well. It make use of Booth Recode radix-x (x = 2, 4, 8) method for generating minimum partial product terms and 3:2, 4:2, 5:2 compressors to reduce addition further. It makes use of carry save adder at initial stages and carry propagation adder at final stage [6].

2. PROPOSED ALGORITHM

Here our algorithm makes use of barrel shifter; recursively for final computation. As we depicted above that barrel shifter can effectively used for number multiplication those are perfectly represented in power of two. But it can be used recursively if stated condition is not satisfied. Just below we have listed step to be followed by our algorithm-

1) Suppose X and Y are two each of N-bit numbers.
2) Count the number of ones in each number.
3) Number with smaller ones count will treat as a multiplier and other will be multiplicand.
4) Finding further successive power two representations of multiplier.
5) Now shift multiplicand by power of two to left
6) Give shifted result to adder
7) Repeat step 4 to 7 till power of two become zero.
8) Final adder result will be multiplication result

In step 3, selecting less ones count number as a multiplier so as to avoid unwanted shifting operation per clock cycle. Algorithm explanation with example gives as below-
Let us consider two number as A=11 (bX1011) and B=9(bX1001), ones count as OA(3) and OB(2)
B having two power indexes as 2^3+2^0
Shifting of A by 3 = (bX01011000)…… (1)
Shifting of A by 0 = (bX00001011)…… (2)

Final result will be as = (1) + (2) = (bX01100011) = 99.

Flowchart of algorithm gives clear idea of operation sequence-

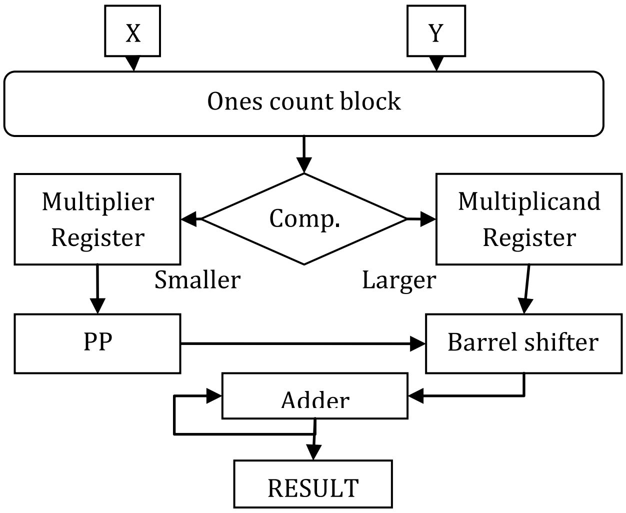

Fig 1: Algorithmic flowchart

3. CONCLUSIONS

Thus we have studied different existed multiplication algorithms and it restrictions in terms of power consumption, cost and speed. We have depicted in our algorithm the effective use of barrel shifter for multiplication.

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