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Design a Low Power Flip-Flop Based on a Signal Feed-Through Scheme

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Abstract - ***Flip-flops and latches are the most important elements of a design for both a delay and energy point of view. In many electronics design low power consumption is basic requirement in most of the applications. Therefore the energy performance requirements enhance the most designers of next generation system towards the least possible power consumption. The power consumption is basically reduced by scaling of a power supply voltage. Flip flops typically consumes more than 50% of power because of redundant transition of internal node. This paper proposes a new method of reducing the power dissipation. A low power flip flop design featuring pulse triggered structure based on signal feed-through scheme is presented which successfully solves the long discharging path problem in a various pulse triggered flip flop design and achieve a better power performance and better speed. In this paper we have studied the different architectures of low power flip-flops. A low power P-FF using adiabatic logic design is implemented using TSMC 65nm CMOS technology achieves more than 50% reduction in power. Based on simulation result the adiabatic logic design exhibits more than 50% energy saving as compared to ep-DCO FF, CD-FF, P-FF architectures.***

Key Words: *Flip-Flops, Pulse Triggered, Low Power, leakage power, Adiabatic Logic.*

1. INTRODUCTION

Flip-flops (FFs) are the basic data storage elements used extensively in all kinds of digital designs. Particularly, most of the digital designs nowadays often use pipelining techniques and built many FF-rich modules such as register file, shift register, and first in first out. Traditionally, the demand for high performance was accessed by increasing clock frequencies with the help of technology scaling. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and nearly all the storage elements, is nearly 50% of the total system power. FFs, thus, consumes a significant portion of the chip area and power consumption to the overall system design [9], [10].

Pulse-triggered Flip Flop (P-FF), having a single latch structure, is more popular than the conventional transmission gate and master–slave based FFs in high speed applications. Along with its speed advantage and simple circuitry P-FF helps to minimize the power consumption of the clock system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage. The latch acts like an edge-triggered FF, if the triggering pulses are sufficiently narrow. Since because of single latch structure, design of P-FF is simpler in respect to circuit complexity. This leads to a higher toggling rate for high-speed operations [11]–[12]. Pulse generation circuitry requires delicate pulse width control to deal with possible variations in process technology and signal distribution network. To obtain balanced performance among power, delay, area and speed, design space exploration is also a widely used technique [8]–[14].
Depending on the method used for pulse generation, P-FF designs can be classified as implicit or explicit [2]. In an implicit-type P-FF, the pulse is generated inside the flip flop; the pulse generator is a part of the latch design while it suffers a long discharging path with delayed timing operation. In an explicit-type P-FF, the pulse are generated externally, the designs of pulse generator and latch are separate. The Implicit pulse generation is often considered to be more power efficient than the explicit pulse generation. This is because the former merely controls the discharging path generating a pulse train and consumes more power. In pulse flip flop the delay variation in latching data '1' and '0' is observed which shorten the delay by introducing input signal directly to the internal node of latch design which result in increasing data transition speed and power delay product (PDP) performance. As the feature size of CMOS technology process decreases the more transistors, the more switching activity and the more power dissipated in the form of radiations or heat. Most of the researchers have worked on low power flip-flop design, but they are mostly focused on one or a few types of flip-flops architecture or

applications. The need for comparing different designs and approaches is the main motivation for this paper. Adiabatic logic style is proving to be an attractive solution for low power digital design. The many researchers have introduced different adiabatic logic styles in last few years and proved that these are better than CMOS. In this paper, we have proposed a new technique to further reduce the energy dissipation of any adiabatic circuit. The simulation results show our technique outperforms the previous quasi adiabatic circuits in terms of energy consumption.

2. ARCHITECTURES OF LOW POWER FLIP FLOP DESIGN

2.1 Conditional Discharge Flip Flop

In [1] the author classified this flip-flop architecture into two categories i.e. conditional pre-charge and conditional capture technologies. This classification is based on how to prevent or reduces the redundant internal switching activities. The figure 1 shows the conditional discharge technique, is proposed in [1] for both implicit type and explicit type pulse-triggered flip-flops without the problems associated CDFF

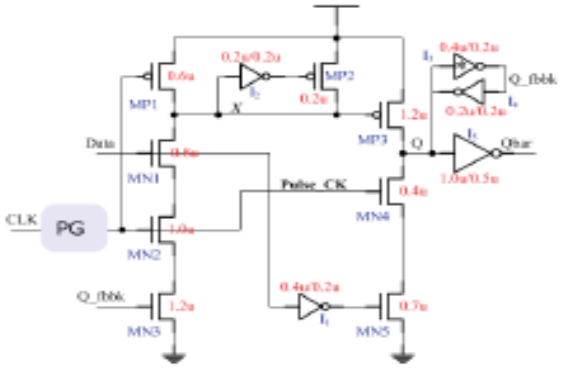

Fig.-1: Schematic of Conditional Discharge flip-flop [5]

Conditional discharge with the conditional capture technique. In this technique, the extra switching activity is reduced by controlling the discharging path when the input is stable HIGH and, therefore, the name given Conditional Discharge Technique. Therefore the conditional discharge is introduced to eliminate the switching activity at the internal nodes of flip flop. The conditional discharge technique used in implicit type of flip flop design. The semi-dynamic nature of these flip-flops provides different internal power dissipation based on input data distribution as compared to a fully static master slave structure. This is because the pre charge node of the dynamic stage is charged and discharged during each clock cycle even if the input data remains at a high logic. Therefore, hybrid designs can have held internal power dissipation for some input patterns due to the pre charge nature of the front end stage. Parameters and the reference values are illustrated in table 1.

Table -1: Parameters for CD-FF

Sr. No.	Parameters	Reference Value
1.	Technology	180nm CMOS
2.	Simulation	HSPICE
3.	Supply Voltage	1.8V
4.	No. of Transistors	28
5.	Power	20.2µw

2.2 Pulsed Triggered (P-FF) Flip Flop

In [5] the author proposed the method of low power design pulse triggered flip flop based on signal feed through scheme for improving the delay. Here the signal feed through scheme uses the pulsed generator circuitry which generates the pulse of sufficient width which is useful in driving the signal from input node directly to the output node. The [5] flip flop is distinct from the previous flip flop architecture design. The changes made in [5] used P-Mos transistor in the first stage of flip flop latch structure. The charge keeper circuit is eliminated in [5] design which makes circuit simple.

The pass transistor MNx incorporate for a discharging path purpose, the main important role of a pass transistor MNx is for providing extra driving to node during 0 to 1 data transition and for discharging node Q during "1" to "0" transition of data. The extra element introduced is an n-MOS pass transistor (MNx) for supporting signal feed through scheme. The Technology used is TSMC 90 - nm CMOS process. The pulsed width is most important factor in latching or holding of data in to the pulsed flip flop for low power consumption. The pulsed flip flop (P-FF) makes signal feed through technique to improve this delay. The parameters and the reference value are illustrated in table 2.

Table -2: Parameters for for P-FF

Sr. No.	Parameters	Reference Value
1.	Technology	TSMC 90-nm CMOS
2.	Simulation	HSPICE
3.	Supply Voltage	1.8V
4.	No. of transistors	24
5.	Delay (D-Q)	109.1ps
6.	Power	16.06 µw

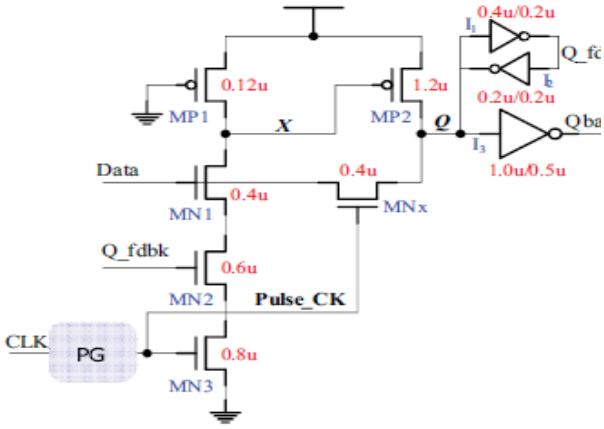

Fig.-2: Schematic of P-FF design ref [5]

The architecture of a pulsed (P-FF) flip flop design is illustrated in figure 2.

2.3 Explicit Pulsed Data Close Output (Ep-DCO FF) Flip Flop

For the high-performance applications, such as the critical paths of a circuit design, for obtaining a smaller flip-flop delay is most important while the lower power consumption is a secondary requirement [18]. The fast (D to Q) data-to-Q delay of the pulsed semi dynamic flip-flops, however, comes at the expense of significant power consumption. The main important reason for this high power consumption is the dynamic nature of the flip-flop, the power may be consumed in the dynamic stage due to the pre-charging and evaluate cycle even when the input is maintained constant. In an implicit type P-FF, the pulse is generated inside of flip flop and is a part of the latch design and no explicit pulse signals are generated

An explicit-pulsed data close output flip flop (ep-DCO) schematic in Figure 3

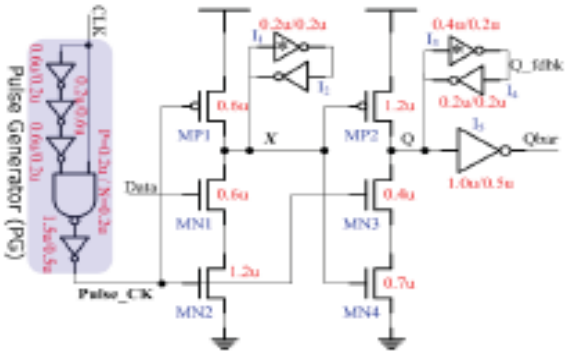

Fig.-3: Schematic of EP-DCO FF design ref [5]

The explicit pulsed data close output does not offer any performance advantage over implicit-DCO, and consumes more energy due to the externally generated pulse. However, the pulse generator power consumption can be significantly minimized by sharing a single pulse generator among a group of flip-flops. Thus performance of the both ip- DCO and ep-DCO with shared pulse generator gives the best among all semi dynamic flip-flop as far as of speed and critical paths is concerned. PF-FFs, in terms of pulse generation, can be classified as an implicit type and explicit type. In an implicit type P-FF, the pulse is generated inside of flip flop and is a part of the latch design and no explicit pulse signals are generated. In an explicit type P-FF, the pulse is generated outside the flip flop, the pulse generator circuit and the latch are separate [5]. The implicit type P-FFs are generally more power-economical without generating pulse signals externally however, they suffer from a longer discharging path, which leads to inferior timing characteristics.

In this P-FF architecture, the inverters I3 and I4 are used for latching of data, and inverters I1 and I2 are used for holding the internal node *X*. The delay of three inverters determines the pulsed width; this design suffers from a serious drawback i.e., the internal node *X* is discharged on every rising edge of the clock in spite of the presence of a input "1". This gives rise to large switching power dissipation [5].

3. PROPOSED P-FLIP FLOP ARCHITECTURE [5]

3.1 Block Diagram Of Proposed Flip Flop (P-FF)

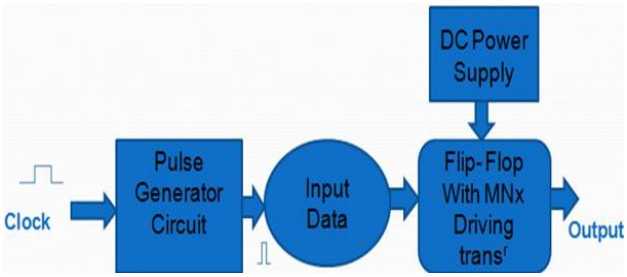

Fig.-4: Block diagram of proposed P-flip flop

Figure 4 shows block diagram of proposed P- flip flop design consist of pulse generator circuit, flip-flop and power supply. The pulse generator circuit adjusts a width of pulse for the proper operation. The input data in the form of logic '0' and logic '1', the flip flop with pass transistor Mnx is basically driving transistor which keeps the input stage of the FF from any driving effort. At the same time, the input data and the output feedback Q_fdbk assume complementary signal levels and the pull-down

path of node *X* is off. Therefore, no signal switching occurs at any internal nodes.

3.2 Design Of Proposed P-Flip Flop (P-FF)

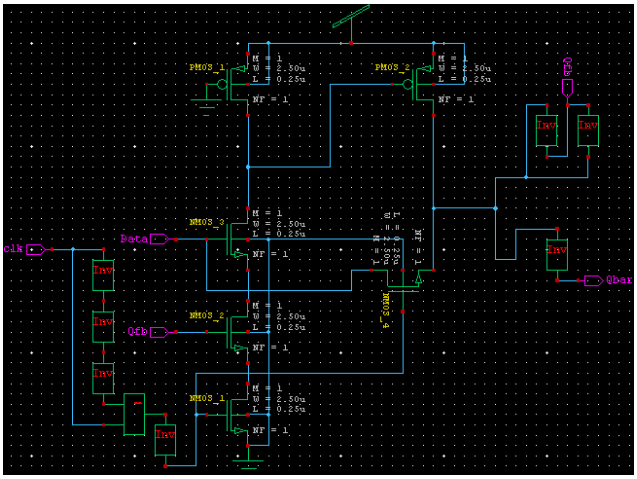

Fig.-5: Design of proposed P-flip flop.

4. PROPOSED DESIGN OF P-FF USING ADIABATIC LOGIC

4.1 Block Diagram Of Proposed P-Ff With Adiabatic Logic

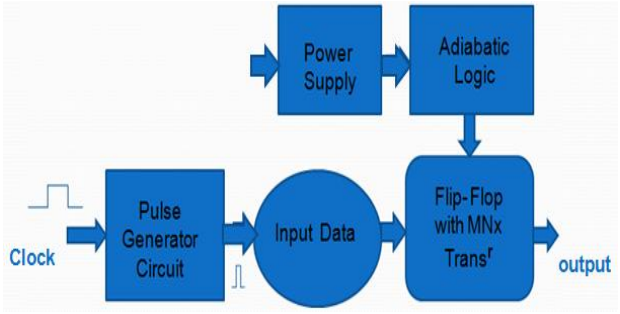

Fig.-6: Block diagram of proposed P-flip flop with adiabatic logic

Figure 6 shows block diagram of proposed design of p-flip flop with adiabatic logic. It consist of pulse generator circuitry, input data for selecting the data bit either '0' or '1'. The Flip flop is for storing the bit information in the form of logic '0' and logic '1. Adiabatic logic is an attractive low-power approach by utilizing supply voltage (power-clocks) to recycle the energy of the circuits instead of being dissipated as heat. Another major advantage of adiabatic logic families is their best behavior for lower generation of switching noise, which is becoming one of the most important problems in current digital and especially in mixed mode integrated circuits. Since the proposed signal feed-through scheme requires occasional signal driving from the input node directly to the output node, we also calculate the power drawn by the MNx pass transistor.

4.2 Design Of Proposed P-Flip Flop With Adiabatic Logic

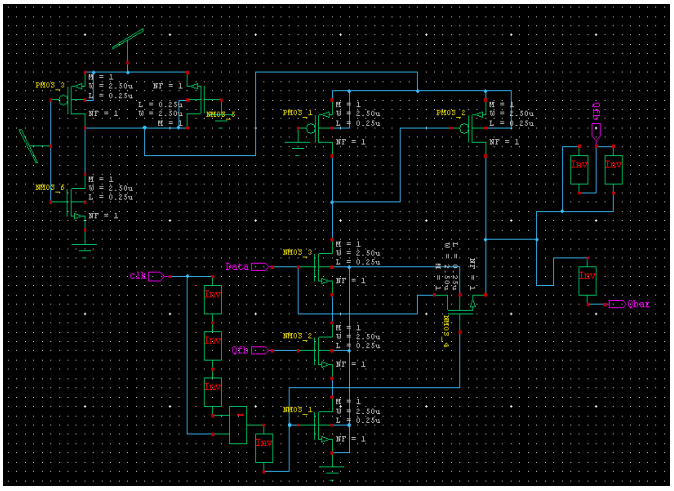

Fig.-7: Design of proposed p-flip flop with adiabatic logic circuit

Since the pass transistor MNx is turned on for only a short time slot, the loading effect to the input source is not significant.

In particular, this discharging does not correspond to the critical path delay and calls for no transistor size adjust finely to enhance the speed.

1. When Pulse is High, Then

   D=MNx, MNx is on then D is copied to Q

2. When Pulse is Low, Then

   i) Qfdb and D =0 then Q=0 state is maintained
   ii) Qfdb and D =1 then Q=1 state is maintained

5. SIMULATION RESULT

The performance of the proposed design of P-FF using adiabatic logic is evaluated against existing designs of proposed P-FF by simulations. The target technology is 65- nm CMOS process. The tool used for the simulation is Tanner Tool V_14. Since pulse width design is crucial to the correctness of data capture as well as the power consumption. A conventional CMOS NAND logic based pulse generator design with a three stage inverter chain which incorporate for selecting the proper pulse width to

ensure the proper operation of a flip flop. Since, the proper pulse width is used for latching of data in the internal node of flip flop. The sizing also ensures that the pulse generators can function properly in all process, since the proposed design requires direct output driving from the input source, for fair comparisons the power consumption of the data input buffer (an inverter) is included. The output waveform of proposed design p-flip flop and proposed design of p-flip flop using adiabatic logic circuit is shown in figure 8 and in figure 9 for the input data i.e i/p data=1, The output V(Q)=1 and output V(Qbar)= 0 when the i/p data =0, V(Q)=0 and V(Qbar)= 1.

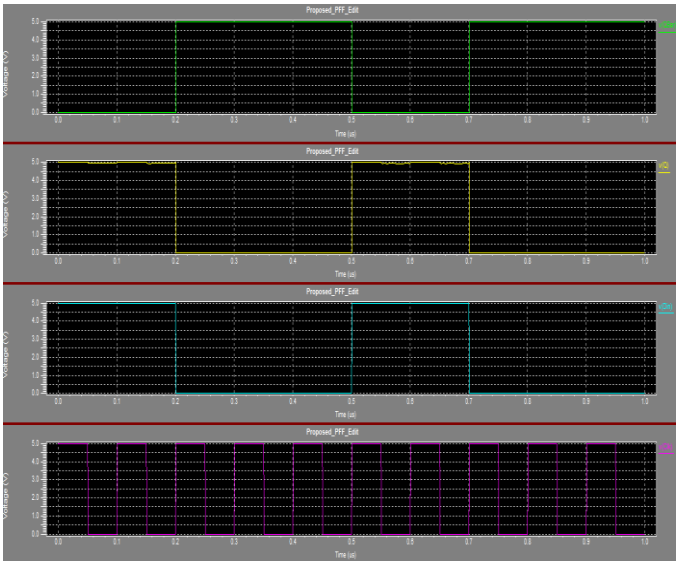

Fig.-8: Simulation result of proposed P-flip flop.

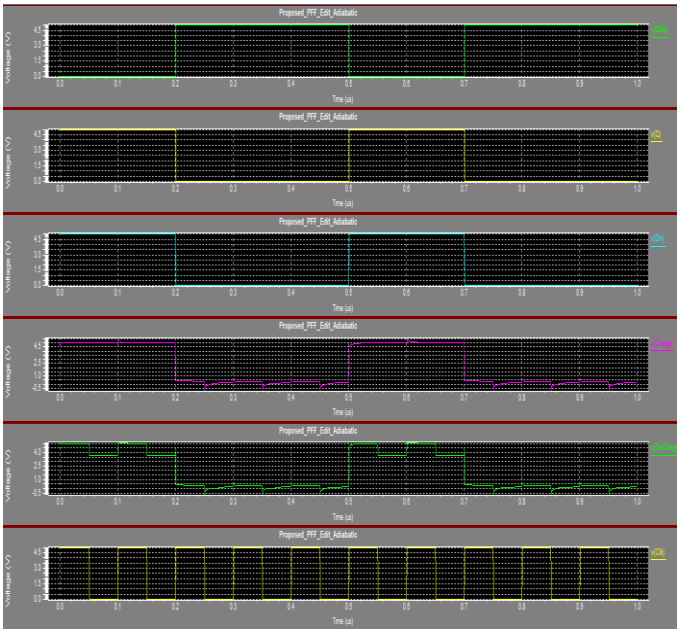

Fig.-9: Simulation result of proposed P-flip flop with adiabatic logic

6. COMPARISON TABLE

The comparison table of all flip flops are and the modified design of proposed p-flip flop with adiabatic logic.

Table -3: Simulation Result table

Parameters	P_FF [5]	P-FF design	Design of P-FF with adiabatic
No. of transistors	24	24	27
Tool Used	-----	Tanner tool v 14.1	Tanner tool v 14.1
Technology Used	TSMC CMOS 90nm	90nm	65nm
Delay (D-Q)	109.1 ps	944 .56 ps	944.56 ps
Avg. Power	16.06 μW	10.33 μW	2.596 μW
Optimal PDP	2.13 pJ	9.75 pJ	2.452 pJ

7. CONCLUSION

In this Paper, We have presented the modified proposed p-flip flop design by incorporating adiabatic logic circuit. The key idea is to provide a signal feed through from input source to the internal node of the latch, which provide extra driving facility to shorten the transition time. This paper presented different architectures of a low power flip flop structure. In this paper we have studies the basic architectures of a Flip flop design of CDFF, EP-DCO FF and Pulsed triggered flip flop for low power consumption with their comparative results. The power performance of proposed design of P-flip flop using adiabatic logic is more efficient than the CDFF, EP-DCO FF. In future we minimize the area and delay of a P- flip flop.

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