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DESIGN & SIMULATION OF ON CHIP I²C PROTOCOL USING ADVANCED MICROCONTROLLER BUS ARCHITECTURE (AMBA)

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Abstract – ***This project is based on designing and simulation of on-chip I2C protocol. The efficient bus architecture AMBA will be designed in this to provide the advanced bus functionalities. The designing of the system will be carried out with the Xilinx VHDL with schematic input (IEEE STD). Simulation results of the overall system will be verified using ISIM. For the future prospective upgradeability and Customization benefits of programmable logic may be obtained by FPGA implementation.***

Key Words: *AMBA, On-chip I2C protocol, FPGA.*

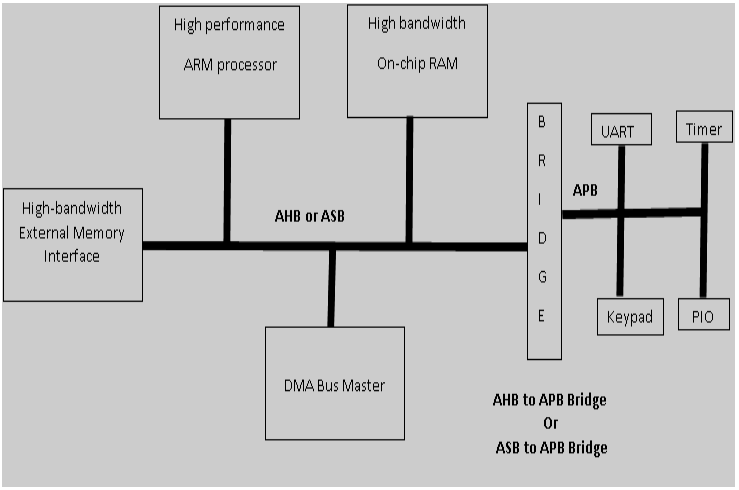
1. INTRODUCTION

1.1 Introduction to Advanced bus architecture

The advanced bus architecture is the high speed bus standard defined to operate for high frequency controllers. In high speed microcontrollers which supports the system on chip SOCs, it requires high speed busing systems to connect various components, such as one or more microprocessors, memory, peripherals and various logic devices etc. Different silicon manufacturers uses different bus architectures such as IBM's CoreConnect, Silicore's Wishbone, ARM's AMBA bus system etc. In the defined system the bus system being design is the AMBA i.e. Advanced Microcontroller Bus Architecture.

2. Advanced Microcontroller Bus Architecture (AMBA)

The Advanced Microcontroller Bus architecture is the multilevel busing system that defines a system bus and a lower level peripheral buses under it:



AHB/ASB:
Advanced High Speed and Advanced System Bus are designed to provide address requirements of high performance synthesizable designs. These are the high-performance system buses that supports multiple bus masters and provides high-bandwidth operations.
AMBA AHB supports the features required for high-performance, high clock frequency systems including: Burst transmits, split transactions, single-cycle bus master handover, one clock edge operation, non-tristate implementation, wider data bus configurations (64/128 bits).
ASB is a non-multiplexed bus with a single data bus Like the AHB, the ASB is a pipelined, multi-master bus that supports bursting0It's a simpler bus and doesn't support split transactions.
Like AHB, it enables a master to "lock" the bus, i.e., reserve the next bus access for itself. Bus transfer types include Address-Only, Non-sequential, and Sequential. Address-Only (no data) is used for idle cycles, bus master hand-over cycles, and speculative address decoding. Non sequential is implemented for a single transfer or the first transfer of a burst. Sequential is employed for the successive burst transfers.

APB:

Advanced Peripheral Bus is defined to fulfill the requirements of low-speed peripherals like UART, keyboards and many other portable input output devices.

The advanced peripheral bus is the simple bus that supplies a simple address with latched address and control signals for interfacing and can be implemented with a single tri-stated data bus. APB do not provides bursting.

Each operation consists of two cycles:

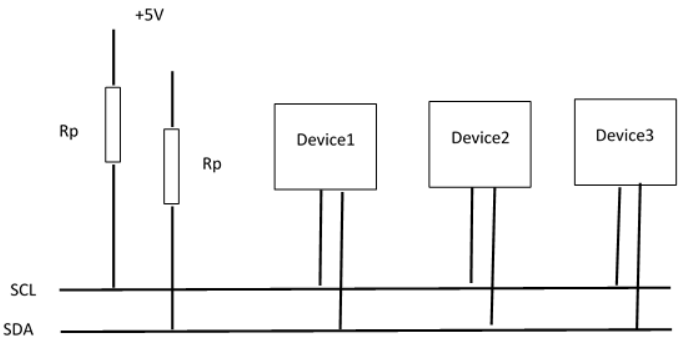
An address cycle (Setup state) and a data cycle (Enable state). The bus requires a single clock, PCLK.

In operation mode the bus turns PSEL and PWRITE up, putting the address on the PADDR address bus. In the Enable state, it turns PENABLE up and places data on the PWDATA/PRDATA bus.

The enable signal, PENABLE, is disabled on the next clock.

3. Inter Integrated circuit I2C Protocol

The Inter Integrated Circuit I2C is the two wired protocol contains two wires named SCL and SDA. SCL is the serial clock line which is used to synchronize all data transfers over the I2C bus. SDA is the serial data line. The SCL & SDA lines are connected to all devices on the I2C bus. For the line to be able to go high you must provide pull-up resistors to the 5v supply. There should be a resistor from the SCL line to the 5v line and another from the SDA line to the 5v line.



The devices on the I2C bus are either masters or slaves. The master is always the device that drives the SCL clock line. The slaves are the devices that respond to the master.

A slave cannot initiate a transfer over the I2C bus, only a master can do that. There can be, and usually are, multiple slaves on the I2C bus, however there is normally only one master. Both master and slave can transfer data over the I2C bus, but that transfer is always controlled by the master.

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