One-Cycle Control of Interleaved Buck Converter with Improved Step-Down Conversion Ratio

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Abstract - ***One of the main disadvantages of the buck converter and the interleaved buck converter is the narrow duty cycle which limits the application of the converters for high step-down applications. The interleaved buck converter with high conversion ratio overcomes this drawback. This converter provides continuous input current and also reduces the voltage stress of the semi-conductor devices to below the input voltage. This is possible due to the presence of two input capacitors. Also, compared to the conventional interleaved buck converter the converter provides much lower output current ripple. The simulation of the circuit with 200 V input, 24V/10A output is done using MATLAB. One-cycle control is used to generate the gate pulses.***

Key Words: *Buck converter; interleaved structure; high step-down conversion ratio; one-cycle control.*

1. INTRODUCTION

The step-down power conversion technique is widely used in power sources for LED drivers, microprocessors, battery chargers, solar power regulators and so on. These applications require low current ripple, which can be achieved by increasing the switching frequency. However, these may lead to high semiconductor losses. The buck converter is widely used for step-down dc-dc conversion when there is no isolation requirement. The conventional buck converter is very efficient when not too large a potential difference separates the output voltage from the input voltage (i.e., when the duty cycle D is high, and typically over 50%).

The main drawback of the buck converter is the low on-time of the switch in the case of high-step down applications with high switching frequency. Thus, the regulation period is very short and becomes very difficult in high frequency applications. In applications where non-isolated, high step-down conversion ratio and high output current with low ripple are required, interleaved buck converters (IBC) have received a lot of attention. Fig. 1. shows the conventional interleaved buck topology. However the semiconductor devices in the conventional IBC suffers from input voltage stress and hence various topologies have been introduced to reduce the voltage stress. In [2] an IBC having low switching losses has been implemented by carrying out zero current transition. [3] describes a topology in which the switches are connected in series rather than parallel. The voltage stress of the semiconductor devices is half of the input voltage after turn-on and before turn-off. However, the input rms current is high in spite of the interleaved structure. [4] introduces a two phase transformer-less interleaved structure with an improved step-down conversion ratio and lower switch voltage stress. It can be noted that in [4] for a 2 phase converter 4 switches are used and the number of components are higher. Thus, the topology becomes more complicated as the number of phases increases.

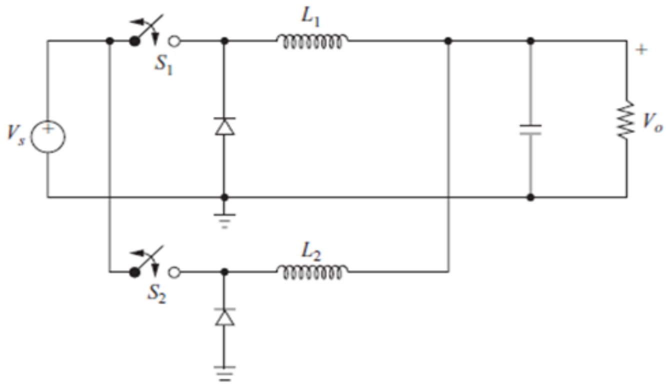


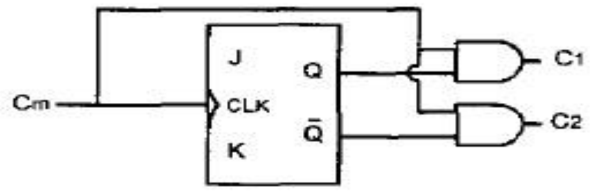
Fig -1: Conventional IBC

An application of IBC is seen in [5]. Standard buck converters require high value inductor to reduce the current ripple. Due to the high value of inductor and high switching frequency, the dimming frequency is reduced which results in audible noise. Thus, IBC are used as a high brightness LED electronic driver. Also, fuel cell plate and lead-acid battery lifetime depends on the ripple current drawn [6], [7], i.e., the output ripple current of the converter has to be low. For such applications IBCs are more preferred.

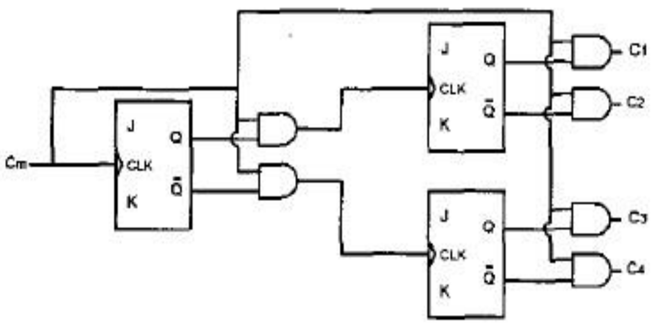
[8] - [9] use coupled inductors/tapped inductors to improve the efficiency of the interleaved converters. In [8], a coupled inductor is used to further reduce the size of the

IBC. But the main drawback is the presence of leakage inductance in the coupled inductors which may cause a huge voltage spike during transients. In [9], extra two phase windings are introduced to extend the duty cycle of the interleaved structure. In order to minimize the voltage spike an extra clamp circuit has also been introduced. This increases the complexity of the circuit. A tapped inductor structure is given in [10] to extend the duty cycle and reduce the voltage stress. But in this topology also a clamp circuit is utilized which makes the circuit complex. In [11], zero voltage switching (ZVS) is achieved using an auxiliary switch, a diode and a coupled inductor. The main drawback is that to achieve ZVS in one switch, a number of components have to be added. In [12], ZVS achieved using a tapped inductor or a transformer. In this topology a part of the energy is directly transferred to the load. The current stress of both the primary and secondary sides is reduced considerably, but the drawback of the circuit is that the conversion ratio is limited.

In [13], the origin of three-level converters is discussed. The three-level topologies of half bridge converter and buck converter is discussed in detail. In [14], a modified three-level buck converter sharing the input and output is discussed. The modification is carried out using a dc voltage blocking capacitor. The modification also reduces the switch stress. The main drawback of the three-level converters is that number of components is more.



(a)



(b)

Fig -2: Control pulse generation circuit proposed in [18] (a) For two interleaved phases, (b) For four interleaved phases

[15] discusses a buck converter which operates at two frequencies. The circuit consists of two buck cells which operate at two different frequencies. The control strategy of the topology is difficult. In [16], interleaved buck converter is used for power factor correction application. The circuit is operated at boundary conduction mode to increase the efficiency and eliminate the reverse recovery loss of the diode. Adaptive master-slave interleaving control technique is used. Phase management is possible using the interleaving technique.

In [17], the design of the passive elements present in the interleaved converter is discussed. The relationship between the number of phases and the passive element design is given. PWM generated pulses are provided as gate signals to the interleaved converters. [18] discusses a hysteretic controller which provides the required pulses for the interleaved converter. The control circuit for N number of phases is described. Fig. 2 shows the control pulse generation, proposed in [18], for two and four interleaved phases. It must be noted that the current shared among the phases of the interleaved converter are balanced. Imbalance in the duty ratio causes one phase to operate at continuous conduction mode and the other phase to operate at discontinuous conduction mode. In [19], a comparison of the current sharing in non-isolated and isolated converters with interleaved structure is discussed.

In this paper, an interleaved buck converter with improved step-down ratio using one-cycle control scheme is introduced. The converter consists of two input capacitors which help to reduce the semi-conductor switch stress. The main advantage of the proposed converter is the improved step-down conversion ratio. Compared to the conventional IBC, the introduced converter has continuous input current. One-cycle control scheme is utilized which provides the advantage of faster response time.

The paper is organized as follows: Section 2 describes the circuit configuration and the converter operation is explained in Section 3. The control strategy utilized is described in Section 4. MATLAB simulation along with results is explained in Section 5. Finally, the conclusion is stated in Section 6.

2. CONVERTER CONFIGURATION

The interleaved buck converter with high step-down conversion ratio has been shown in Fig.3. The converter consists of two input capacitors C_{in1} and C_{in2}, two switches which are triggered 180 degrees apart, 2 phase inductors L_1 and L_2 and an output inductor L_o. Due to the presence of input capacitors, the voltage stress across the semiconductor devices is much less than the input current. The conversion ratio of the converter is lower than that of the conventional interleaved buck converter. The converter does not require any additional current sharing control block.

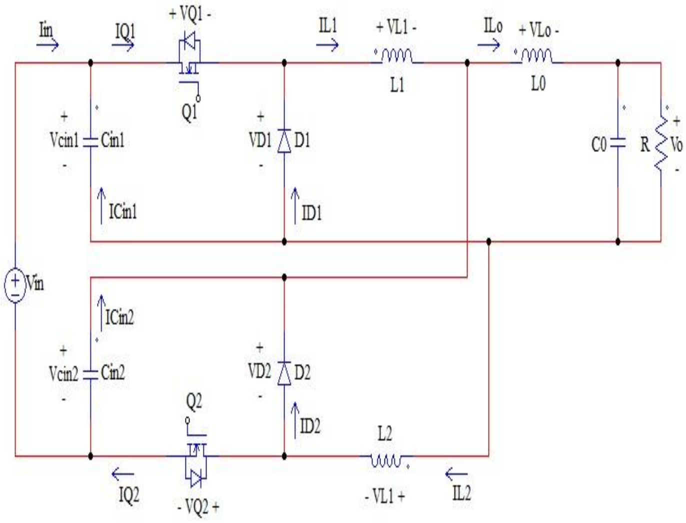


Fig -3: Circuit configuration of the interleaved buck converter with high step-down conversion ratio

The conversion ratio of the conventional interleaved buck converter is D whereas the conversion ratio of the interleaved buck converter with high step-down conversion ratio is D/(2-D). Similarly the semiconductor voltage stress of the conventional IBC is equal to the input voltage, whereas in the converter given in Fig. 3, the semiconductor voltage stress is V_{in}/ (2-D).

3. CONVERTER OPERATION

Initially both the freewheeling diodes are forward biased and the capacitors C_{in1} and C_{in2} are being charged. First the switch Q_1 is turned ON and Q_2 is OFF. During this interval, the diode D_1 is reverse biased and D_2 is forward biased. Inductor L_1 is charging and L_2 is discharging. Input Capacitor C_{in1} is discharging and C_{in2} is charging. During the next interval both the switches are OFF and both the freewheeling diodes D_1 and D_2 are conducting. Inductors L_1 and L_2 are discharging and input capacitors C_{in1} and C_{in2} are charging. In the next interval, Q_2 is ON and Q_1 is OFF. This interval is symmetric to the interval where Q_1 is ON and Q_2 is OFF. During this interval, the diode D_2 is reverse biased and D_1 is forward biased. Inductor L_2 is charging and L_1 is discharging. Input Capacitor C_{in2} is discharging and C_{in1} is charging. In the next interval, both the switches are again OFF.

4. CONTROL STRATEGY

The most simple and stable method to trigger the semi-conductor devices is by using Open-Loop control technique. The main disadvantage of open-loop control is that the output is independent of the changes in the load or line, thus the output varies accordingly. In order to obtain a constant output, Closed-Loop control schemes are introduced. The most simple and commonly used closed-loop control is the PWM technique. In PWM control, the control signal is compared with a reference signal (commonly used reference signals are ramp wave, triangular wave or sine wave). The main disadvantage of the PWM technique is the slow response time, i.e., when the line or load changes suddenly the error signal must change first and only after that the appropriate gate pulses are obtained. Thus, a transient over-shoot is produced. A large number of cycles are required to reach steady state.

One-cycle control scheme is a non-linear control technique which forces the mean value of the switched variable to be equal to the reference value. A PI controller is added along with the one-cycle control to obtain improved one-cycle control. The basic block diagram of the one-cycle control is given in Fig.4.

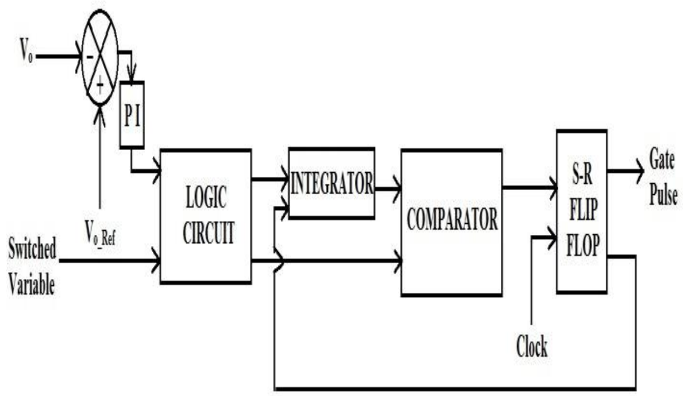


Fig -4: Block diagram of One-Cycle Control

For the introduced converter, equation (1) is implemented using one-cycle control. The reference signal is two times the output voltage and the switched variable is considered as the sum of the input voltage and the output voltage.

$$2V_o=(V_{in} +V_o)\ D \quad (1)$$

The main advantage of one-cycle control is the ability to cancel out the disturbances in the line voltage. Using improved one-cycle control the load regulation is also obtained.

5. SIMULATION

The simulation of the interleaved buck converter with improved step-down conversion ratio has been carried out and the simulink model is shown in Fig.5. An input voltage of 200V and switching frequency of 100 kHz is chosen and an output of 24V/10A is obtained. The duty ratios of both the switches are equal to 0.214 and the corresponding parameters are listed in Table 1.

Table -1: Parameter values of the simulated converter

Parameter	Value
Input Voltage	200 V
Output Voltage	24 V
Power Level	240 W
Switching Frequency	100 kHz
L_1 and L_2	100 µH
L_o	5 µH
C_{in1} and C_{in2}	4.4 µF
C_o	1 µF

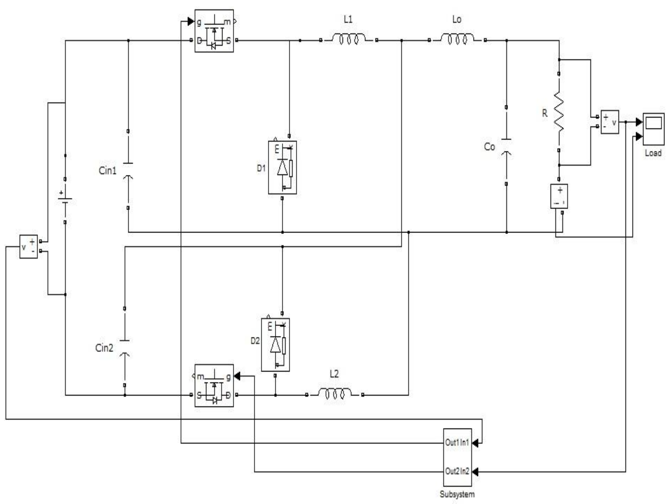
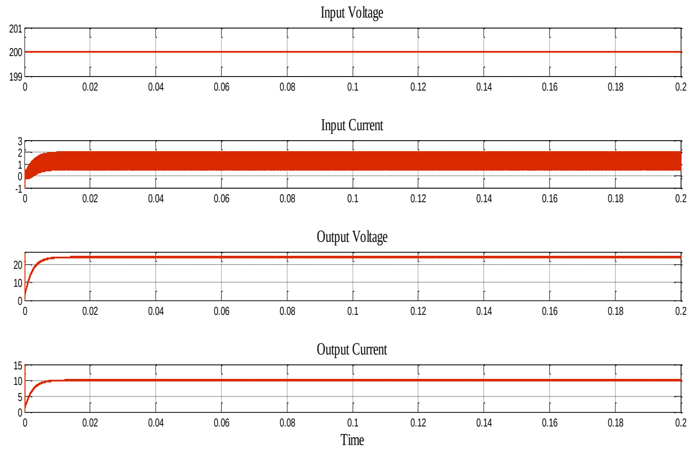


Fig -5: Simulink model of the converter



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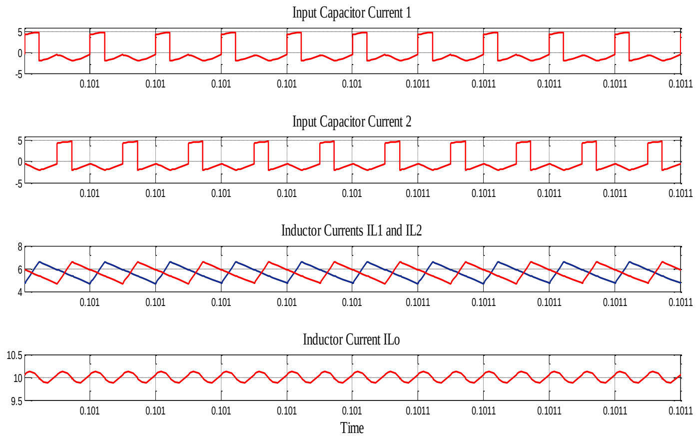

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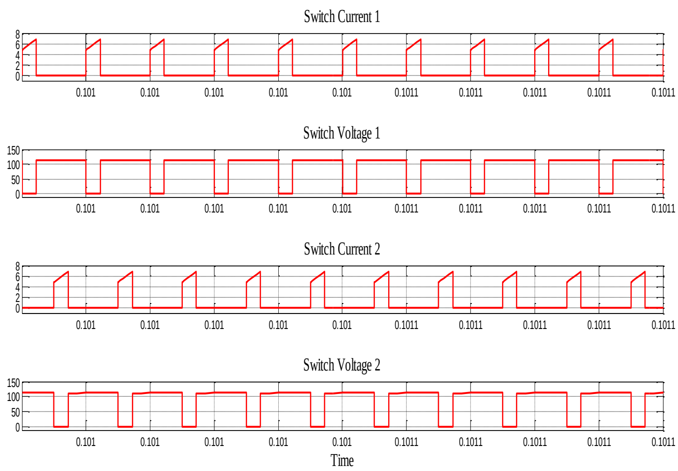

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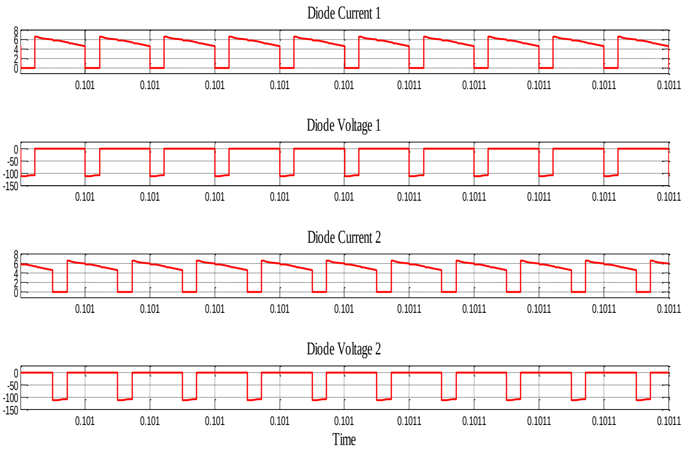


(d)

Fig -6: Simulated key waveforms of the converter

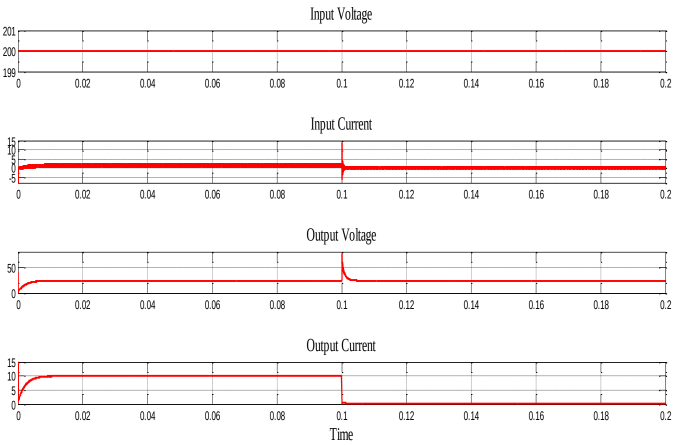
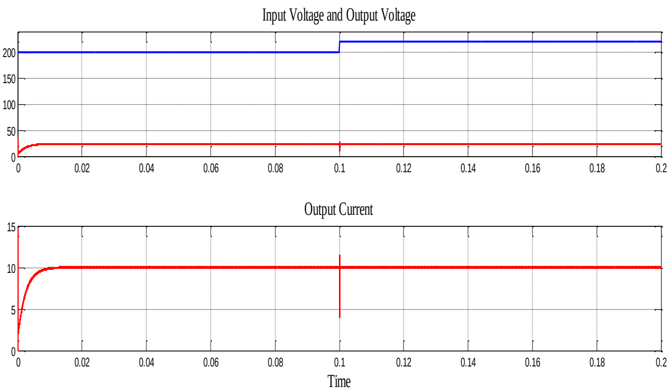
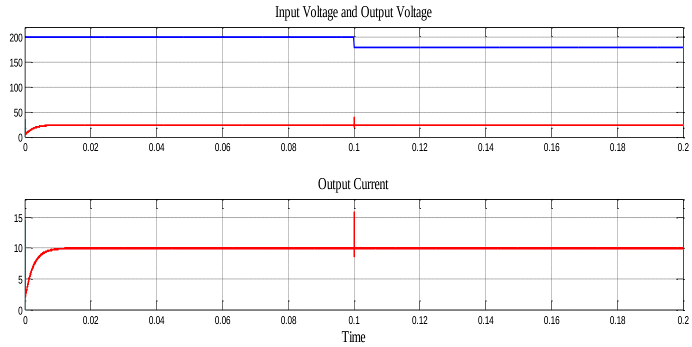


Fig -7: Load regulation of the converter



(a)



(b)

Fig -8: Line regulation of the converter at (a) V_{in} = 220 V (b) V_{in} = 180 V

The input voltage of 200 V has been stepped down to 24 V. Fig.6(a). shows the input voltage (200 V), input current, output voltage and output current waveforms. It is clear from Fig. 6(a) that the input current is continuous. Continuous input current is one of the main features of the converter. It can be noted that the output ripple current is highly reduced. The current waveforms of the two input capacitors and also the inductor current ripples of L_1, L_2 and L_o can be seen in Fig. 6(b). Fig. 6(c) shows the voltage and current stress of the switches and Fig. 6(d) shows the voltage and current stress of the diodes. The voltage stress of the diodes and the switches are approximately 110 V, i.e., less than half the input voltage whereas in the conventional interleaved buck converter, the voltage stress of the semi-conductor devices are equal to the input voltage. Theoretically, the voltage across the inductor L_o is zero, but due to the voltage ripple present in the input capacitors C_{in1} and C_{in2} and the output capacitor C_o, there is a small ripple voltage present across L_o. The load regulation can be seen in Fig. 7. The line regulation at Vin = 220 V and Vin = 180 V are given if Fig 8(a) and Fig. 8(b) respectively.

6. CONCLUSIONS

The main features of the interleaved buck converter with high step-down conversion ratio have been discussed. The main advantages of the converter include: (1) Improved step-down conversion ratio (2) Continuous input current (3) Lower semiconductor voltage switch stress and (4) Extremely low output current ripple. One of the main features of the converter is that an additional current sharing circuit is not required for the converter. One-cycle control scheme is used to produce the gate pulses for the switches. The simulation of the converter with 200 V input and 24 V/10 A output has been carried out using MATLAB software.

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