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REVIEW ON DESIGN OF HIGH SPEED ARRAY MULTIPLIER USING BICMOS LOGIC

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Abstract- ***The new combination of semiconductor technology BiCMOS is evolved from two formerly separate technologies those are Bipolar Junction Transistor and CMOS transistor. BiCMOS logic has several advantages such as low static power dissipation, large load drive capabilities and fast switching. Multiplier is one of the most important arithmetic unit in Microprocessors and DSP applications. This paper presents design of Array multiplier using BiCMOS logic. The designs for proposed multiplier will be done on TANNER S-Edit tool and simulated on T-Spice.***

Key Words- CMOS, Power dissipation, adder, CSA, CLA, latch up, BiCMOS, Array multiplier, TANNER Tools.

INTRODUCTION

The use of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been growing at a very fast pace. CMOS technology has become the mainstream fabrication technology for memories and microcomputers because of its high density and low power features. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. But some applications such as computer and communication systems require better speed performance than that obtained by CMOS technology so bipolar LSI's have been used in such fields.

In the 1990's modern integrated circuit fabrication technologies began to make BiCMOS a reality. BiCMOS is an evolved semiconductor technology that integrates two formerly separate semiconductor technologies, those of the bipolar junction transistor and CMOS transistor, in single integrated circuit devices. Bipolar junction transistor technology ensures high switching and I/O speed and good noise performance, high gain , low output resistance, which are excellent properties for high-frequency analog amplifiers. On other hand, CMOS technology offers less power dissipation, smaller noise margin, and high packing density, high input resistance. BiCMOS technology used in Pentium, Pentium Pro and SuperSPARC microprocessors.

REVIEW WORK

A brief review of all the following papers has been done and the work of the following authors is as written below. These papers describes about Design of Array Multiplier using CMOS and BiCMOS logics.

G.Rajeshwari, Anjo.C.A,N.Arun Kumar present the paper on design of array multiplier in which they deisgned the multiplier with new logic that is BiCMOS logic. And similarly discussed the latch up problem occurred in CMOS devices and their preventions. The Multiplier designed with the Cadence Simulator that simulates the design using with 180nm technology for BiCMOS. Results shown that a proposed BiCMOS have better performance in terms of delay than the CMOS, as delay for 4*4 multiplier using CMOS logic is 7.888 ns and using BiCMOS logic it is 6.388 ns [1]. Kripa Mathew, S.AshaLatha, T.Ravi, E.Logashanmugam during this paper planned for minimize the transistor count in adder cell for more efficient in terms for area, power and delay. With this less transistor

count in adder cell, the proposed array multiplier performance Increases using 10T compared with the conventional array multiplier using 16T full adder cell. The design is simulated using 32nm and 130nm CMOS technology. For 32nm CMOS technology, the proposed design uses 96 less transistor count and saves 2.82% of total power, 13.24% of more speed and 15.69% less power delay product [2]. N. Ravi, A.Satish, Dr.T.Jayachandra Prasad and Dr.T.SubbaRao worked on the design of Array Multiplier with trade of in power and area for the same. In this paper, the proposed 4x4 multiplier, to add carry bits without using Ripple Carry Adder (RCA) in the final stage. Due to this the multiplier shows 56 less transistor count which cause trade off in power and area. For 180nm technology the proposed multiplier has shown 13.91% less power, 34.09% more speed and 59.91% less energy consumption and to compute the multipliers performance same design is simulated with different technologies [4].

Paul G. Y. Tsui, Bernie Pappert, Shih Wei Sun, and John R. Yeargain have done the analysis of the BiCMOS logic gate configurations for improved low voltage performance. The BiCMOS gate configuration and temperature effect on it is briefly discussed. They proposed the design of BiCMOS gate with PMOS/n-p-n pull-down BiCMOS gate configuration designed for improved low voltage performance. is presented. The measured propagation delay of the BiCMOS speed path is faster than its CMOS counterpart down to 2.3-V supply voltage at -10°C and sub-2 V at 110°C [6]. Mariano Aguirre-Hernandez and Monico Linares-Aranda given the work on design of energy efficient full adders. In this, the proposed full adder and previous various full adders are compared in terms of power, delay and PDP. The proposed full adder is designed with two logic styles that is double pass-transistor logic (DPL), swing restored CPL (SR-CPL). These designs were designed with a 180nm CMOS technology. The simulations is done with Hspice and Nanosim compared against other energy-efficient full-adders for the proposed design simulations gives the power savings up to 80%, and speed improvements up to 25%, for a joint optimization of 85% for the PDP [8]. Raminder Preet Pal Singh, Parveen Kumar, Balwinder Singh planned the work on two different array multiplier by using carry look-ahead adder (CLA) and Carry save adder (CSA). These multipliers are designed for 32-bit unsigned numbers using VHDL language. In this the brief study of carry look-ahead adder (CLA) and carry save adder (CSA) is done. According to the results, implementation of multiplier which uses CSA logic in each partial product lines, due to this Speed improved by 78.3%, Area reduced by 4.2% and power consumption decreased by 1.4% as compare to CLA logic [9].

PROBLEMS ASSOCIATED WITH CMOS LOGIC

The problem of driving large load is traditionally solved by using specific CMOS buffer circuits with enhanced driving capabilities. But most of the buffer configurations require a significant amount of silicon area for improvement in the signal propagation delay. Another serious problem in CMOS is Latch up condition which leads to device failure. Taking advantage of the low static power consumption of CMOS and the high current driving capability of the Bipolar Junction Transistor (BJT) during transients, the BiCMOS configuration can combine the “best of both worlds” [1].

Latch up condition

Latch up is a state in which semiconductor device undergoes a high-current state due to interaction between a PNP and an NPN bipolar transistor. Latch up in CMOS is type of short circuit occur in integrated circuits.When these parasitic pnpn elements undergo a high-current state, latch up can initiate thermal runaway and can lead to destruction of a semiconductor package, chip or system. This condition of CMOS logic is overcome by BiCMOS logic and So using BiCMOS logic we are designing high speed Array multiplier.

ARRAY MULTIPLIER

Multiplier is one of the most important arithmetic unit in Microprocessors and DSPs and also a major source of power dissipation. Reducing the power dissipation of multipliers is a key to satisfy the overall power budget of various digital circuits and systems. With advances in technology, many designers trying to make design efficient in terms of high speed, low power consumption, regularity of layout and less area .

Conventional multiplier

The common multiplication method is “add and shift” algorithm. In parallel multipliers number of partial products to be added is the main parameter that determines the performance of the multiplier.

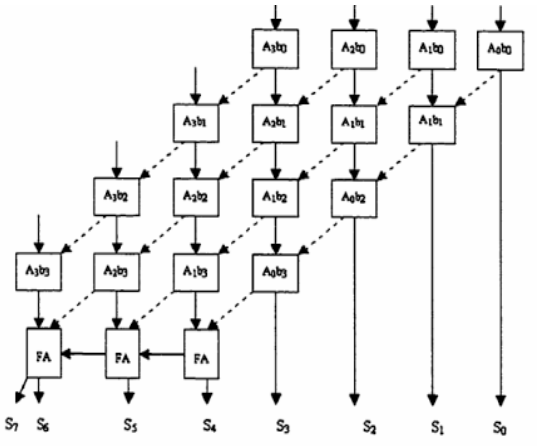

*Fig.1. m*n Array Multiplier*

Booth's Multiplier

Booth's multiplier work on Booth's Multiplication Algorithm. The conventional multiplier multiplies the unsigned numbers and for multiplication of two signed numbers booth's multiplier in 2's complement representation is used. Booth's algorithm is faster than add and shift method i.e. conventional multipliers.

Wallace Tree Multiplier

Several popular and well-known schemes, with the objective of improving the speed of the parallel multiplier, have been developed in past. Wallace introduced a very important iterative realization of parallel multiplier. In Wallace tree architecture, all the bits of all of the partial products in each column are added together by a set of counters in parallel without propagating any carries.

Types of Adders

The most important component in the architecture of multiplier is adder. There are various types of adder such as Carry look-ahead adder, carry save adder, carry select adder, ripple carry adder, carry skip adder etc.

Carry Look Ahead Adder (CLAA)

Carry look-ahead adder will take the less time for carry computation. Look ahead carry algorithm speed up the operation to perform addition, because in this algorithm carry for the next stages is calculated in advance based on input signals [9].

Carry Select Adder (CSLA)

Carry select adder will uses the ripple carry adders, the carry generated through each section determines the carry in of the next section. The carry out will be selected and these carriers are propagated through multiplexers.

Carry Save Adder (CSA)

Carry save adder tries to add many n-bit numbers these adders are similar to the basic full adder. If the first row of the partial products is implemented with Full-Adders, Cin will be considered '0'. Then the carries of each Full- Adder can be diagonally forwarded to the next row of the adder [4].

Ripple Carry Adder (RCA)

Ripple carry adder is built when the full adders are cascading in series for n -bit numbers.

An m × n array multiplier uses on m × n AND gates can compute all the terms AiBi simultaneously. The terms are summed by an array of 'n' half adders, 'n×[m -2]' full adders. (total ' (m-1)×n' adders). Delay due to AND's in partial product at every level is equal to one unit AND gate delay. Calculation of delay at level 1 to (n-1) unit of m-bit adders is given by (n-1) × delay of one unit m-bit adders.

PROPOSED WORK

BICMOS logic exhibit better characteristics when we consider large load. So, BICMOS can be used where high speed is the prime aim. BiCMOS logic has advantages such as large load drive capabilities, low static power dissipation, fast switching and high input impedance. Here, using this BiCMOS technology we are going to design high speed array multiplier and the power of this multiplier is compared with array multiplier designed by CMOS logic. And will work on optimization of power for proposed multiplier. The result will be compared with previous work. This proposed array multiplier is designed and simulated with TANNER Tool.

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