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High performance of cubic $Al_xGa_{1-x}N$/GaN Double Gate MOS-HEMTs

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Abstract – ***In this paper, we have compared the performance of cubic $Al_xGa_{1-x}N$/GaN and InP/$In_yGa_{1-y}As$ DG MOS-HEMTs, by analyzing the impact of gate length (L_G) using 2D nextnano³ software. Drift-diffusion model was taken for simulating the proposed device. The gate length was varied from (12 to 18) nm in a step of 3 nm. As gate length is reduced for scaling, higher drain current is observed, again as Indium content y of channel layer $In_yGa_{1-y}As$ is increased, there is an increase in drain current density, while threshold voltage is decrease comparable to InP/$In_yGa_{1-y}As$ DG MOS-HEMT. Except drain current density and threshold voltage all other parameters are acceptable, a needful to improve the two parameters. However, the proposed model of cubic $Al_xGa_{1-x}N$/GaN DG MOS-HEMT is the ultimate to replace InP/$In_yGa_{1-y}As$ DG MOS-HEMT and MOSFET for next-generation microwave and power switching application fields in the future.***

Keywords: *cubic $Al_xGa_{1-x}N$/GaN, InP/$In_yGa_{1-y}As$, device simulation, DG MOSFET, DG MOS-HEMT, next**nano³**.*

1. INTRODUCTION

For switching devices and digital electronics field-effect transistors (FETs) with normally-off characteristics are desirable. Therefore, cubic $Al_xGa_{1-x}N$/GaN without undesirable parasitic piezoelectric and spontaneous polarization fields and with equal electrical properties for all gate orientations [1] and has a significant transport advantages, and is being used extensively in research as channel materials for upcoming highly scaly devices [2]. Further the cubic nitrides would allow using the same technology for normally-on and normally-off devices [1]. But, majority of III-V materials have considerably smaller band gap as compared to silicon, leading to excessive band-to-band tunneling leakage currents, which eventually limits their scalability beyond 22 nm technology node gate length (L_G) [3]. In HEMT devices, the gate leakage current and buffer leakage are important factors limiting its performance and reliability. Therefore, the use of a gate oxide helps to improve gate contact forming a MOS-HEMT, reduce the gate leakage and increase drain current, however, it partly reduces the transconductance because of a larger gate-to-channel separation [4].

In this work, we have analyzed the impact of the gate length on devices performance of InP/$In_yGa_{1-y}As$ and cubic $Al_xGa_{1-x}N$/GaN nanostructures based DG MOS-HEMT devices. Key devices performance such as drain current density and threshold voltage. Following by the description of the device structures in Section 2, we will discuss the devices simulation results and comparison study of a symmetrical underlap DG MOSFET devices, cubic $Al_xGa_{1-x}N$/GaN and InP/$In_yGa_{1-y}As$ nanostructures based DG MOS-HEMTs switching devices using next**nano³** software [5]. Moreover, to validate our simulation results of proposed models we have compared with both results which were obtained by H. Pardeshi et al [6] and obtained by F. Djeffal et al [7].

2. DEVICE SIMULATION RESULTS

In this work, we have simulated the I-V characteristics of three different device structures such as: silicon symmetrical underlap DG MOSFET, cubic $Al_xGa_{1-x}N$/GaN and InP/$In_yGa_{1-y}As$ DG MOS-HEMT. However, we have analyzed the impact of LG on performance gate based cubic $Al_xGa_{1-x}N$/GaN DG MOS-HEMT using 2D next**nano³** software.

2.1 Device description structures

The simulated of a symmetrical underlap DG MOSFET and III-V heterostructures devices have the same geometry and doping concentrations, but different channel materials and gate lengths. We have considered three structures: the first structure consists of a symmetrical underlap DG MOSFET used in our simulation is shown in Fig.1, where L_G = 10 nm is the gate length, L_{un} = 5 nm is the underlap symmetrical lengths on both the source and drain sides, $t_{bd} = t_{Si}$= 3 nm is the undoped ultrathin body (UTB) thickness and t_{Ox} = 1 nm is the gate oxide thickness.

The second structure consists of the cubic $Al_xGa_{1-x}N$/GaN DG MOS-HEMT is shown in Fig.2, where the gate length L_G variable from (12 to 18) nm, in steps of 3 nm and Al content x in the barrier layer $Al_xGa_{1-x}N$ (x = 30 %), with ultrathin t_{bd} = 6 nm. The body consists of cubic GaN channel t_{Ch} and $Al_xGa_{1-x}N$ barrier tb, where tbd = t_{Ch} + 2.tb. For analyzing the influence of L_G, t_{Ch} is kept constant at 2 nm and t_b = 2 nm. The source/drain lengths are kept fixed L_{un} = 5 nm, the upper and lower gate oxide thickness t_{Ox} = 1.2 nm with SiO_2 dielectric to minimize the gate leakage. The source and drain regions are also assumed to be heavily doped with n-type doping concentration N_D = 10^{20} cm-3 and uses abrupt doping profile at source/drain ends.

Furthermore, we have assumed also a symmetric underlap from source-to-gate and gate-to-drain sides. While the third structure consists of InP/$In_yGa_{1-y}As$ DG MOS-HEMT devices is shown in Fig.3, where Indium content y in the channel layer $In_yGa_{1-y}As$ is variable (53 % and 75 %), the gate length L_G = 18 nm, and tbd = 6 nm is the ultrathin body thickness. The body consists of t_{Ch} is the $In_yGa_{1-y}As$ channel and tb is the InP barrier thickness, where tbd = t_{Ch} + 2.tb are assumed in this work. For analyzing the impact of Indium content y, keeping barrier and channel thickness constant (t_b = 2 nm and t_{Ch} = 2 nm).

Moreover, the device channel consists of III-V heterostructure consisting of narrow band $In_yGa_{1-y}As$ t_{Ch} layer and two layers of wide band InP (t_b). $In_yGa_{1-y}As$ has high electron mobility and is lattice matched InP [7]. While, the channel of second device consists of narrow band cubic GaN (t_{Ch}) layer and two layers of wide band cubic $Al_xGa_{1-x}N$ (t_b). Cubic GaN has high electron mobility and is lattice matched cubic $Al_xGa_{1-x}N$. A narrow band gap cubic GaN layer is sandwiched between the two wide band gap cubic $Al_xGa_{1-x}N$ barrier layers and the channel is confined at the heterostructure interfaces. The barrier layer used has the conduction band edge offset with the channel and is nearly the lattice matched with the narrow band layer to minimize the traps at its interface with the channel [8].

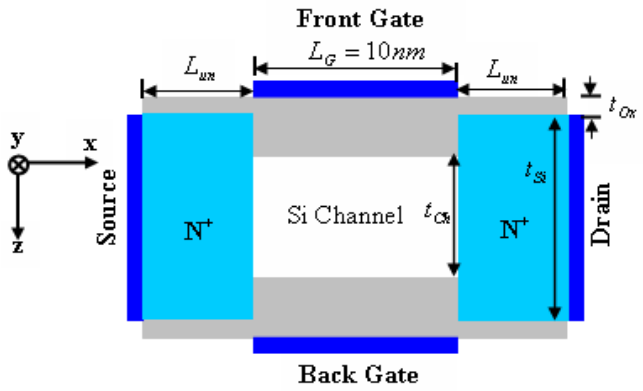

Fig. 1: Schematic structure of a symmetrical underlap DG MOSFET.

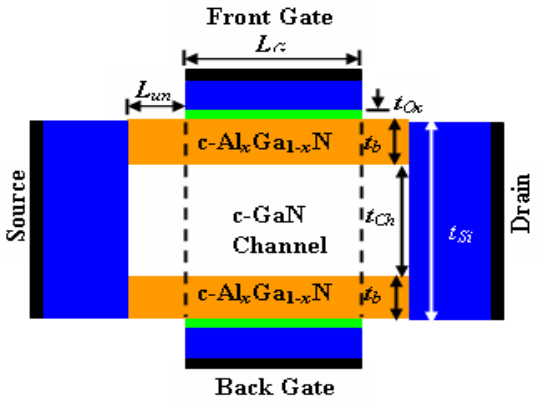

Fig. 2: Schematic structure of cubic $Al_xGa_{1-x}N$/GaN nanostructures based DG MOS-HEMT.

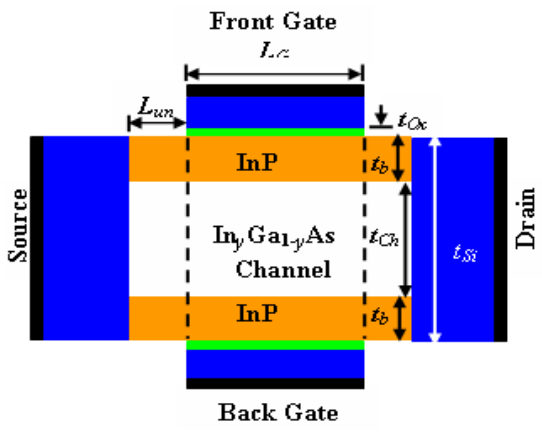

Fig. 3: Schematic structure of InP/$In_yGa_{1-y}As$ nanostructures based DG MOS-HEMT.

2.2 Results and discussion

The density gradient model used in the numerical simulation, solves the quantum potential equations self consistently with the Poisson's equation and carrier continuity equations. The quantum potential is introduced to include quantization effects in a classical devices simulation. Density gradient transport model is used mainly in simulating nanoscale devices, such as single gate MOSFETs, and DG MOSFETs, FinFETs and underlap structures. A quantization effect is used to analyze the carrier transport in the interface between the two dissimilar band-gap semiconductor materials [8].

Moreover, the two-dimensional drift-diffusion model numerical simulation has been carried out using 2D nextnano3 software. This model of drift-diffusion uses to solve the Poisson's equation self-consistently with carrier continuity equation. We have assumed the mobility-model-simba-2 [5], if the exponents kappan,p ($k_{n,p}$) are temperature dependent then this equation is called Canali model (with $\mu_{n,p}$ as the low field mobility) with suitable modifications to precisely capture the non-equilibrium carrier transport [9] with suitable modifications to precisely capture the non-equilibrium carrier transport.

$$\mu^{p,n}\left(\vec{E}\right)=\frac{\mu^{p,n}}{\left[1+\left(\mu^{p,n}\frac{\left|\vec{E}\right|}{v_0^{p,n}}\right)^{\kappa^{p,n}}\right]^{1/\kappa^{p,n}}} \qquad (1)$$

- **Simulation at different voltages**

Fig.4 shows the electrical output characteristics of a symmetrical underlap DG MOSFET are calculated using 2D nextnano3 at gate voltage VG is varied from 0.05 V to 0.5 V with a step of 0.05 V and at room temperature. For low drain bias the linear drive current is directly proportional to the conductivity and for high drain bias the saturated drive current is proportional to the carrier density. In order to validate the simulation results and calibration of our proposed model parameters we have compared with the results obtained by F. Djeffal et al [7].

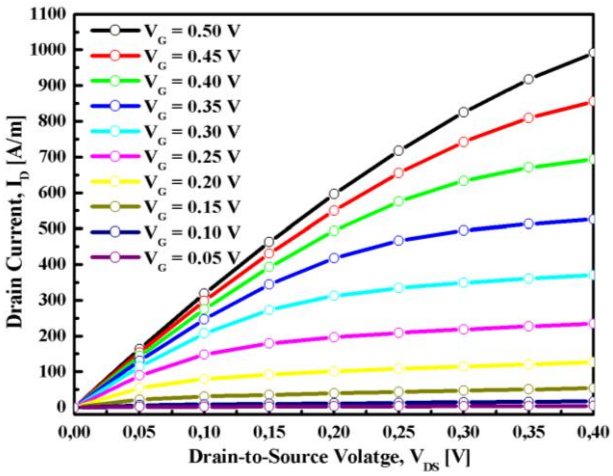

Fig. 4: The output characteristics of a symmetrical underlap DG MOSFET are calculated using next**nano³** at different gate voltages where L_G = 10 nm, t_{Si} = 3 nm and t_{Ox} = 1 nm.

The I_D-V_{GS} transfer characteristics of a symmetrical underlap DG MOSFET at different drain voltages V_D are shown in Fig.5 are calculated using 2D next**nano³**. By varying of the gate-to-source potential, the current increases due to increase of carrier density i.e. 2DEG in channel. For validating the simulation results and calibration of the model parameters are compared with numerical simulation results and experimental values [10].

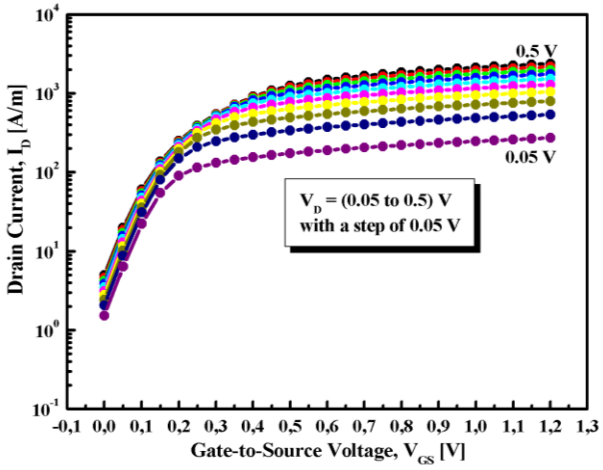

Fig. 5: I_D-V_{GS} transfer characteristics of a symmetrical underlap DG MOSFET are calculated using next**nano³** at different drain voltages where L_G = 10 nm, t_{Si} = 3 nm and t_{Ox} = 1 nm.

- **Variation in gate length of cubic $Al_xGa_{1-x}N$/GaN DG MOS-HEMT**

The I_D-V_{GS} transfer characteristics of cubic $Al_xGa_{1-x}N$/GaN DG MOS-HEMT at V_D = 0.05 V and 0.5 V are shown in Fig.6. With varying of the gate-to-source potential, the current increases due to increase of carrier density i.e. 2DEG in channel.

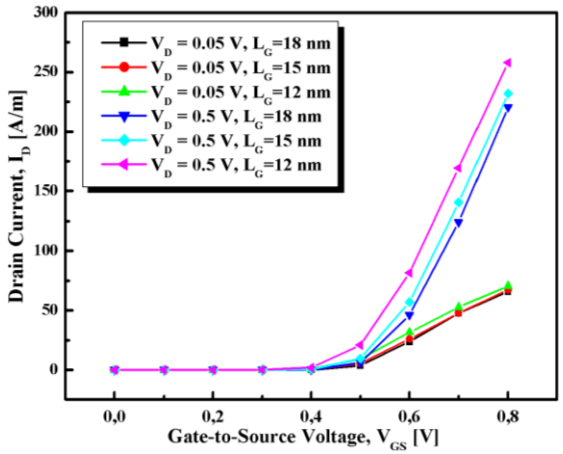

Fig. 6: ID-VGS transfer characteristics of cubic $Al_{0.3}Ga_{0.7}N$/GaN DG MOS-HEMT at V_D = 0.05 V and 0.5 V and for L_G-dependent at room temperature using next**nano³**.

The gate length is varied from (12 to 18) nm in a step of 3 nm, keeping barrier and channel thickness constant (barrier thickness, t_b = 2 nm and channel thickness, t_{Ch} = 2 nm). Reduction of current was observed as gate length increases because of increase of channel resistance. The peak value of drain current obtained 257.84 A/m at L_G = 12 nm, t_b = 2 nm, and V_D = 0.5 V.

- **Variation in Indium content y within the $In_yGa_{1-y}As$ channel layer**

Fig.7 shows the current-voltage characteristics of InP/$In_yGa_{1-y}As$ DG MOS-HEMT at different Indium content y in the $In_yGa_{1-y}As$ channel layer. Our simulation results are showed that at y = 75 % , InP/$In_yGa_{1-y}As$ DG MOS-HEMT reaches the peak value of drain current obtained is 91.05 A/m at L_G = 18 nm, t_b = 2 nm, and V_D = 0.5 V using drift diffusion model.

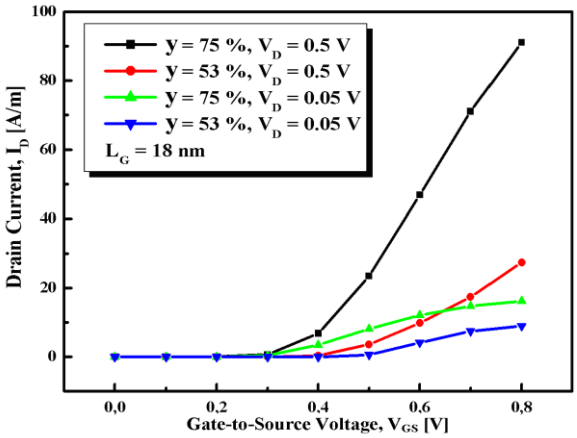

Fig. 7: I_D-V_{GS} characteristics of InP/$In_yGa_{1-y}As$ DG MOS-HEMT where t_{bd} = 6 nm and L_{un}= 5 nm. The applied drain voltage is V_D = 0.05 V and $_{VD}$ = 0.5 V at different Indium content y.

- **Comparative study on I-V characteristics of cubic $Al_xGa_{1-x}N$/GaN and InP/$In_yGa_{1-y}As$ DG MOS-HEMTs**

Fig.8 shows simulated current-voltage characteristics of both devices, by varying the gate-to-source potential, the drain current increases due to increase of carrier density. Keeping gate and underlap lengths constant (gate length, L_G = 12 nm and underlap length, L_{un} = 5 nm). We could be obtained excellent characteristics clearly depicting higher drain level for cubic $Al_{0.3}Ga_{0.7}N$/GaN DG MOS-HEMT devices, arising from high mobility and conductivity than InP/$In_{0.75}Ga_{0.25}As$ DG MOS-HEMT devices. We have observed a good drain

current saturation arising from considerably lower, with double gate providing much better channel control [11]. High mobility and conductivity leads to higher drive current at both (low and high) drain biases, which have great significance for high speed logic applications. For low drain bias the linear drive current is directly proportional to the conductivity and for high drain bias the saturated drive current is proportional to the carrier density, as well as the carrier injection velocity. The carrier injection velocity in turn depends on the low field carrier mobility and effective mass m* [12].

The transfer characteristics of both devices are compared in Fig.9 at V_D = 0.5 V by varying the gate-to-source potential current. The gate length is varied from (12 to 18) nm in a step of 3 nm, keeping barrier and channel thickness constant (t_b = t_{Ch} = 2 nm). As devices are scaled for enhancing the performance, short channel effects start to dominate.

The current-voltage characteristics of the DG MOS-HEMTs are analyzed. Thus exploitation of high mobility/wide band gap characteristics can be done using new structure of devices, such as cubic $Al_xGa_{1-x}N$/GaN DG MOS-HEMT. Furthermore, with high-κ dielectric provides higher ON-current.

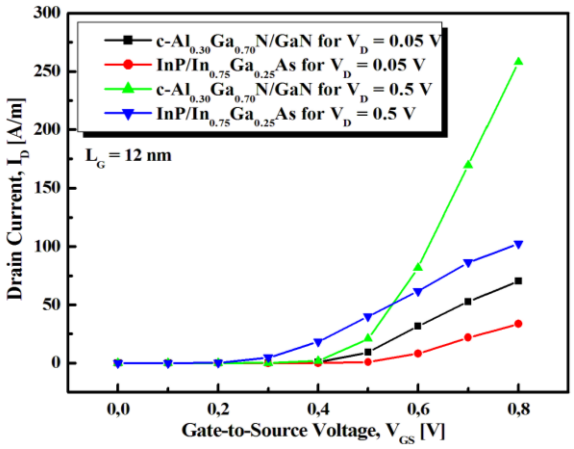

Fig. 8: I_D versus V_{GS} characteristics of both devices, where L_G = 12 nm, t_{bd} = 6 nm, and L_{un} = 5 nm are kept fixed constants. The applied drain voltage is V_D = 0.05 V and V_D = 0.5 V for both devices.

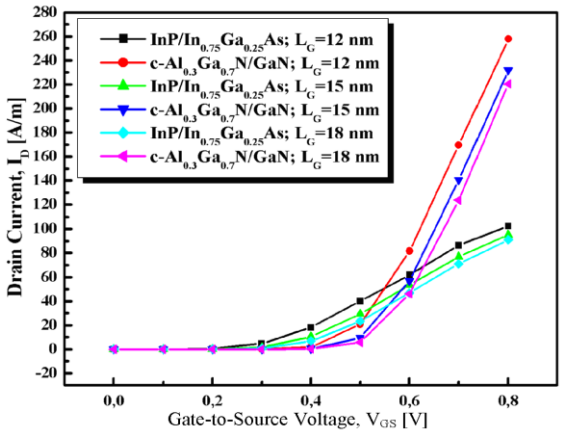

Fig. 9: I_D versus V_G characteristics of both devices where applied drain voltage is V_D = 0.5 V, t_{bd} = 6 nm, L_{un} = 5 nm, and gate length L_G is varied from (12 to 18) nm with a steps of 3 nm for both devices.

On the other hand, the simulation results of the device characteristics of cubic $Al_xGa_{1-x}N$/GaN DG MOS-HEMT are compared with InP/$In_yGa_{1-y}As$ DG MOS-HEMT for various gate lengths at drain bias of 0.5 V. The maximum source-to-drain current of these devices is in the order of some hundred A/m. Therefore InP/$In_yGa_{1-y}As$ based DG MOS-HEMT is applicable for high speed applications can be viewed as replacement of MOSFET compared to cubic $Al_xGa_{1-x}N$/GaN DG MOS-HEMT is applicable for ultrahigh-speed logic amplifications, high power switching, and high temperature application fields. Thereby, the drain current of cubic $Al_xGa_{1-x}N$/GaN DG MOS-HEMT is a factor 40% higher than the same current of InP/$In_yGa_{1-y}As$ based DG MOS-HEMT at V_{GS} = 0.8 V and L_G = 12 nm.

3. CONCLUSION AND OUTLOOK

Our simulation results indicate that, the cubic $Al_xGa_{1-x}N$/GaN DG MOS-HEMT provide higher ON-current at L_G = 12 nm and V_D = 0.5 V compared with InP/$In_{0.75}Ga_{0.25}As$ is lower which is acceptable for the devices performance, needful improvements are required. However, ultra-short cubic $Al_xGa_{1-x}N$/GaN MOS-HEMTs need DG structures to overcome the weakness of short channel effect caused by their narrow band gap and small electron effective mass. From the futuristic point of view, our simulation results showed that the device designs of cubic $Al_xGa_{1-x}N$/GaN DG MOS-HEMT could be proposed as replacement of InP/$In_yGa_{1-y}As$ DG MOS-HEMT and MOSFET in the future. We therefore clearly establish the potential of using cubic $Al_xGa_{1-x}N$/GaN DG MOS-HEMT is

useful for ultrahigh-speed logic amplifications of next-generation, high power switching, and high temperature application fields. Double Gate technologies with proper design parameters are attractive for counteracts the effect of carrier injection into the device buffer (since no buffer is used in the device structures).

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BIOGRAPHIES

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