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WEIGHTED RANDOM PATTERN GENERATOR OF BIST

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Abstract - ***In Built-In Self-Test (BIST), test patterns are generated and applied to the circuit-under-test (CUT) by on-chip hardware; minimizing hardware overhead is a major concern of BIST implementation. In pseudorandom BIST architectures, the test patterns are generated in random nature by Linear Feedback Shift Registers(LFSR). A System-on-Chip (SOC) is the integration of all components of an electronic/computing system on a single integrated circuit. This paper presents a novel test pattern generation technique called BIST,As the complexity grows, testing is becoming one of the most significant factors that contribute to the final product cost. The established low-level methods for hardware testing are not any more sufficient and more work has to be done at abstraction levels higher than the classical gate and register-transfer levels. This paper deals with testing and design for testability of modern digital systems. This process is performed BY Pseudo-random testing is an attractive approach for BIST. A linear feedback shift register (LFSR) can be used to apply pseudo-random patterns to the CUT.***

Key Words: *ATPG-Automatic Test Pattern Generation, BIST-Built In Self-Test, CUT -Circuit Under Test, LFSR – Linear Feedback Shift Register, MISR(Multiple Input Signature Register.*

1. INTRODUCTION

A System-on-Chip (SOC) increasing capacity of system integration in modern semi-conductor processes, reduced time-to-market requirements, and decreasing system costs make multi core systems and SOC implementations as new design paradigms in integrated circuit design. A typical SOC includes components such as volatile memory systems, non-volatile memory systems, digital signal processers, microprocessors, mixed signal circuits, logic circuits and buses. Testing is checking the quality, performance, reliability and functionality of the system before actually using it.

1.1 Testing Of Core

Testing is checking the quality, performance, reliability and functionality of the system before actually using it. Once the designed circuit is manufactured, the circuit needs to be tested to check if it is functioning properly and if it meets the specifications. Test vectors are used to ensure the circuit functions properly. Because of the test vector, the circuit is relied upon to deliver an arrangement of results. Testing of SOCs is turning out to be extremely mind boggling because of the set number of inputs and many-sided quality of equipment. This has significant implications on the design and test of these devices. Low-power requirements affect test in two separate ways. First, it’s important to ensure that any functional power constraints are met (or at least adequately managed) during test execution. Second, it’s necessary to ensure that a test solution is compatible with whatever low-power design techniques are being used.

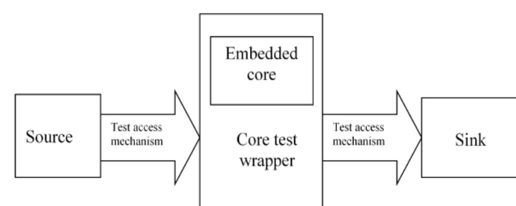


Fig.1.1 Testing of Embedded System

1.2 Pseudo-Random BIST

The primary necessity has by and large meant guaranteeing circuit exchanging action levels are kept up beneath a practically characterized edge amid sweep test design application. This is refined by producing the sweep test designs so as to control the quantity of 1 to 0 and 0 to 1 moves inside of every example. The move recurrence compares straightforwardly to circuit switch action and consequently to normal force. Each PRPG output produces a stream of pseudo-random bits. These bit streams are fed [into a phase shifter to produce a much larger number of pseudo-random bit streams to feed each of the individual scan chains within the circuit under test. To reduce the inherent toggle rate of each bit stream, a holding register is placed between each PRPG output and the phase shifter.

A low-power LBIST module individually controls each of these holding registers.

2. LITERATURE REWIEW

There are limits on the test length, which is the number of pseudo-random patterns that can be applied during BIST. One limit is simply the amount of time that is required to apply the patterns. Another limit is the fault simulation time required to determine the fault coverage. A third limit is heat dissipation for an unpackaged die. Thus, in order for pseudo-random pattern testing to be effective, high fault coverage must be obtained for an "acceptable" test length. What is considered acceptable depends on the particular test environment. This paper presents architecture of a low power pseudo random test pattern generator with programmable features that allow selection of wide range of user-defined toggling rates. An *n*-bit PRPG connected with a phase shifter feeding scan chains forms a kernel of the generator producing the actual pseudorandom test pattern. Today's designers using Design Automation (DA) with the latest semiconductor technology are accelerating this rate of integration even more. This combination of increased functionality with the faster, denser, and smaller packaging brings up a dilemma: it is becoming more difficult to access, test, and verify chip and system functionality using traditional external equipment and instruments.

3. PROPOSED DESIGN

A full toggle pattern may consume more power at every pattern it generated and trends to rise in power dissipation. Apart from these high switching activity can result in failure of chips functionality during test phase. Though the result show improvement in reducing power consumption but the test pattern generated are repeated since there is knowledge of the chains. In the author presents bit swapping in LFSR which reduce power consumption and cost of testing. But during swapping the problems comes when the n is even the swap chain resets to zero and start again. In the testing Power-Aware At-Speed Scan Test Methodology for Circuits with Synchronous Clocks is presented with modifying the previous works .A low transition in LFSR to reduce the power consumption is presented in by minimizing the test patterns which increases the cost of testing.

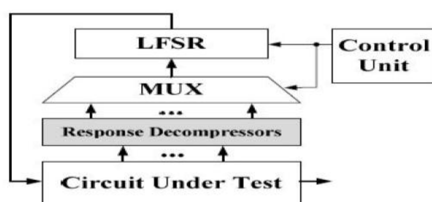


Fig.3.1 Response Analyser

In Implementation, Before describing the principles of the state-of-the art methods, namely the Reseeding, Weighted pattern testing, Bit-fixing, Bit-flipping and Row-marching methods, the basic BIST methods will be introduced, for better understanding to the latter ones.

1. Exhaustive Testing

2. Pseudo-Random Testing

3. Reseeding-Based Techniques
4. Weighted Pattern BIST:

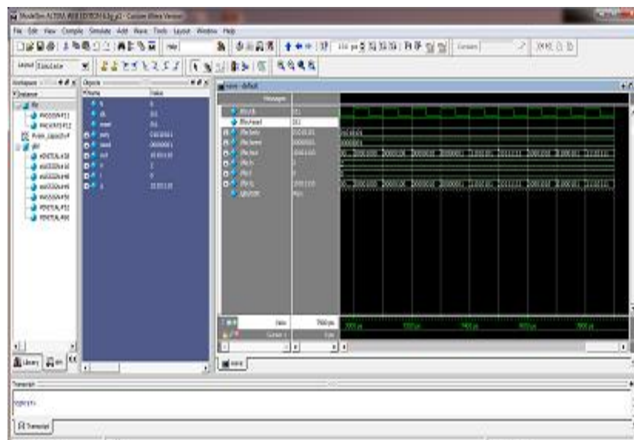
To one of the approaches, where the pseudo-random patterns are modified so that better fault coverage is reached, belongs the weighted pattern testing. Here the PRPG patterns are being biased by a signal probability of some of the PRPG outputs (the probability of a "1" value occurrence). In the weighted pattern testing method two problems have to be solved: first, the weight sets have to be computed and then the weighted signals have to be generated. Many weight set computation methods were proposed and it was shown that multiple weight sets are needed to produce patterns with sufficient fault coverage [Wun88]. These multiple weight sets have to be stored on a chip and also the logic accomplishing switching between them is complicated, thus this method often implies a large area overhead. Several techniques reducing the area overhead of a weighted pattern testing BIST were proposed -The area overhead is reduced, however it is restricted to one weight set only.

The row matching approach is based on a similar idea. A simple combinational function transforming some of the PRPG patterns into test patterns is designed in order to reach better fault coverage. Here the test patterns are independent on the PRPG code words in a sense of a similarity of the patterns – proper test vectors are pre-computed by an ATPG tool; they are not derived from the original PRPG code words as it was being done in the previous methods. The row matching comprises of finding an assignment of deterministic test patterns to the PRPG code words, Each of the test patterns has to be assigned to some PRPG pattern to generate the required test. Here the problem to be solved consists in finding such a row matching that the pattern transformation function is as simple as possible. The aim of the algorithm is to find a row matching that minimizes the cost function, which is a rough measure of the complexity of the final BIST design. This is, unfortunately, an NP-hard problem and thus some heuristic must be used. In the proposed algorithm the rows are being matched sequentially (one-by-one) preferring the match that locally minimizes the cost function. After the matching is done, the result is in a form of a truth table, which has to be minimized by some Boolean Minimizer (ESPRESSO) to obtain the final solution.

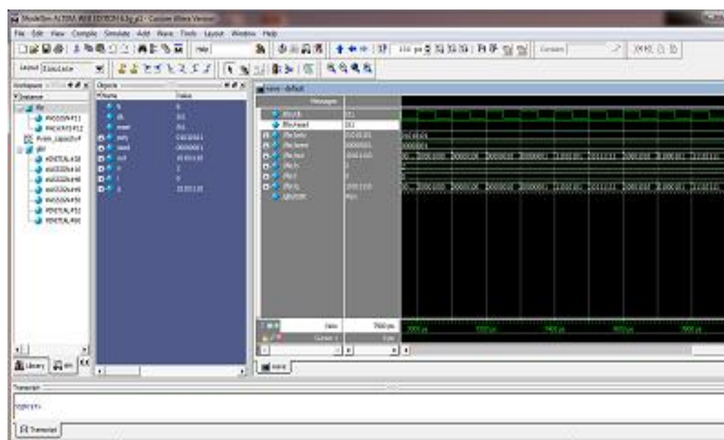
3. RESULT

A Bench Mark Combinational Circuit C17.bench was used for testing the algorithm.The proposed method significantly reduces the power consumption during testing mode with minimum number of switching activities using conventional LFSR in the circuit used for test pattern generator. From the implementation results, it is verified that the proposed method gives better power reduction compared to the exiting method.

4. Simulation Result



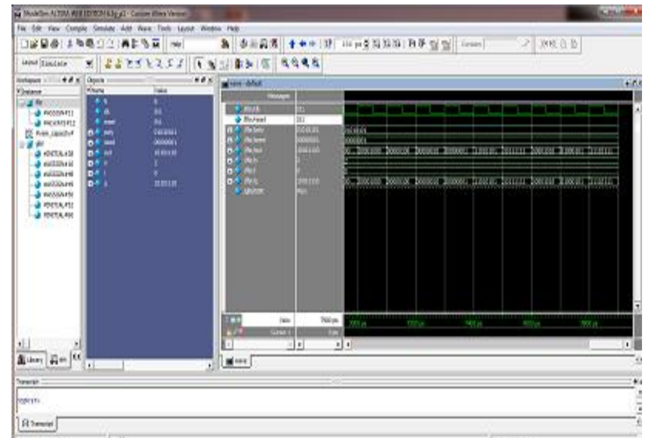
Simulation of LFSR



Simulation of LFSR parallel

The output file from ATALANTA is parsed and SET - F_n = **{**TF_{n1}, TF_{n2}, ...TF_{nm}} is generated, each subset TF_{nm} consists of test vectors {TV_1,TV_4,....TV_n} which could identify individual faults F_n. From the set F_n a SET - TF_nU = {TV_1, TV_2,TV_3……. TV_n} is generated which is the intersection subsets present in F_n, this is a set of unique vectors without repetitions. Now for each vector present in set TF_nU the set of faults detected by it is obtained. Ie. A SET - TVF_n = {TVF_{n1}, TVF_{n2}, ...TVF_{nm}} is generated where each subset TVF_{nm} = {f_n ....} contains the set of faults detected by the vector TV_n that corresponds to TVF_{nm}. Find the maximum of the set TVF_n, R = MAXIMUM (TVF_n). The test Wei-Cheng Lien; Tong-Yu Hsieh; Kuen-Jong Lee, "Routing-

Paschalis, Antonis, Ioannis Voyiatzis, and Dimitris Gizopoulos. "Accumulator based 3-weight pattern generation." Very Large Scale Integration (VLSI)



4. CONCLUSIONS

In this paper, the Dissertation is aim of to propose a flexible way how to design test pattern generators (TPGs) meeting any of the above-mentioned restrictions (or, better, quality measures). The designer should be able to freely adjust the BIST equipment design runtime, BISTE area overhead and BIST run time, according his preferences. In this we proposed a low power test pattern generation method that could consumes more density. It also developed a theory to express a sequence generated by linear sequential architectures, and extracted a class of SOC sequences named MSIR. Thus the proposed method significantly reduces the power consumption during testing mode with minimum number of switching activities using conventional LFSR in the circuit used for test pattern generator. This paper presents a low hardware overhead TPG for scan based BIST that can reduce switching activity in cuts during BIST and also achieve very high fault coverage with a reasonable length of test sequence. The main objective of most recent BIST techniques has been the design of TPGs that achieve high fault coverage at acceptable test lengths for such circuits. While this objective which is reducing heat.

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