International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 02 Issue: 09 | Dec-2015 www.irjet.net p-ISSN: 2395-0072

PHASE LOCKED LOOP (PLL) DESIGN IN FM RECEIVER CHIP

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Abstract: ***The existing technologies are based on software defined radio (SDR) and the demand needs programmable SDR instead of analog SDR. In SDR, Programmable digital devices are used and they transmit and receive the baseband signal at radio frequency. The research paper focuses on the design of the different components of PLL such as phase detector, Loop filter, VCO, ADC and DAC using VHDL Programming language. The integrated chip of these components is called digital PLL, can be utilized in FM demodulator. In the paper the design of programmable FM demodulator is developed in Xilinx 14.2 ISE software and functionally checked in Model Sim 10.1 b software.***

Key Words: *Frequency Modulation (FM), Wireless local area network (WLAN), Field programmable gate array (FPGA), Voltage Controlled Oscillator (VCO)*

1. Introduction

Phase Locked Loops (PLL) is a closed loop system that locks two signals in such a way that exist with same frequency and constant phase (zero) difference between them. The system compares the frequencies of an input waveform to that of the output of PLL and then adjusts the frequency of output such that they are totally synchronized with each other. PLL consist of three parts: a phase detector, loop filter and a voltage controlled oscillator (VCO). The VCO helps in changing the output frequency and provides frequency equal to the frequency of incoming signal. PLL locks two signals in such a way that they are synchronized with each other. The incoming signal in the reference or input signal is the frequency that is to be adjusted so that it can match the reference signal and feed to VCO. PLL is used in clock generation in system on chip (processors).PLLs can accurately generate a desired frequency. In a communication system there are three modulation techniques, Amplitude Modulation (AM), Frequency Modulation (FM) and Phase Modulation (PM). In the old system all transmissions were analog so the traditional PLL are based on analog block. Analog PLL have noise and gives varied output. Digital PLL are based on digital clock signal and lock the signal with faster lock time such as in high speed microprocessor. This is the need of rapid change of the technology existing for our handset and base station used in 3G mobile system. PLL is a technique used to design a FM demodulator. In the PLL operation can be understood with the help of the diagram as shown in Figure 1. The use of phase generator is to produce an error signal with the help of the input signal and the reference signal. The phase comparator is a multiplier of two signal inputs FM modulated signal and reference signal. Therefore additional signal is generated so there is a need of digital filter. The reference signal is generated using a numerically controlled oscillator (NCO) where oscillator is noticed by that of error signal. Recent advancement in the chip technology is integrating several sequential elements in System on Chip (SoC). But most of the circuits are using traditional clock distribution networks and facing the problem of skew and jitter problems. The clock signal generated by the oscillators and the flip-flops and registers are not receiving the clock pulse at the accurate time. The problem can be solved using Network of Phase-Locked Loop (PLL) oscillators coupled in phase. A phase locked loop ensures that the clock frequencies seen at the clock inputs of various registers and flip-flops match the frequency generated by the oscillator. The popular technique to demodulate FM signal is Phase Locked Loop (PLL). The design approach is based on digital components rather than analog components such as phase detector, loop filter and Voltage Controlled Oscillator (VCO). The signal is presented using digital words instead of analog voltages. In digital FM receiver, PLL is the main part to capture and lock the signals at different frequency and phase. The main purpose of PLL is to maintain the coherence between the modulated signal frequency (f_i) and the respective frequency (f_o), with the concept of phase comparison. PLL permits to track the frequency changes of applied input signals, as it is locked once.

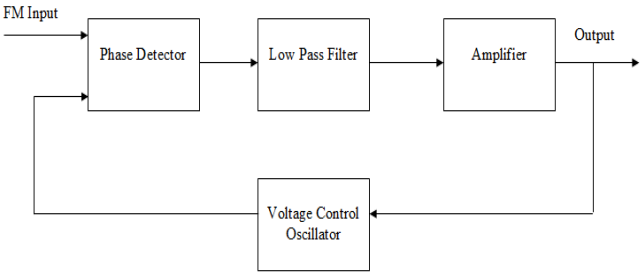

Fig 1: PLL Components

The recent cellular devices follow the communication protocol and provide connectivity to end user anywhere in the particular region. The technologies which are using software and can process the data in real time use base on field programmable gate array (FPGA) or digital signal processors (DSP). Frequency modulation/demodulation is

widely used schemes applied on mobile and fm devices. Audio and voice signal clarity is the main issue in mobiles. In a FM modulated/demodulated signal it is very difficult to achieve the good quality voice and clarity because VCO circuits are lagging to provide desired frequency that is why there is a use of programmable chip implementation of FM modulation system. The cellular industries always need such scalable hardware chip which can support wireless local area network (WLAN) technologies, Bluetooth, global positioning system (GPS) receiver, camera, MPEG videos etc. these applications need high level of memory integration with transmitter-receiver integration.

2. PLL in FM

Phase Locked Loop (PLL) is the main part of FM demodulator. The PLL consist of three parts (i) Phase Detector (ii) Loop Filter (iii) Numerically Controlled Oscillator (NCO).The functional diagram of PLL is shown in Figure 2. The function of the phase detector is to produce an error signal based on the difference in phase value between the input signal and the reference signal. The phase detector is a multiplier circuit and producing additional signal. The output of multiplier is needed to filter with the help of a digital filter. The function of NCO is to generate a reference signal is calculated by the error signal.

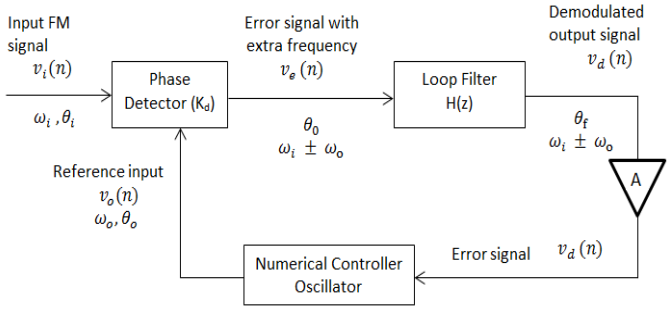

Fig 2: PLL Block diagram

PLL is most common component used in the System on Chip (SoC) processors and used to provide clock pulse. PLL is used to provide a desired frequency for high precision crystal reference. The Frequency Synthesizer has the parameters switching speed, frequency resolution, frequency range, power and jitter consumption.

3. Results

The Register Transfer Level (RTL) view of the developed chip of FM demolator is shown in Fig.3 and function simulation in Modelsim foftware is shown in Fig. 4. The simulations is carried for the data by the chip. The simulation is carried at a frequency 95.00 MHz and 195 MHz and received at the ending side or by the receiver.

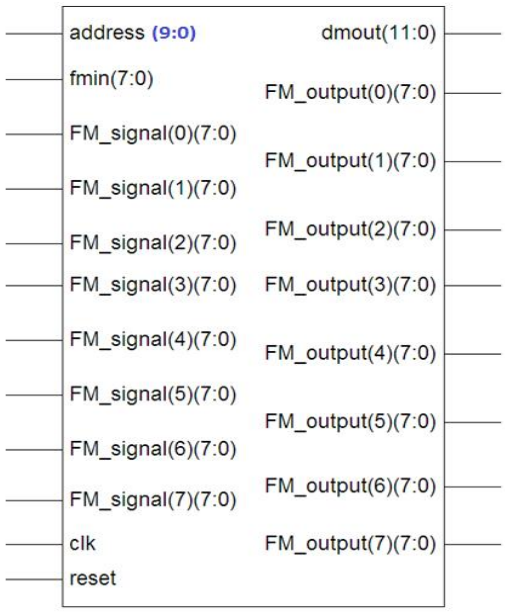

Fig 3: RTL view of PPL

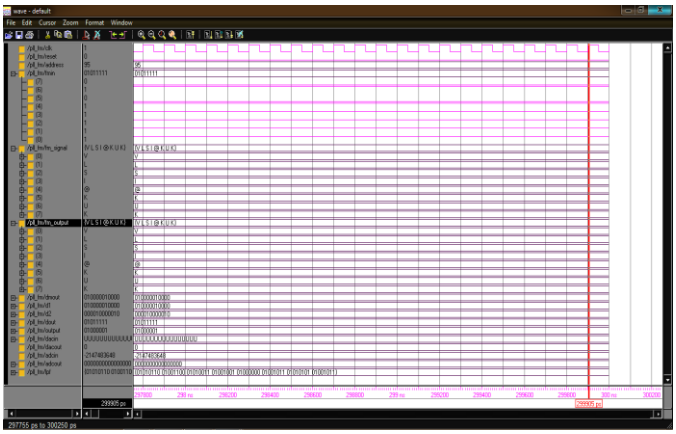

Fig. 4: Model Sim Simulation of FM Receiver –data 1

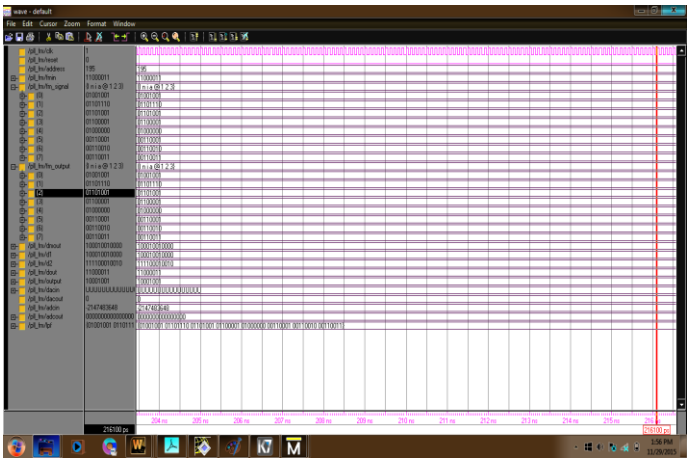

Fig. 5: Model Sim Simulation of FM Receiver –data 2

Device utilization report gives the percentage utilization of device hardware for the chip development of the chip. Device utilization report provides the information of no. of slices, no. of flip flops, no. of input LUTs, no. of bounded

IOBs, and no of gated clocks (GCLKs) used in the implementation of design. Timing details are helpful in analyzing the timing performance based on the information of delay, timing parameters such as minimum period, maximum frequency, minimum input arrival time before clock and maximum output required time after clock. Table 1 and Table 2 show the synthesis results as device utilization and timing parameters for digital FM Receiver.

Table1: Device utilization in DPLL based FM receiver

Device	Utilization
Number of Slices	500 out of 12480, 4%
Number of Slice Flip Flops	996 out of 12480, 8%
Number of 4 input LUTs	112 out of 493, 11%
Number of bonded IOBs	70 out of 172, 41%
Number of GCLKs	1 out of 32, 3%

Table 2: Timing parameters for FM Receiver

Timing parameter	Utilization
Minimum period	1.671ns
Maximum frequency	400.00MHz
Minimum input arrival time before clock	4.90 ns
Maximum time after the arrival of clock	2.230ns
Total memory usage	151340 KB

4. Conclusions

The design for the different components of digital PLL and FM is carried successfully with the help of VHDL programming language. The functional check for the design is carried with different frequencies and test cases the value of frequency varies form 0 -255 MHz. The design is a great solution for the future generation FM receiver.

ACKNOWLEDGEMENT

I would like to acknowledge Dr. Adesh Kumar Assistant Professor Department of Electronics, Instrumentation and Control Engineering, University of Petroleum & Energy Studies, Dehradun (Uttrakhand), India for inspiring me to continue my research work.

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