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Experimental Design of a Ternary Full Adder using Pseudo N-type Carbon Nano tube FETs.

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Abstract - ***A full adder is an important component of an arithmetic circuit. Increasing the level of logic in an Adder circuit results in more efficiency as it can compute larger numbers with greater accuracy. In this paper a ternary adder is designed with ternary logic. The implementation of the design is based on Pseudo N-type carbon nano tube field effect transistors. This paper shows the analysis of the ternary full adder and evaluates the design depending on its power consumption, delay and power delay product.***

Key Words: *TFA, Ternary Logic, Ternary Full Adder, Pseudo N-type CNTFET, Pseudo.*

1. Introduction

With the advancement of technology need for smaller high performance electronic devices are growing rapidly. Scaling down of MOSFET transistors has reached its minimum and further shrinking has introduced challenges like high leakage current, passive power dissipation, short channel effects and variations in device structure and doping[1]. These challenges can be overcome to a very good extent by replacing the traditional MOSFET with Carbon nano tube field effect transistors. Structurally CNTFET is similar to MOSFET, with carbon nano tubes used as channels instead of traditional channel material. Considering the advantages of CNTFETs a lot of binary, multi value logic, arithmetic circuits have been designed [2-6].

Ternary logic has many advantages over binary circuits such as it reduces the number of required computation steps. The Full adder presented in this paper is based on ternary logic. The circuit designed in this paper has low threshold voltage to keep the power dissipation low. Pseudo N-type CNTFET's is used to design the TFA cell. The full adder is designed based on binary nature of a TFA and pseudo transistor based logic requiring less gates. To decrease the power consumption the design uses two sources. In this Paper a CNTFET based Ternary Full Adder is designed, analyzed and evaluated on the basis of its performance based on power dissipation, Propagation delay and PDP. Extensive simulation under different operating conditions is performed using HSPICE.

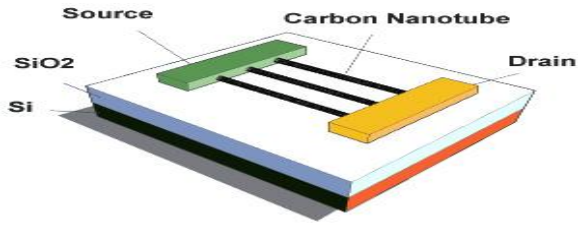


Fig -1: CNTFET structure similar to that of a MOSFET

2. Review of Carbon Nano Tube Field Effect Transistor (CNTFET)

Carbon nano tube field effect transistor uses carbon nano tube as a channel material. Carbon nano tube (CNT), discovered by S.Iijima[7], is a tube produced in nano scale as rolled sheet of graphite. CNTs can be single walled (SWCNT) or multi walled (MWCNT) depending on the angle of the atom arrangement along the tube. This is referred to as the chirality vector and is represented by the integer pair (n,m). A simple method to determine if a carbon nano tube is metallic or semiconducting is to consider its indices (n,m). The nano tube is metallic if n=*m* or *n-m=3i*, where *i* is an integer. Otherwise, the tube is semiconducting.

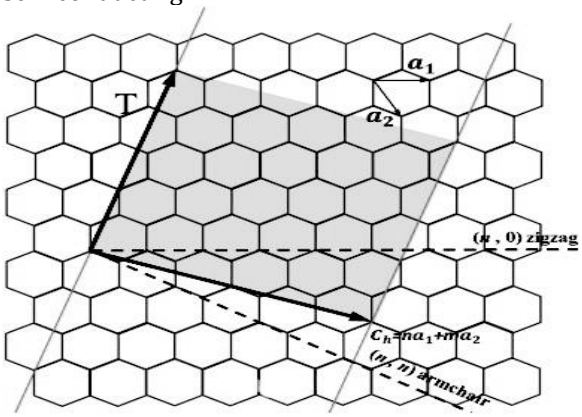


Fig -2: Construction of Graphene sheet and important parameter for CNTs: C_h is chiral vector, T is tube axis, and θ is chiral angle [8]

Every carbon atom on the sheet can be expressed as a function of integers (n, m). A chiral vector C is the vector perpendicular to the tube axis T[10], given by

$$\bar{C} = na_1 + ma_2 \quad (1)$$

The diameter of the CNT can be calculated based on the following equation [10]:

$$D_{CNT} = \frac{a_0\sqrt{3}}{\pi}\sqrt{n^2 + m^2 + nm} \quad (2)$$

Where, $a_0 = 0.142nm$ is the inter-atomic distance between each carbon atom and its neighbor.

This nano tubes are used as channel material in the construction of a CNTFET. Fig-1 shows the structure of CNTFET with tubes connecting the source and drain. Use of CNT eliminates the bulk silicon channel reducing the effects of parasitic elements. Similar to a MOSFET, CNTFETs can be both n type and p type. The current-voltage (I-V) characteristic [10] of the CNTFET is shown in Figure 3. They are similar to the I-V characteristics of a MOSFET.

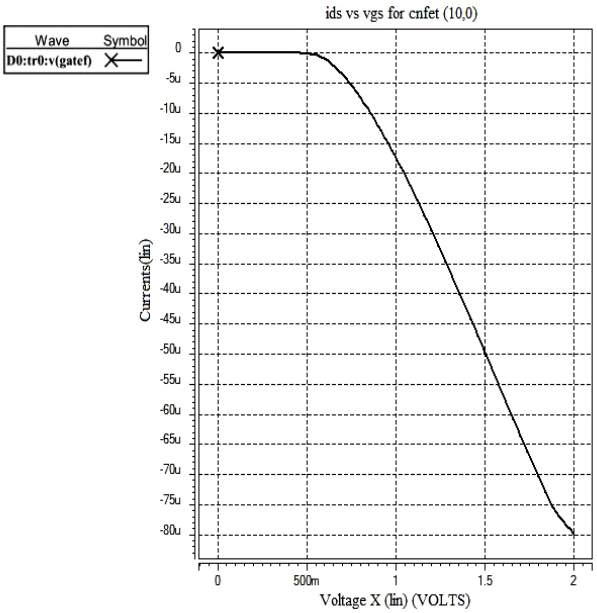


Fig -3: I–V characteristics curve of a typical NCNTFET for the chirality vector (10, 0)[10]

The threshold of the CNTFETs is calculated based on the following equation[10]:

$$V_{th} \approx \frac{E_g}{2} = \frac{\sqrt{3}}{3}\frac{a V_\pi}{e D_{CNT}} \quad (3)$$

Here $a = 2.49\text{Å}$ is the carbon-to-carbon atom distance, $V_\pi = 3.033eV$ is the carbon bond energy, e is the unit electron charge

From equation (3) it is seen that the threshold voltage us inversely proportional to the CNT diameter, which makes a CNTFET device able to work in multi-threshold designs. The unique feature of CNTFET makes it a promising device to be implemented in low power VLSI systems.

3. Review of Ternary Logic

Ternary logic is a generalized form of the binary logic. In binary logic values (0, 1) is used, where Vd=1 and GND =0. In Ternary logic we use (0,1,2) where Vd=2, Vd/2=1 and Gnd=0. The basic ternary logic gates can be defined as follows. Table -1 shows the ternary logic symbols.

Table -1: Logic Symbols

Voltage Level	Logic Value
0	0
Vd/2	1
Vd	2

The most important structural block of a ternary system is the ternary inverter. A universal ternary inverter is a gate which has one input x and three outputs such that[11]:

$$Y(STI) = C_1(X) = 2 - \bar{X},$$

$$Y(NTI) = C_2(X) = \begin{cases} 2 \text{ if } X = 0, \\ 0 \text{ If } X \neq 0, \end{cases} \quad (4)$$

$$Y(PTI) = C_2(X) = \begin{cases} 2 \text{ if } x \neq 2, \\ 0 \text{ if } x = 2, \end{cases}$$

Thus a ternary inverter requires three inverters, a STI, PTI and a NTI[11]. Truth tables for the three inverters are shown in Table -2 and the schematics are shown in Fig- 4.

Table -2: Truth table of STI,PTI and NTI

Value	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

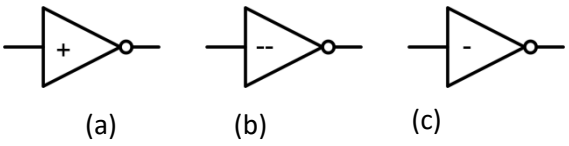


Fig -4: Ternary inverters (a) STI (b) PTI (c) NTI

3. Proposed Design

The ternary full adder performs addition between two ternary variables. A TFA cell is the basic component of a Ternary adder. A TFA cell performs addition between two Ternary 1 bit numbers (A and B) and the third bit is the carry signal (Cin) generated from previous lower significant position of a n-nit addition and generates two outputs, Sum and Cout. The maximum number a Sum can produce is 4 at LSB or at most 5 in other positions, which generates Cin equal to logic 1. Therefore Cin can be logic 0 or logic 1. Table.-3 shows the truth table of a ternary adder.

Table -3: Truth Table of ternary full adder

A	B	Cin	Sum	Cout
0	0	0	0	0
0	1	0	1	0
0	2	0	2	0
1	1	0	2	0
1	2	0	0	1
2	2	0	1	1
0	0	1	1	0
0	1	1	2	0
0	2	1	0	1
1	1	1	0	1
1	2	1	1	1
2	2	1	2	1

The TFA cell is designed based on careful investigation of the Truth table. Here, The TFA uses the ternary decoder designed in paper[11]. The Ternary decoder produces the unary functions of input A and B. The equation to design the TFA are shown below :

$$XFA = B_0(\overline{Cin}.A_1 + Cin.A_0) + B_1(\overline{Cin}.A_0 + Cin.A_2) + B_2(\overline{Cin}.A_2 + Cin.A_1) \quad (5)$$

$$YFA = B_0(\overline{Cin}.A_2 + Cin.A_1) + B_1(\overline{Cin}.A_1 + Cin.A_0) + B_2(\overline{Cin}.A_0 + Cin.A_2) \quad (6)$$

$$SUM = XFA + 2.\overline{YFA} \quad (7)$$

$$Cout = A_2(\overline{Cin}.A_2 + Cin.B_1 + Cin.B_2) + B_2(\overline{Cin}.B_2 + Cin.A_1) + B_1(Cin.A_1) \quad (8)$$

where, A0, A1, A2, B0,B1 and B2 are unary functions of A and B. Cin is the Carry in. Equation (5), (6) and (8) is formulated based on binary and equation (7) is formulated based on ternary nature to get the final SUM. To implement, The unary functions are generated utilizing the ternary decoder of [11] shown in Fig-5. The decoder contains PTI, NTI and ternary NOR gates. XFA and YFA both produce logic 1 when the equation (5) and (6) is true. To get the SUM where logic 2 is required, YFA produces logic 1 ie. $\overline{YFA}$ is logic 0, to make the SUM equal to logic 2. In any other cases when YFA is logic 0, SUM is equal to XFA (Logic 0 or Logic 1).

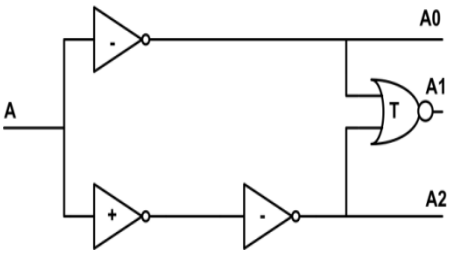
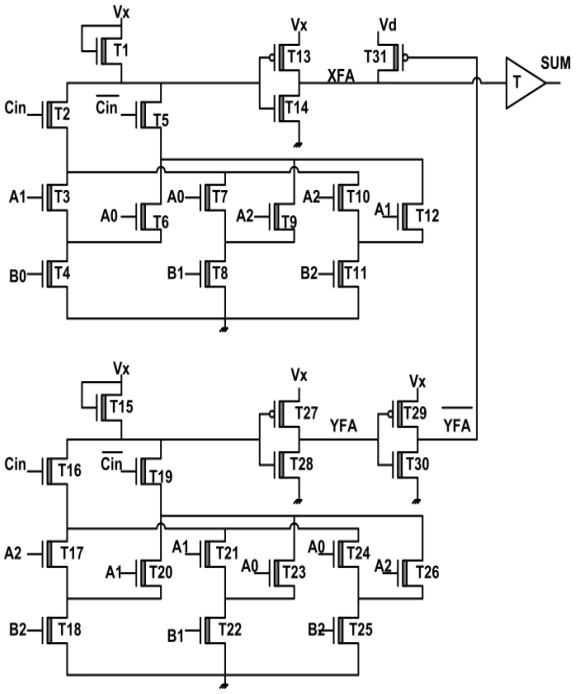
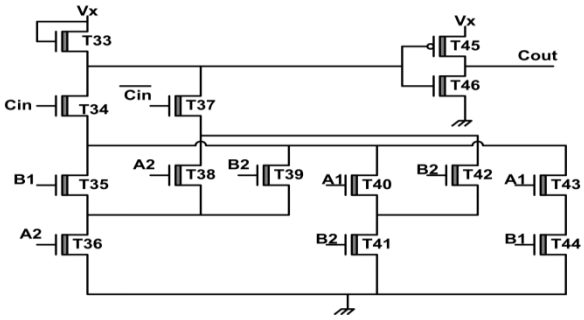


Fig -5: Ternary Decoder [11]

The equations are implemented using Pseudo N-type CNTFETs. The proposed design uses two source with voltage value of 0.45V(Vx) and 0.9V(Vd) which are equal to the voltage value of logic 1 and logic 2 respectively. The proposed design is given in Fig-6. The design utilizes pseudo pass transistor based realization of the equations.



(a)



(b)

Fig -6: Proposed Design of a TFA cell. (a) Sum generator, (b) Carry Generator.

In the proposed design all the transistors has the chirality vector of (19,0) which yields a threshold voltage of 0.293 V. When T2 is on along with T3, T4 or T7, T8 and T10,T11; XFA is equal to Vx which is logic 1. Similarly when T5 is on along with T6,T4 or T9,T8 or T12,T11; XFA is equal to Vx. YFA is high when along with T16, T17 or T21,T22 or T24,T25 is on. Similarly if T19 is on along with T20,T18 or T23,T22 or T26,T25. Here both XFA and YFA can produce logic 0 or logic 1. Transistor T31 is used to get logic 2. From equation (7), SUM is logic 2 when YFA is on. T31 is a PCNTFET and only turns on when YFA is logic 1 i.e . $\overline{YFA}$ is logic 0. To do this T29 and T30 are used which acts as the binary inverter and inverts YFA, so that T31 is on and passes Vd which is Logic 2 to the SUM output. A Ternary buffer 'T' is used in the proposed design. The ternary buffer is used to increase the driving capability of the SUM output. The design of the ternary buffer is shown in Fig.-7.

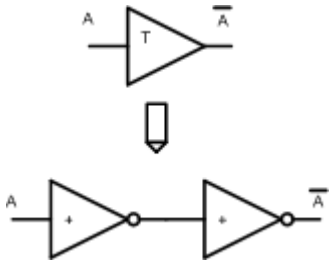
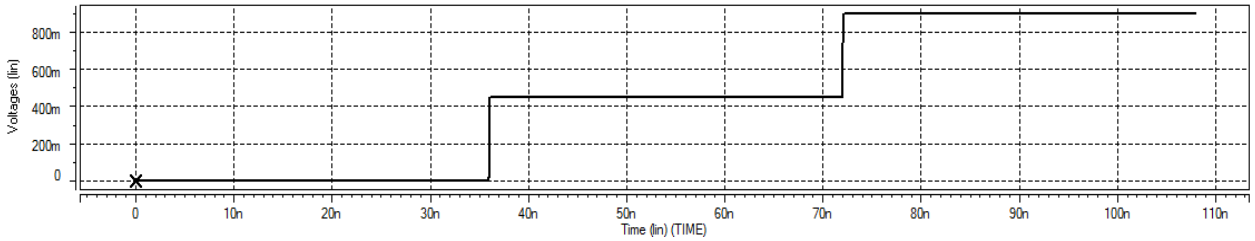


Fig -7: Ternary Buffer

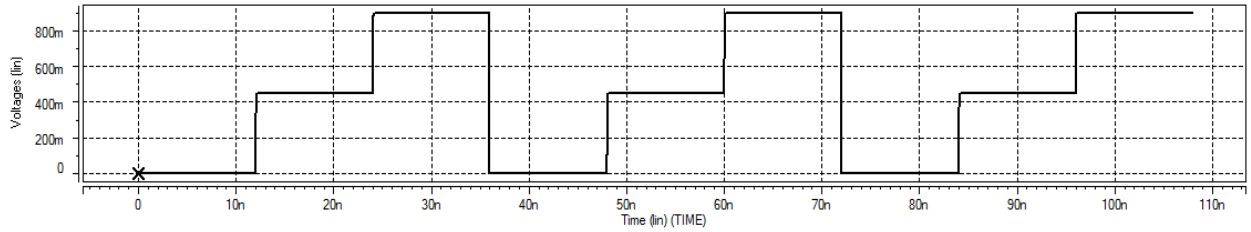
Fig -6(b) is the proposed carry out generator designed, based on equation (8). From the equation it is seen that Cout is also binary in nature and is designed utilizing its binary nature. Here, Vx (0.45) is used as supply of the circuit.. Cout is high when T34 is on along with any of the following transistor pairs T35,T36 or T39.T36 or T40,T41 or, T42,T41. And again Cout is high when T37 is on along with T38,T36 or T42,T41 is on. In every other cases Cout remains off i.e logic 0. For the design of the carry generator all the transistor has the chirality vector (19,0) and threshold voltage is 0.293 V.

4. Simulation and Performance Analysis

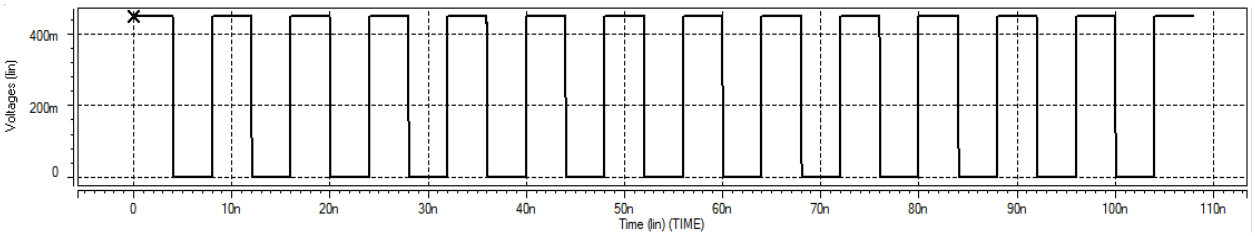
In this section, the designed TFA cell is simulated and analyzed under various conditions using Synopsis HSPICE simulator with 32nmm STANFORD model of CNTFET [12]. This model has been designed for MOSFET like Single Walled CNTFETs, which includes practical non idealities such as, charge screening effects, scattering SB effects, parasitic including CNT, Source/Drain, Gate Resistances and Capacitances. The model also includes full transcapacitance network to deliver more accurate transient and dynamic responses [13, 14]. The transient simulation of the design is performed at room temperature, at 250 MHz operational frequency and at 0.9V supply. Moreover a capacitor of 2fF is used at the output nodes of the circuit for simulation. Simulation is done for all the input combinations of A, B and Cin for a longer period. An input pattern with all the combination ensures that the average power consumption is accurate estimation of the power consumption of the circuit. The propagation delay is measured for all the possible input variations. The maximum propagation delay is considered as the propagation delay to provide accurate estimation of the delay of the proposed design. The PDP of the circuit is measured by multiplying the propagation delay with the average power consumption.. Fig-8 shows the waveform of the sample input and output signals which authenticates the correct operation of the circuit.



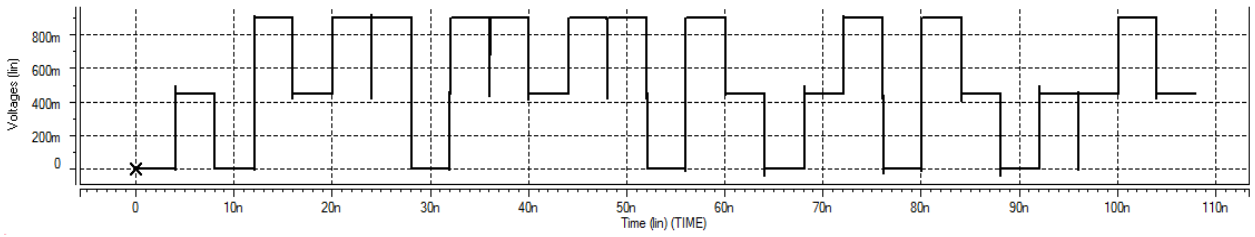
A



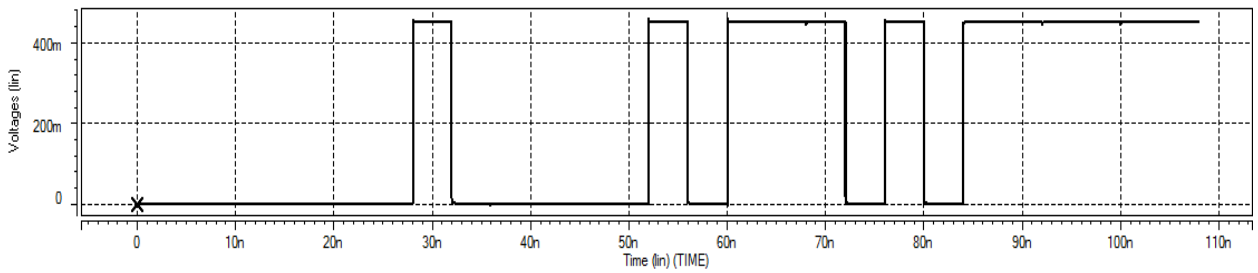
B



Cin



SUM



Cout

Fig -8: Transient analysis of the proposed design

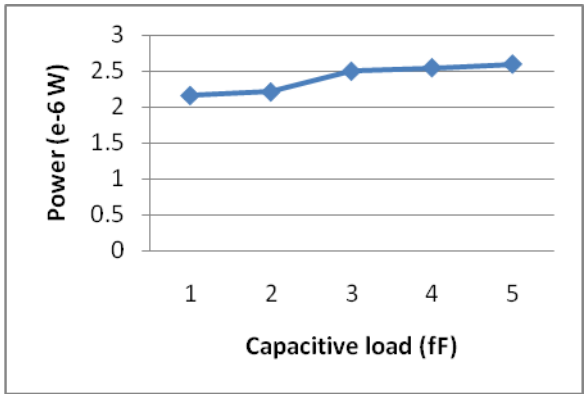
5. Results and Discussions

Table-4 shows the delay, power consumption and PDP of the proposed design. The designed TFA has a low power dissipation but the propagation delay is high.

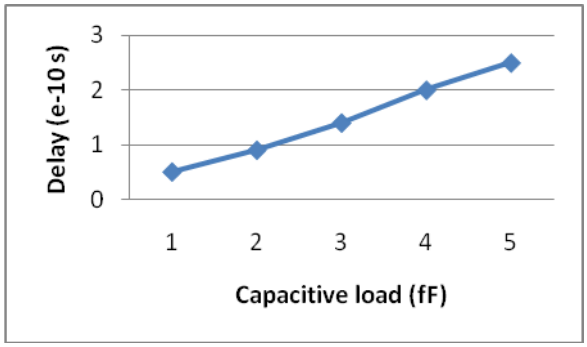
Table -4: Simulation Results of CNTFET based TFA cells

Circuits	Delay(e-10 S)	Power (e-6 W)	PDP (e-16 J)
Designed TFA	0.9	2.21	1.989

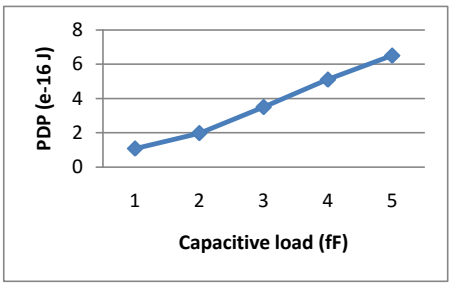
To analyze the driving capability of the design the output load was varied from 1fF to 5 fF to measure the effect of load variation on Delay and Power consumption. Simulations are performed at room temperature with 250 MHz operational frequency. Fig-9(a-c) shows plot of power consumption, delay and PDP of the proposed circuit with respect to varied load capacitors. The slope of the power vs load curve in Fig-9(a) indicates the power consumption of the circuit is less sensitive to the load variation. In Fig-9(b)the delay curve increases with the increase in load. This is due to the fact that psuedo N-type CNTFETs shows more resistance than a complimentary CNTFET arrangement which results in better static power consumption but on the contrary the delay increases[15]. Fig-9(c) shows the overall change in PDP with load capacitors. Since the delay increases with load the PDP increases with the increase in load. The designed circuit performs better at lower loads.



(a)



(b)



(c)

Fig -9: Simulation results at different load Values: (a) Power consumption,(b) delay, (c) power delay product

6. CONCLUSIONS

This paper has presented an experimental design of a Ternary Full Adder based on pseudo N-type CNTFETs The proposed design uses pseudo transistor based design to reduce the number of CNTFETs, which in turn reduces the overall Power consumption, but with increase in propagation delay. Extensive simulation has shown that design is power efficient but not acts slower at higher loads. Further research may include the research of reducing delay of the design.

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