Review of high throughput area efficient pipelined viterbi decoder for wireless application

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Abstract – *This paper presents a pipelined VSLI architecture for virerbi decoder. This used in many wireless communication systems due to good error control performance convolutional encoder and viterbi decoder. The viterbi algorithms are used for decoding the convolutional codes to design the convolutional encoder and pipelined vietrbi decoder is in field programmable gate array. This architecture is capable of achieving high throughput in area efficient manner. Hence it required for large constraint length and high throughput rate. The throughput can be linearly increases by increasing the basic process elements. The add compare select (ACS) units and trace back units and its sub circuits of the viterbi decoder have been operated in pipelined manner to achieve high throughput rate. By analysis the algorithm of viterbi decoder, it explores a practical method to design a pipelined processing of viterbi decoder.*

Key Words: *convolutional encoder, viterbi encoder, viterbi algorithm, FPGA, pipelining.*

1. INTRODUCTION

In communication system the convolutional coding has been used with the help of deep space communications and wireless communications. It is an alternative to block codes for the transmission over a noisy channel. A convolutional coding having a many advantages it can be applied to a continuous data stream as well as to blocks of data. In IS-95 and wireless digital cellular standard for CDMA (code division multiple access) also in employs convolutional coding. In the Viterbi decoding algorithm, proposed Viterbi in 1967, is a decoding process for convolutional codes in memory-less noise. This algorithm can be applied to a problems encountered in the design of communication systems.

This Viterbi decoding algorithm gives both a maximum likelihood and a maximum a posteriori algorithm. A maximum a posteriori algorithm identifies a code word that maximizes the conditional probability of the decoded code word against the received code word and maximum likelihood algorithms identifies and indicate a code word that maximizes the conditional probability of the received code word against the decoded code word. These two algorithms give the same results when the source information has a uniform distribution. Traditionally, In VLSI design the performance and silicon area are the two most important concerns. Recently, in battery power application power dissipation has also become an important concern, such as laptop computers, pagers and cellular phones. Power dissipation can be classified into two categories, dynamic power dissipation and static power dissipation.

1.1 Viterbi decoder architecture

In the organization of convolution encoder and Viterbi decoder several important design issues have also been discussed such as, branch metric unit computation method, the design of add compare select, parallel unit of trace back and decoder. A normal Viterbi decoder is usually composed of five blocks, as shown in the Fig. 1.
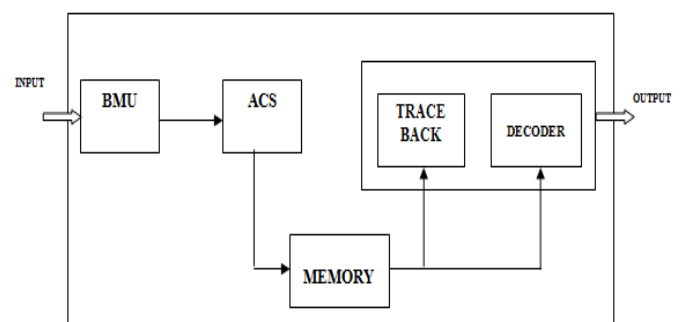

Fig -1: Viterbi decoder architecture.

BMU (Branch Metric Unit) –It receives the input signals and compare the difference between the input signals and the expected values, and then gives the results to the Add Compare Select. [1], [6]
ACS (Add Compare Select) – ACS completes the survivor paths and creates the decision vector. In this module there are two comparers, and these two comparers are exactly parallel. The one is used for comparing data bit and the

other is used for comparing signal bits. The advantage of this design is to reducing the circuit timing delay. [1], [6] MEMOEY- MEMORY is cycle used for saving the survivor paths. The core unit of this design is the TB (Trace Back) and DECODER, which include two function modules. The one is TB that read the information of the survivor paths in the MEMORY and other is DECODER that computes the output results. These two modules are work simultaneously in different MEMORY addresses. In this way, the Viterbi decoder is more efficient than a normal one because the DECODER do not need to wait TB. [1], [6]

2. LITERATURE REVIEW

In this paper a modified Viterbi algorithm has been presented for a Wi-Fi receiver. It shows that by using Xilinx tool in verilog design plan goes ahead associated with the modified Viterbi decoder implementation. An implementation on Field Programmable Gate Arrays (FPGA) gives user flexibility to a lowering the cost and programmable solutions. [1]

In this paper proposes an implementation on the CSA which optimizes Viterbi decoder circuits. CSA gives first comparison method for path metric calculation and reduced at circuit Hamming distance calculation. CSA module improves the power consumption up to 10% with respect to the total area of the circuit. For error minimization in CSA module the counter output is compared with number of input bits. By this CSA module experimental results indicate that the proposed CSA module decreases nearly 10% of power consumption.[2]

The author proposed a pre-computation scheme with associated hardware architecture is proposed for Viterbi decoders employing T-algorithm. Compared with existing schemes that target at efficient implementation of T algorithm, the proposed approach is more reliable in general. The analysis of the critical path reveals that the pre-computation scheme can achieve the iteration bound for Viterbi decoders employing T-algorithm with negligible hardware overhead. [3]

In this paper the author shows three objectives. Firstly, to design and simulated an orthodox Viterbi decoder is used . The Gate Diffused Input Logic (GDIL) based Viterbi decoder for faster process application is designed using Xilinx ISE, simulated and synthesized successfully. The new proposed GDIL Viterbi gives low power simulation results with very less path delay. Secondly, the GDIL Viterbi decoder is ones again compared with our proposed technique, which comprises a Survivor Path Unit (SPU) implements a trace back method with DRAM. This proposed approach of incorporating DRAM stores the path information in a manner which allows fast read access without requiring physical partitioning of the DRAM. This leads to a comprehensive gain in speed with low power effects. Thirdly, all the viterbi decoders are compared, simulated, synthesized and the proposed approach shows

the best simulation and synthesizes results for high speed application and low power in VLSI design. [4]

In this paper presents the Viterbi algorithm is one of the very popular for decoding convolutional codes. Due to this Implementation of high-speed Viterbi decoder is a demanding task due to the recursive iteration of an add-compare-select operation. In this paper, we suggest and examine various optimization techniques to advance the area and performance tradeoffs on Virtex-6 FPGAs of high speed Viterbi decoders. Add-compare-select units are implemented with Radix-2, Radix-4 and a modified radix-4 techniques. By using Virtix-6 FPGA in that proposed technique to achieve very efficient designs of Viterbi decoders in terms of performance and area. With the help of radix–2 solutions the 360 Mbps are achieve and with radix-4 can achieve 430 Mbps, better than previous state of the art solutions. The sliding block method gives higher data rates can only be achieved with other parallelization techniques. [5]

The Author proposed due to the excellent error control performance Convolution encoder and Viterbi decoder are widely used in many communication systems. By using field Programmable Gate Array this paper deals with the design and implementation of convolution encoder and Viterbi decoder. By study the algorithm of Viterbi decoder, the paper explores a practical method to design a parallel processing Viterbi decoder. It means that trace back units and decoder can simultaneously work in order to improve the processing speed. The experimental results show that this method is feasible, and some of the implementation issues related to the Viterbi decoder, such as branch metric unit, add compare select, memory unit and trace unit. [6]

3. CONVOLUTION ENCODER

Convolutional encoder is takes input data bits and gives out of two bits. It also combines the fixed number of input bits. The input bits are stored in fixed length of shift register and they combine with mod – 2 adders which are implemented with a XOR gate. Convolutional encoding is also process of adding redundancy to signal bit of stream and it is equivalent to binary convolutional.

The concept is illustrated with help of above example. As shown in Figure. 2, whenever the message bit is shifted to position „S‟, the new values of V1 and V2 are generated depending upon S0, S1, and S2. S1 and S2 store the previous two message bits. The current bit is present in S0. Thus, equation becomes, V1= S0 XOR S2, and V2= (S0 XOR S1) XOR S2

The output switch first samples V1 and then V2. The shift register then shifts contents of S1 to S2 and contents of S0 to S1. Next input bit is then taken and stored in S0. Again V1 and V2 are generated according to this new combination of S0, S1, and S2. The output switch then samples V1 and V2. For every input message bit two

encoded output bits V1 and V2 are transmitted. For a single message bit, the encoded code word is two bits for this convolution encoder. Number of message bits k=1, Number of encoded output bits for one message bit, n=2.
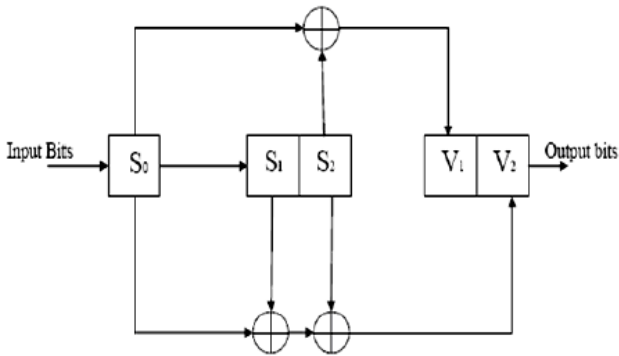

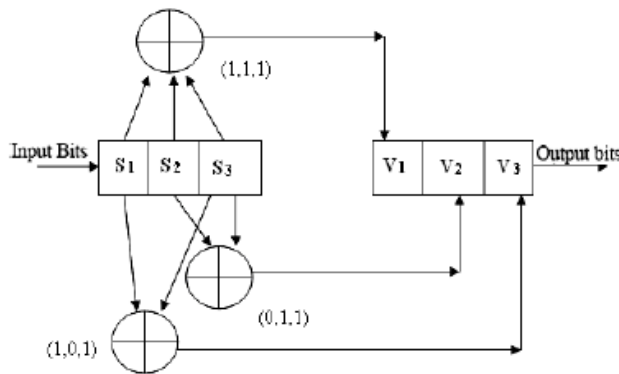**Fig -2**: The Rate 1/2 convolutional encoder.

Fig -3: The Rate 1/3 convolutional encoder.

4. VITERBI ALGORITHM

The Viterbi Algorithm given the named after Andrew Viterbi it is a active algorithm that proceed with certain path metrics to compute the 'most likely' path of a transmitted sequence. From this algorithm "most likely" path there are certain bit errors can be corrected to decode the original bit sequence given after it has been sent down a communicative line. An important characteristic of the Viterbi algorithm is that ties are randomly solved and still constant an original sequence. In this algorithm what the Viterbi algorithm can do is correctly reproduce your input string at the output even in the presence of one or more errors. With more errors introduced in the likelihood of a successful decryption does go down. This two system i.e. Convolution encoding and Viterbi decoding are the most accepted because of their powerful coding-gain performances. In a wide variety of devices this Convolutional encoder and Viterbi decoder is extensively used to reduce transmitted power and decrease the degrading effects of noise in the channel. For more complex satellite receivers and deep space

missions the Viterbi decoder is used in devices ranging from the mobile phones people use in the daily life. In the the wireless connections the Viterbi decoder is mainly used where the additive wide Gaussian noise is pre dominant. FEC ensemble FPGA because they have efficient parallel architecture from this we can reconfigure them without nonrecurring engineering costs and with their performance is always improving.

for finding the shortest path through a trellis we can view the Viterbi algorithm as a dynamic programming algorithm and the algorithm can be broken down into the following three steps.

Weigh the trellis; that is, calculate the branch metrics. [8]

Recursively compute the shortest paths to time n and in terms of the shortest paths to time n-1. In this step, decisions are used to recursively update the survivor path of the signal. This is known as add-compare-select (ACS) recursion. [8]

Recursively find the shortest path leading to each trellis state using the decisions from Step 2. The shortest path is called the survivor path for that state and the process is referred to as survivor path decode. Finally, if all survivor paths are traced back in time, they merge into a unique path, which is the most likely signal path that we are trying to find. [8]
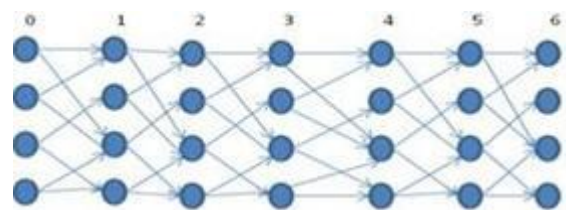

Fig -4: Actual flow if Viterbi algorithm

In fig. 4 in order to realize the process of look-ahead, consider the flow in the normal execution. On the basis of minimal value of the two possible paths at each time interval the branch metrics will be computed and the best path metric will be determined. This process will continue till the trellis is completely filled and the number of hops taken will be equal to the number of time stamps. Figure 4 depicts this that for filling a trellis to "6" time units, 6 comparisons needed to be done in "6" hops.[8]

5. CONCLUSIONS

Viterbi decoder is very important block in CDMA or wireless system. This paper has design and implemented convolution encoder and Viterbi decoder targeting FPGA implementation. The aim of this paper was to expand a pipeline processing in trace back and decoder memory unit and in this way we can show area efficient and to reduce power.

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