International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 02 Issue: 08 | Nov-2015 www.irjet.net p-ISSN: 2395-0072

Effects of Gate Length and Oxide Thickness on DG-MOSFET

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Abstract - ***In single Gate MOSFET, short channel effect give rise to many problems when it is scaled down to nanometres. Double Gate MOSFET (DG-MOSFET) is a new designing technology for technology for MOSFET which is more resilient to short channel effects. Here by changing the modelling parameter of DG-MOSFET (Gate Length and Oxide Thickness) we will study the effect of these parameters on I-V Characteristics of double gate MOSFET.***

Key Words: *KeyDIBL, Double-gate MOSFET, Short Channel Effects (SCEs)*

1. INTRODUCTION

In 1965 Gordon Moore predicted that the number of transistor on a device would quadruple every three years. The channel length which is an important dimension has been shrinking continuously and will continue to decreasing. The reason behind this continuous miniaturizing is to have high speed devices in very large scale integrated circuits. As we are scaling down the size of device, channel length of the device shrinks and this nearness between source and drain reduces the gate electrode's controlling influence on the potential distribution and current flow in the channel which in result deteriorates device performance .This instability in the structure when scaled device down to nanometers is mainly due to short channel effects (SCEs) like threshold voltage roll-off, gate leakage current, drain induced barrier lowering (DIBL), hot electron effects (HCEs) which play a major role in determining the performance of scaled devices. SCEs results in increasing the leaking current between the drain and source and reduces ON state to OFF state ratio of current.

Double gate MOSFET is an alternate emerging device to counter these all problems occurred in single gate MOSFET. This new architecture will aid us to maintain the Moore's law research going towards inventions of novel devices [1]-[4]. The predictions of International Technology Roadmap for Semiconductors (ITRS) are followed by the device designers to propose various novel device structures and process parameter variations [5].The relation between natural length of device and number of gates n, is given as: $\lambda = \sqrt[2]{\frac{\varepsilon_{Si}}{n\varepsilon_{ox}} t_{ox}}$ where n is number of gates, permittivity of Si, permittivity of oxide, t_{Si}& thickness of Si body and oxide respectively [5]. SCEs are directly proportional to so to maximize SCEs should to minimum by the above relation can be minimized by using more than two gates.

This paper presents brief discussion on the fact that how I-V Characteristics change when the length of the gate and thickness of oxide layer are varied in DG-MOSFET.

2. DEVICE STRUCTURE AND THEORITACAL APPROACH

2.1 DG-MOSFET STRUCTURE

In DG-MOSFET structure we use two gates namely front gate and back gate. Due to double gate structure, gate to channel coupling gets double and hence SCE's can be suppressed easily.

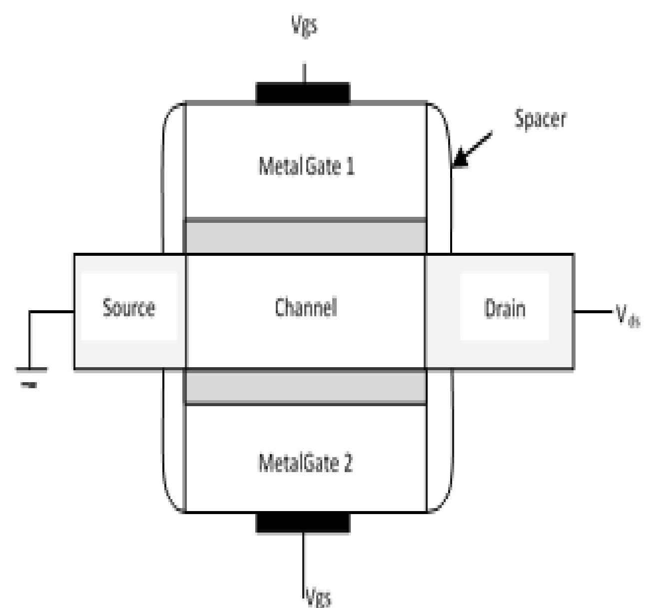


Fig -1:A general Double Gate MOSFET structure.

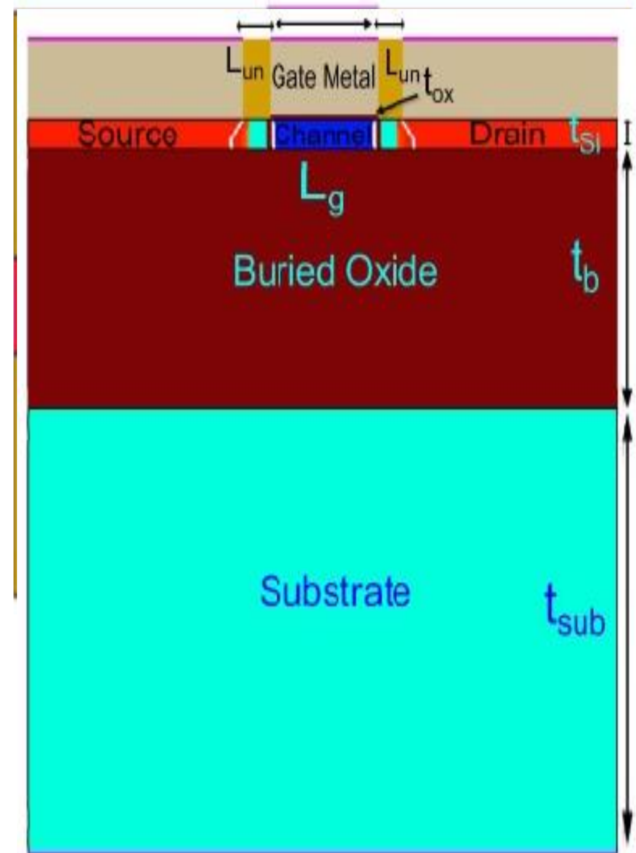
2.2 Types of DG-MOSFET

DG-MOSFETs may be categorized on the way the gate voltages are applied

2.2.1 Symmetric DG-MOSFET
A DG-MOSFET is said to be symmetric when both gates have the same work function and a single input voltage is applied to both gates.

2.2.2 Asymmetric DG-MOSFET
An asymmetric DG-MOSFET either has synchronized but different input voltages to both of the identical gates, or has the same input voltage to two gates but gates having different work functions [6].

Here we consider an ideal DG MOSFET viewed as a perfectly symmetrical device where the two channels facing each-other are activated simultaneously and feature identical charge and mobility. The schematic diagram of the single gate (SG) and double-gate (DG) MOSFET structures are used for basic understanding in Fig 2. In this figure of single gate MOSFET structure L_g is Gate length, t_b is the buried oxide thickness, t_{ox} gate oxide thickness and t_{Sub} *is* the silicon substrate thickness.



(a)
(b)

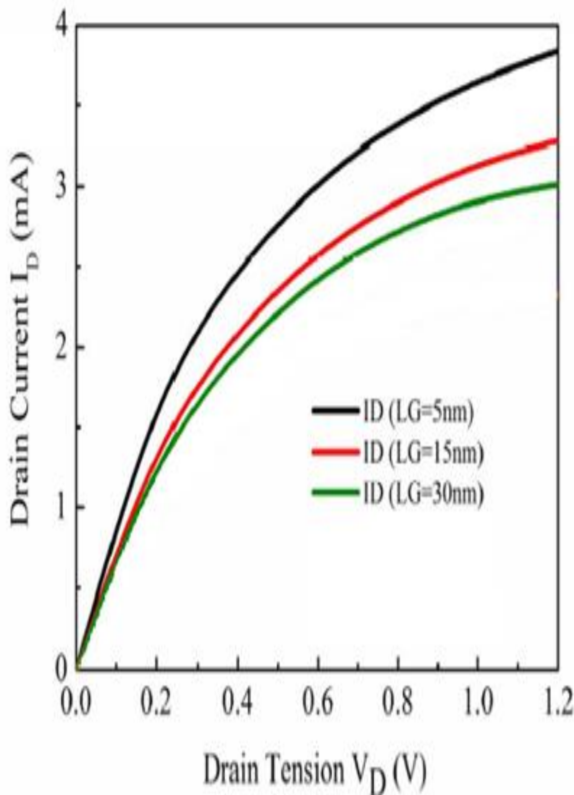
Fig -2: Schematic Structure MOSFET (a) Single Gate and (b) Double Gate MOSFET [5]

Above figure shows a Double Gate MOSFET having gate lengthL_g, length of underlap is L_{un} ,t_{ox} &t_{Si} are thickness of oxide and Silicon substrate thickness respectively. To understand the phenomena of DGFET semi-classical model and quantum-mechanical approach are used in a combined form. In MOSFET the movement of electron take place in channel .this movement of electron will be governed by drift diffusion equation [7]. Moreover this equation is linked with the universal conservation equation of particle density which states that current density is sum of the diffusion current and the drift current sum of the diffusion current and the drift current [8, 9].

3. I-V CHARACTERISTICS VARIATION

3.1 Variation in Gate Length

If the gate length is taken is 5nm, 15nm and 30 nm then I_D -V_D Characteristics for these three different gate length will be as per figure 3 [7]. With the increase of gate length, the saturation drain current decreases. Thus



reduction of gate length may result in DIBL effects. For short channel devices, when high drain to source bias is applied it shorten the threshold voltage and increases the off current. This effect is called drain induced barrier lowering (DIBL) effect which appears due to SCE's. DIBL is an important point that should be kept in mind while scaling down the MOSFET devices. If SCE's for shortchannel devices is not considered, it can be concluded that gate length does not drastically change the on state of DGFET. This happen because of high parasitic resistance which limits the on state current of device. If gate length is less significant than channel length, gate will lose its control over channel. So gate length should not be reduced randomly [10].

Fig -3:I_D-V_D characteristics atdifferent gate lengths.

3.2. Variation in Oxide Thickness

Similar to gate length if thickness of oxide layer is varied by taking the value of t_{ox} as 5 nm, 15 nm & 30 nm the variation of I_{D-V_D} curve will be as per fig 4[7]. It is useful to consider the impact of silicon thickness on the device current and performances.

Thinner gate oxide are necessary is the drain current and therefore more important are the transconductances. Therefore for large current the oxide layer thickness should be less. If the t_{ox} is larger drain current will increase which will shift threshold voltage of device to smaller values [11-13]. The off state current is high with thick oxide layer and low with thin oxide layer. Devices with thick oxide layer have less control of gate on channel barrier height [10].

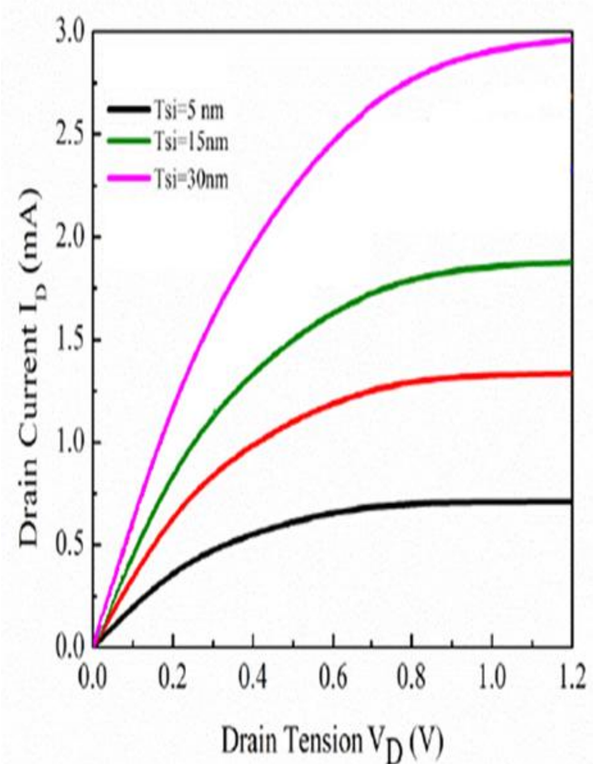


Fig -4: I_D–V_D characteristics at different oxide layer thickness

4. Conclusion

The main goal of the present work was to show the growing interest for double gate MOSFET. From the above discussions done in this paper, we can conclude that as we scale down the devices, according to the International Technology Roadmap for Semiconductors we can reduce the short-channel effects (SCEs) in MOSFET by using double gate. After a brief introduction of the problems occurred during miniaturizing of MOSFET, device structure and theoretical approach wereused to study DG-MOSFET. Variations of modelling parameters like Gate Length and Oxide Thickness have

been shown with a brief discussion on their influence on the device I-V characteristics.

5. References

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