CHARACTERIZATION QUATERNATY LOOKUP TABLE IN STANDARD CMOS PROCESS

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Abstract- The Binary logics and devices have been developed with an latest technology and gate design area. The design and implementation of logical circuits become easier and compact. Therefore present logic devices that can implement in binary and multi valued logic system. In multi-valued logic system logic gates varies in different logic systems, a quaternary has become mature in terms of logic algebra and gates. Some multi valued logic systems such as ternary and quaternary logic schemes have been developed. Quaternary logic has many advantages over binary logic. Since it require half the number of digits to store any information than its binary equivalent it is best for storage; the quaternary storage mechanism is less than twice as complex as the binary system. The Various quaternary logic gates and digital building blocks are presented and its power comparisons are made by using Tanner 14.2 version.

Keywords: Quaternary Lookup Table (QLUT), Multiple Value Logic(MVL).

1. INTRODUCTION

The emerging trend of technology gives the better ways of communicating when compared with earlier stages. The field of computation and(SP)signal processing is growing day by day. The technology mainly improves by means of VLSI revolution. Therefore an alternative technological solution to the problem of high speed information processing is needed.

Quaternary is the base 4 numerical system. It uses the digits 0,1,2,3 to represent any real numbers, four is the largest number with in the subsidizing range and one of two number that is both a square and a highly composite number(the other being 36),making quaternary an convenient choice for a base at this scale. despite being twice as large, its radix economy is equal to that of binary. Using CMOS technology this is the very low static power consumption in compare with NMOS technology. CMOS process gets low power and easy to scale down, gate of MOS need much lower driving current than base current of two polar, scaling down increase CMOS speed Comparing MVL present high power consumption, due to current mode circuit element or require nonstandard multi threshold CMOS technologies. multiple-value logic are increase the high power required for level of transition and increase the number of required interconnections ,hence also increasing the overall energy. Interconnections are increase the dominant contributor to delay are and energy consumption in CMOS digital circuit.

2. QUATERNARY LOGIC AND LUTs

Ternary logic system: It is based upon CMOS compatible ternary logic based circuit and analyzed its implementation and difficulties. They describe that multiple power sources will be needed for multiple thresholds and a new theory of transmission function will be required.

1. Arithmetic logic design with color coded ternary for ternary computing. We introduces a novel means of representing ternary states using color-codes, suggests a logic design model for a ternary half adder circuit and separate carry circuits.
2. Quaternary logic system: An extension of regular ternary logic function to function on discrete interval truth values. They presented this extension into quaternary valued logic and its mathematical properties.

A quaternary variable can assume 4 different logic levels. First I assuming a rail-to-rail voltage range and equal noise margins for four logic levels and three different reference voltage values are required,1/6vdd,3/6vdd,5/6vdd that value using to determine a quaternary value.

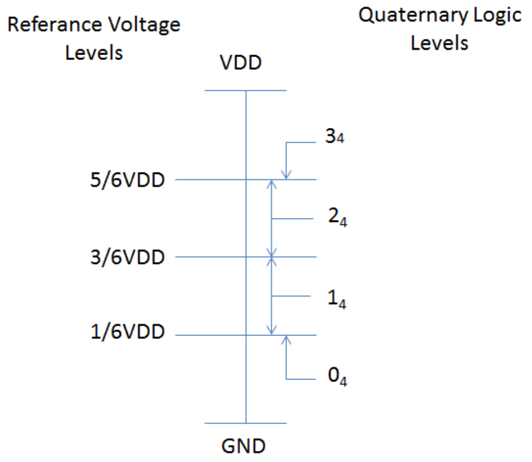


Fig -1Quaternary Logic Values and Reference Voltage

Therefore, two binary variables may be grouped in to one quaternary variable without data loss, merging two nodes in to one.It should be noted that there is no direct conversion of BTQ logic gates unconventional CMOS ,since the binary circuits use the available power rails to represent the binary symbols .For quaternary logic there are2more intermediate levels, which can not be obtained directly using the same techniques. On the another than, viable implementation so quaternary circuits have already been achieved for LUT.ALUT is an array indexing operator, where the output is mapping by the input, based on the configuration memory. The configuration values are initially stored in the Lookup table configuration memory, and according to the input ,the logic value in the addressed position is assigned to the output. By properly programming the LUT configuration memory ,the LUT can implement any logic function with give thenumber of inputs and outputs,making it very practical to implement reconfigurable hardware, such as FPGAs.

$$2^k:1$$

The number of possible functions that may be represented in aquaternary LUT is much larger than in a binary lookup table with the same number of inputs and outputs.Therefore, apart from reducing the total number of connections,MVL also leads to are duction of the total number of gates when compared with a binary implementation.

2. PROPOSED QLUT TOPOLOGY AND IMPLEMENTATION

2.1Quaternary Logic with Two Inversions

I need to achieve quaternary lookup table so I taking two inversions method with help of binary logic devicesMulti-valued logic (MVL) is a non binary logic with R>2. Binary logic is limited to only two states ‘True’ (1) and ‘False’ (0), MVL replace these with finite and infinite number of values. MVL system is defined as system operating on higher radix than two.

The Multi Value Logic LUT can replace or complement conventional binary logic, since the designed circuit is simple and efficient.

For example

1.Ternary logic (R=3) has three logical states {0, 1, 2} or { $\bar{1}$, 0, 1}. These are known as ordinary ternary.

2.Quaternary logic (R = 4) has four logical states {0, 1, 2, 3}.

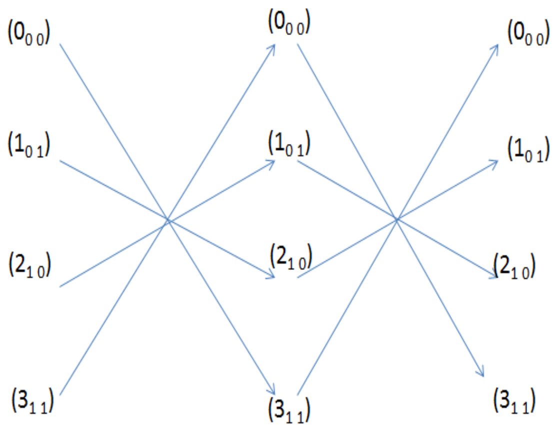
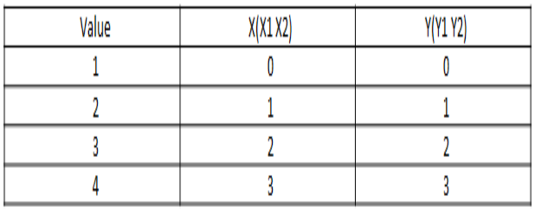


Fig 2: Quaternary Logic With Two Conversions

2.2 Two Binary NOT Gates And Implemented With CMOS Binary Logic

Using NOT gate and how to implementing lookup table in NOT gate truth table using quaternary lookup table and implementing with help of binary logic devices value.Giving the X1 and X2 input getting the output is Y1 and Y2.Input is 0,1,2,3 using two inversions method after that getting the output 0,1,2,3.

Table -1:NOT Gate Truth Table



Value	X(X1 X2)	Y(Y1 Y2)
1	0	0
2	1	1
3	2	2
4	3	3

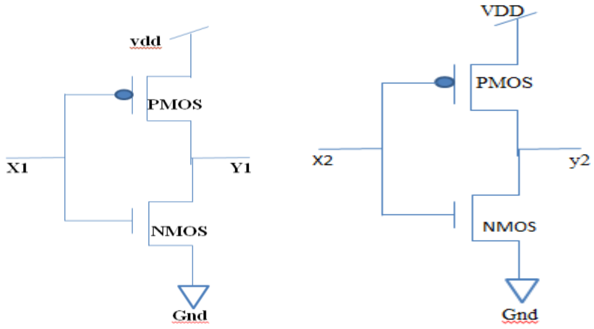


Fig -3: Two binary NOT gate Implemented With CMOS Binary Logic

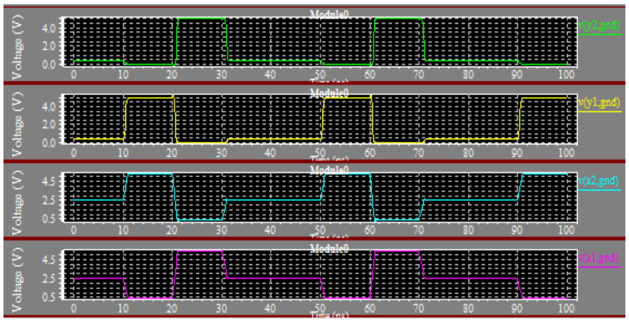
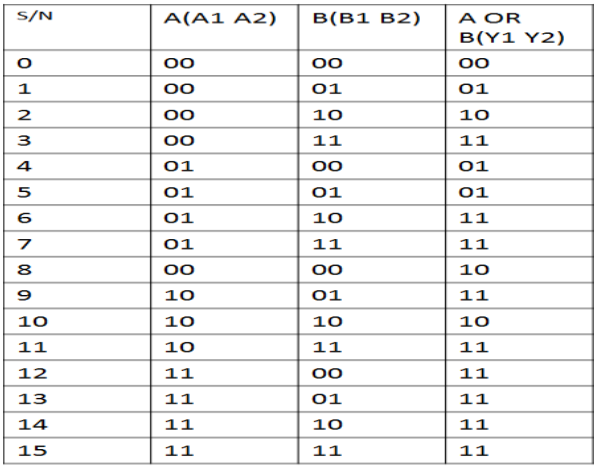


Fig -4:NOT gate output

2.3 Two Binary OR Gates And Implemented With CMOS Binary Logic

Two bit OR gate and how to implementing lookup table in OR gate truth table using quaternary lookup table and implementing with help of binary logic devices value.Giving the A1,A2,B1 and B2 input getting the output is Y1 and Y2.Input is 0,1,2,3 using two inversions method after that getting the otput 0,1,2,3.

Table -2:OR Gate Truth Table



S/N	A(A1 A2)	B(B1 B2)	A OR B(Y1 Y2)
0	00	00	00
1	00	01	01
2	00	10	10
3	00	11	11
4	01	00	01
5	01	01	01
6	01	10	11
7	01	11	11
8	00	00	10
9	10	01	11
10	10	10	10
11	10	11	11
12	11	00	11
13	11	01	11
14	11	10	11
15	11	11	11

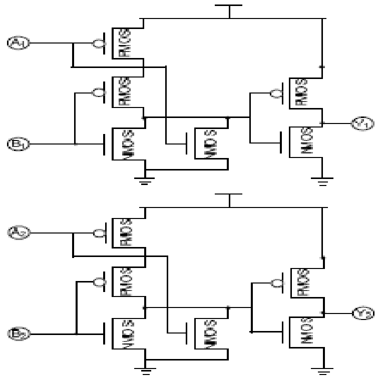


Fig -5:ORGate Circuit Design

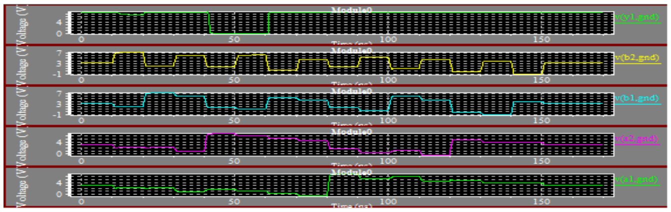


Fig -6: Output Y1 For OR Gate

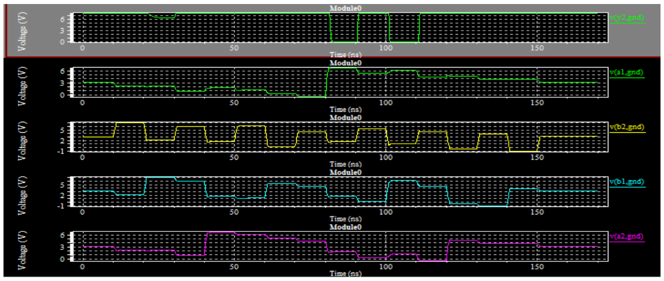


Fig -7: Output For Y2 OR Gate

2.4 Two Binary AND Gates And Implementing Using CMOS Binary Logics

This is and gate lookup table design and 16 possibility of combinational logic values.Input is A1,A2,B1 AND B2 OUTPUT is Y1 AND Y2 designing the AND gate circuit with help of the lookup table after getting the outputs.

Table -3:AND Gate Turth Table

S/N	A(A1 A2)	B(B1 B2)	A AND B(Y1 Y2)
0	00	00	00
1	00	01	00
2	00	10	00
3	00	11	00
4	01	00	00
5	01	01	01
6	01	10	00
7	01	11	01
8	00	00	00
9	10	01	00
10	10	10	10
11	10	11	10
12	11	00	00
13	11	01	01
14	11	10	10
15	11	11	11

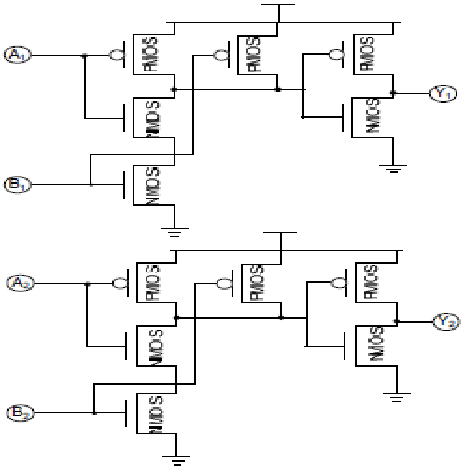


Fig -8:AND Gate Circuit

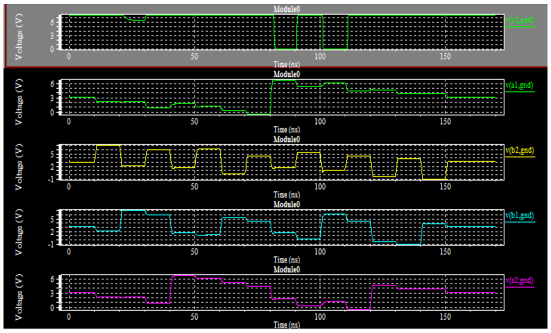


Fig-9:AND Gate Output y1

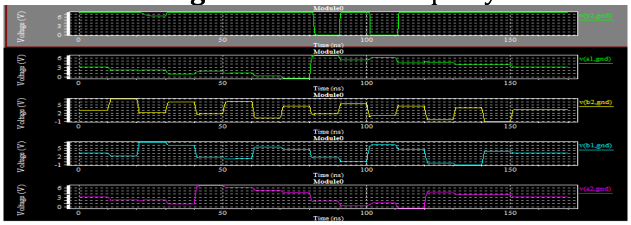


Fig -10:AND Gate Output Y2

2.5 Quaternary Half Adder

This is the half adder circuit separating the three part of design a,b,c a is sum,b is a AND gate design and c is a carry design combining the three type of design is the quaternary half adder design.

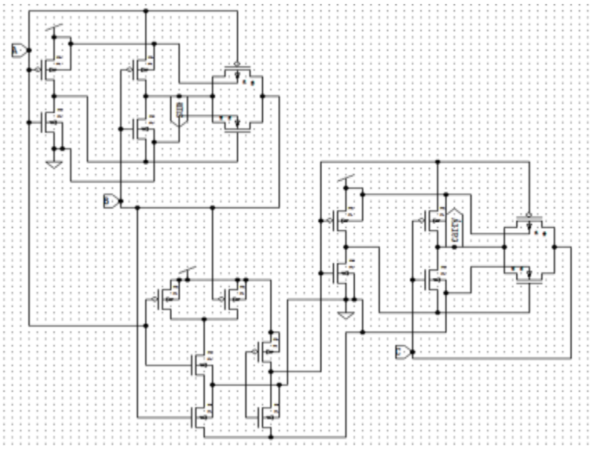


Fig -11: Quaternary Half Adder Circuit

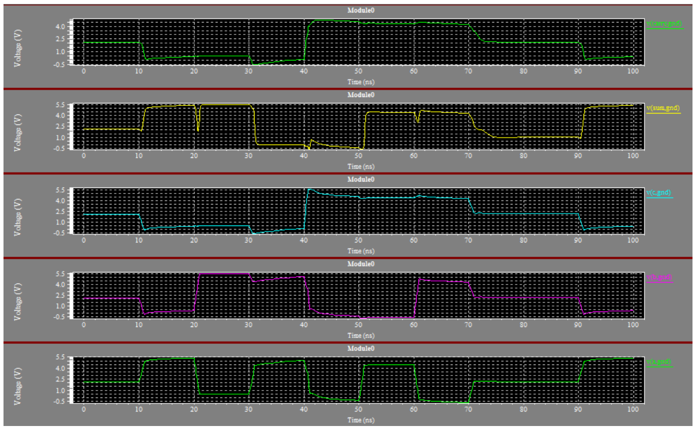
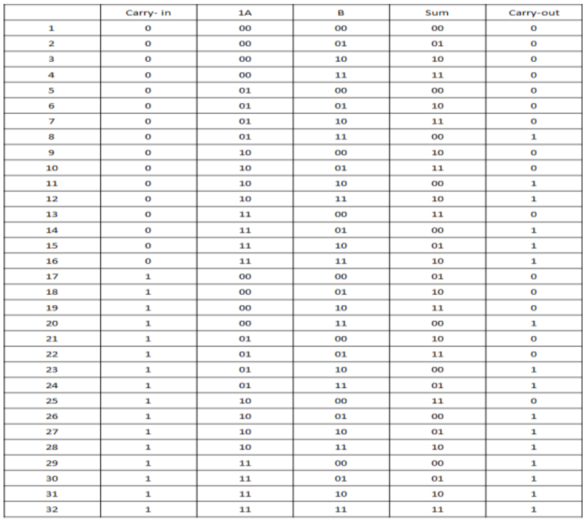


Fig -12: Quaternary Half Adder Output

2.7 Full Adder Design

A simple full adder implementation in CMOS with binary logic for two bits requires eighty transistors as compared to eleven required for the adder presented here using SWSFET with quaternary logic.

Table -3:fulladderTurth Table



	Carry- in	1A	B	Sum	Carry-out
1	0	00	00	00	0
2	0	00	01	01	0
3	0	00	10	10	0
4	0	00	11	11	0
5	0	01	00	00	0
6	0	01	01	10	0
7	0	01	10	11	0
8	0	01	11	00	1
9	0	10	00	10	0
10	0	10	01	11	0
11	0	10	10	00	1
12	0	10	11	10	1
13	0	11	00	11	0
14	0	11	01	00	1
15	0	11	10	01	1
16	0	11	11	10	1
17	1	00	00	01	0
18	1	00	01	10	0
19	1	00	10	11	0
20	1	00	11	00	1
21	1	01	00	10	0
22	1	01	01	11	0
23	1	01	10	00	1
24	1	01	11	01	1
25	1	10	00	11	0
26	1	10	01	00	1
27	1	10	10	01	1
28	1	10	11	10	1
29	1	11	00	00	1
30	1	11	01	01	1
31	1	11	10	10	1
32	1	11	11	11	1

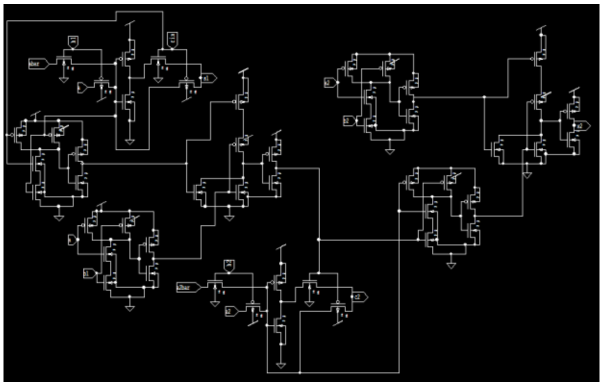


Fig -13: Circuit For Full Adder

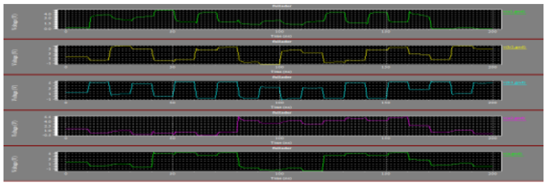


Fig -14: Ouput For Full AdderS1

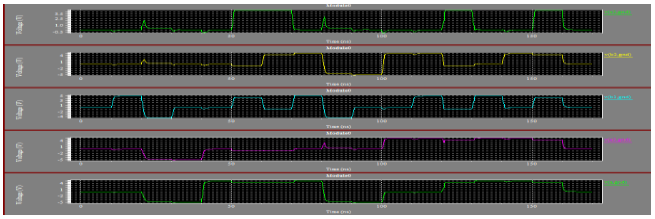


Fig -15: Ouput for Full AdderS2

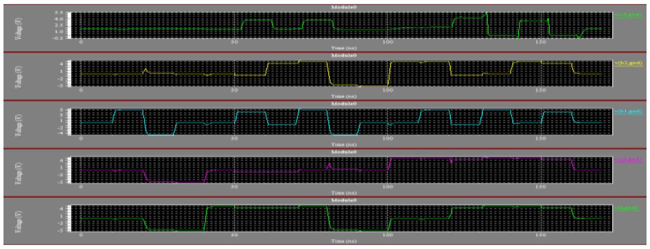


Fig -16: Ouput For Full Addercarry

3. DEFINE QUATERNARY TO BINARY ENCODING

Two output one is LSB another one is MSB and getting one output.Already known that two time inversions method after achieving the output.

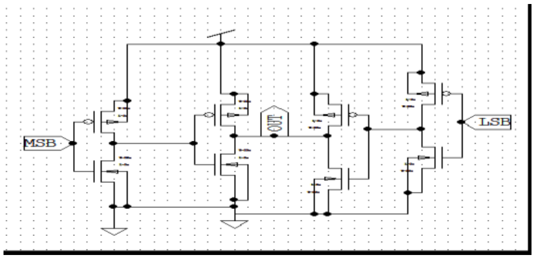


Fig -17: Quaternary to binary

4. DEFINE BINARY TO QUATERNARY DECODING

Separating the two type one is pullup and full down concept.b1 and b2 is pullup input and pulldown give to the clock,Clock is used to activate the pull down network.

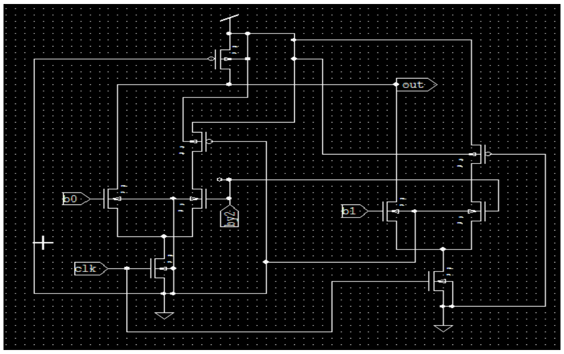


Fig 20: Binary To Quaternary Circuit

CONCLUSION

Hereby,wehavereportedaninnovativeQLUTdesignthatcanbeusedto quaternary bus model is superior to the binary. Adders are one of the important parts of the processing element and hence it has a focus of research. The designing of adders using QULT can prove to be very useful. Thus there is a need to design an optimal adder. In this task the Quaternary Logics based on OR logic and AND logics are designed. To encode and decode Quaternary to binary and binary to Quaternary is constructed respectively. Hence Quaternary adder is constructed based on lookup table. Thus it is investigated and analyzed different adder on the basis of different parameters such power and transistor count.while at the same time,achieving low power consumption.

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