Image Compression using High Efficient Video Coding (HEVC) Technique

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Abstract— ***the transformation of 2D-DCT is applied in video compression technique with 14 additions for area and power compaction. The proposed structure could be implemented in 4, 8, 16, 32 bit size. The proposed 2D-DCT system is used to reduce the complexity of video compression. It results in less area delay and power consumption with "0" and "1" by implementing in FPGA. HEVC/H265 is applied for enhancing good video quality during compression for higher pixel size and consumes only half the bandwidth of H264 for the same video quality.***

Keywords—*Area and Power efficiency, High Efficiency Video Coding/ H.265, Proposed 2D-DCT algorithm, FPGA.*

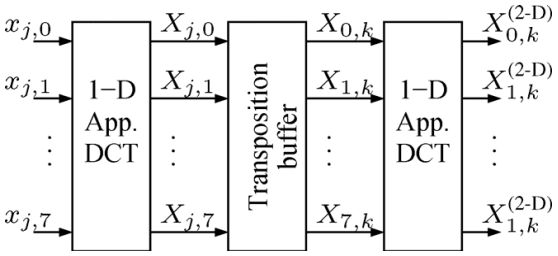
I. INTRODUCTION

The DCT approximation possesses an extreme low arithmetic complexity, require 14 addition operation. This proposed transform obtained by means of solving a customized optimization problem aiming at minimizing the transform computational cost and also propose Power and area for several 2-D8-point approximate DCT. The approximate DCT methods under consideration are (i) the proposed transform; (ii) the2008 Bouguezel-Ahmad-Swamy (BAS) DCT approximation (iii) the Cintra-Bayer modified (CB) 2011 approximate DCT based on the rounding-off function. All the implementations are sought to be parallel time multiplexed 2-D architectures for each 8*8 data blocks. Additionally, the designs are based on consecutive calls of 1-D architectures captivating advantage of the separability property of the 2D-DCT kernel. Designs were systematically assessed and compared. The digital hardware architectures and algorithms are used both for 1-D and 2-D analysis.

As a result, the two dimensional (2-D) version of the 8-point DCT was adopted in several imaging standards such as JPEG especially effective for high-resolution video applications .However, HEVC possesses a significant computational complexity in terms of arithmetic opperation. In fact, HEVC can be 2–4 times more computationally demanding when compared to H.264/AVC. Therefore, low complexity DCT-like approximations may benefit future video codes including emerging HEVC/H.265 systems.

II. DIGITAL ARCHITECTURES AND REALIZATIONS

In this section we propose architectures for the detailed 1-D and 2-D approximate 8-point DCT. We aim at physically implementing for various transformation matrices. Introduced architectures were submitted to (i) Xilinx FPGA implementations and (ii) CMOS 45 nm application specific integrated circuit (ASIC) implementation up to the synthesis level. This section explores the hardware utilization of the discussed algorithms while providing a comparison with the proposed novel DCT approximation algorithm and its fast algorithm realization. Our objective here is to offer digital realizations together with measured or simulated metrics of hardware resources so that better decisions on the choice of a particular fast algorithm and its implementation can be reached.

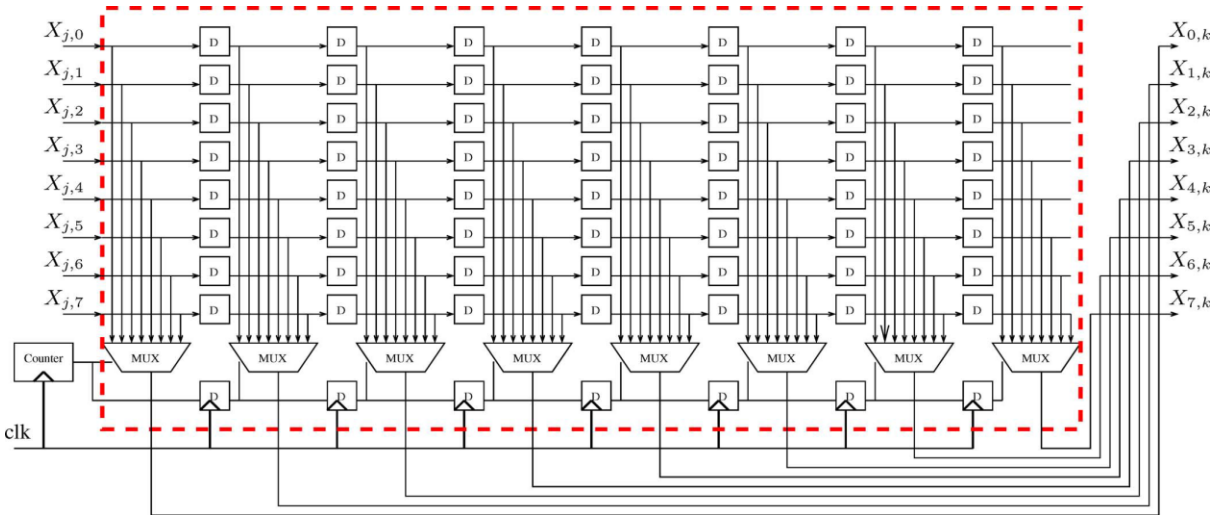


A. Proposed Architectures

We propose digital computer architectures that are custom designed for the real-time implementation of the fast algorithms. The proposed architectures employ two parallel realizations of DCT approximation blocks. The 1-D approximate DCT blocks implement a particular fast algorithm chosen from the collection described earlier in the paper. The first instantiation of the DCT block furnishes a row-wise transform computation of the input image, while the second implementation furnishes a column-wise transformation of the intermediate result. The row- and column-wise transforms can be any of the DCT approximations detailed in the paper. In other words, there is no restriction for both row- and column-wise transforms to be the same. However, for simplicity, we adopted identical transforms for both steps. Between the approximate DCT blocks a real-time row-parallel

transposition buffer circuit is required. Such block ensures data ordering for converting the row-transformed data from the first DCT approximation circuit to a transposed format as required by the column transform circuit. The digital architectures of the discussed approximate DCT algorithms were given hardware signal flow diagrams as listed below:

1) Proposed transform architecture
2) BAS2008 -architecture
3)CB2011-architecture



Details of the transposition buffer block.

The circuitry sections associated to the constituent matrices of the discussed factorizations are emphasized in the figures in bold or dashed boxes.

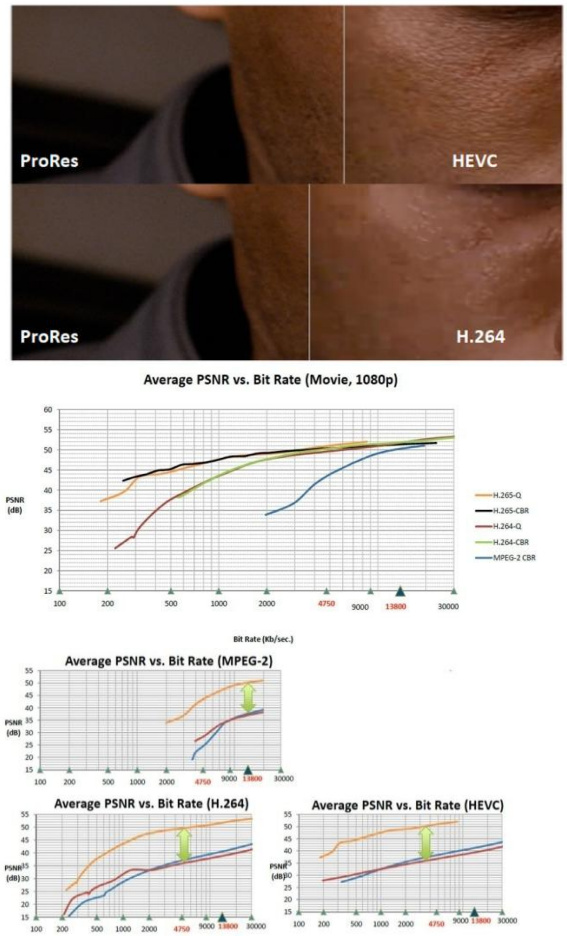
B. Xilinx FPGA Implementations

Discussed methods were physically realized on a FPGA based rapid prototyping system for various register sizes and tested using on-chip hardware-in-the-loop co-simulation. The architectures were designed for digital realization within the MATLAB environment using the Xilinx System Generator (XSG) with synthesis options set to generic VHDL generation. This was necessary because the auto-generated register transfer language (RTL) hardware descriptions are targeted on both FPGAs as well as custom silicon using standard cell ASIC technology. The proposed architectures were physically realized on Xilinx Virtex-6 XC6VSX475T-2ff1156 device. The architectures were realized with fine-grain pipelining for increased throughput. Clocked registers were inserted at appropriate points within each fast algorithm in order to reduce the critical path delay as much as possible at a small cost to total area. It is expected that the additional logic overheard due to fine grain pipelining is marginal. Realizations were verified on FPGA chip using a Xilinx ML605 board at a clock frequency of 100 MHz. Measured results from the FPGA realization were achieved using stepped hardware-in-the-loop verification .Several input precision levels were considered in order to investigate the performance in terms of digital logic resource consumptions at varied degrees of numerical accuracy and dynamic range. Adopting system word length , we applied 10 000 random 8-point input test vectors using hardware co-simulation. The test vectors were generated from within the MATLAB environment and routed to the physical FPGA device using JTAG based hardware co-simulation. JTAG is a digital communication standard for programming and debugging reconfigurable devices such as Xilinx FPGAs. Then the measured data from the FPGA was routed back to MATLAB memory space. Each FPGA implementation was evaluated for hardware complexity and real-time performance using metrics such as configurable logic blocks (CLB) and flip-flop (FF) count, critical path delay in ns, and maximum operating frequency in MHz. The number of available CLBs and FFs were 297,600 and 595,200, Quantities were obtained from the Xilinx FPGA synthesis and place-route tools by accessing the flow .results report file for each run of the design flow. In addition, the static and dynamic power consumptions were estimated using the Xilinx Power Analyzer

C. IMPLEMENTATION IN REAL TIME VIDEO COMPRESSION SOFTWARE

The proposed approximate DCT transform was embedded into an open source HEVC standard reference software in order to assess its performance in real time video coding. The
original integer transform prescribed in the selected HEVC reference software is a scaled approximation of Chen DCT algorithm, which employs 26 additions. For comparison, the proposed approximate DCT requires only 14 additions. Both algorithms were evaluated for

their effect on the overall performance of the encoding process by obtaining rate-distortion (RD) curves for standard video sequences. The curves were obtained by varying the quantization point (QP) from 0 to 50 and obtaining the PSNR of the proposed approximate transform with reference to the Chen DCT implementation, which is already implemented in the reference software, along with the bits/frame of the encoded video.



In these graphs of the average PSNR as a function of bit rate for the three codes, the orange line represents a news program, red is a movie, and blue is sports. As you might expect, news has the best PSNR at a given bit rate because there's not much motion, while sports performs the worst at low bit rates because of all the fast motion. Interestingly, all three codes exhibit a similar difference between content with slow and fast motion

III. CONCLUSION

In this project an 8 point DCT has been proposed. This DCT approximation requires only 14 addition operation. Because of that it can be implemented in digital VLSI, that use only 0's and 1's. Hence the new proposed Transform is the best DCT approximation in terms of Low computational complexity and high speed among other transform. By using that number of gate count and power also reduced. This widely used in image and video compression standards. Future work includes replacing the Free PDK standard cells with highly optimized proprietary digital system. Additionally, we intend to develop the approximate versions for the 4, 16, and 32 point DCT as well as to the 4-point discrete sine transform, which are discrete transforms required by HEVC.

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