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Design and Simulation of Power Optimized 8 Bit Arithmetic Unit using Gating Techniques in Cadence 90nm Technology

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Abstract - ***In present day technology, designing of low power systems has emerged as one of the important theme of electronic industries due to the fact that, power consumption is drawing much of the concentration in any very large scale integration (VLSI) chip design. In most of the electronic gadgets Arithmetic Unit (AU) is has become one of the basic elements due to fact that, calculation is required in almost all of the electronic systems. For this reason, power consumption of the AU forms a significant portion of the total power consumption of the system. So AU's power consumption has become one of the major concerns in designing any electronic portable devices. In existing AU, power supply and inputs are fed to all the modules irrespective of the required operation, as a result of which AU's power consumption increases. Hence there exists a need to reduce power consumption of AU. In order to meet this objective an 8 bit AU is designed by applying Gating techniques such as Power Gating and Input Gating, which reduces the power consumption. The traditional as well as power optimized 8 bit AUs are designed and simulated in cadence 90nm technology and it is found that the proposed AU has achieved 61% of power reduction compared to the traditional AU.***

Key Words: *VLSI, AU, Power Gating, Input gating*

1. INTRODUCTION

In any system ALU is the most important part of a processor as it is required even for calculating the address of each memory location. It performs particular arithmetic and logic operations on each set of operands, based upon the instructions given by the processor. In some processors ALU is split into two unit, an Arithmetic unit (AU) and logic unit (LU). Some processors possess a couple of Arithmetic units – one for the fixed point operations and another for the floating point operations. As AU operates at a very high speed and it is accessed by the system almost frequently, it contributes to one of the highest power-density locations on the processor. Because of this reason, there exist thermal hotspots and sharp temperature gradients inside the execution core, thereby reducing the reliability as well as battery life of the system. Therefore, there is a great need for the development of a power optimized AU design. This encourages powerfully for the design of a power optimized AU that satisfies the superior needs along with the reduction of average power consumption. The rest of the paper is organized as follows. Section 2 discusses the fundamentals of AU. Section 3 presents the methodology for developing a power optimized AU. Section 4 includes the Design and Simulation details of AU. Section 5 gives the Results and Analysis and Section 6 concludes the paper.

2. FUNDAMENTALS OF ARITHMETIC UNIT

An AU is designed in an order to perform the Arithmetic operations which are essential in most of the electronic devices. The arithmetic operations performed by the AU include addition, subtraction and multiplication. Since AUs are designed to carry out only the integer operations, they perform only the addition, subtraction and multiplication of any two integers, as their result is also an integer. But they do not handle division operation since its output may be a fraction. Therefore division operations are handled by the Floating Point Unit (FPU). This FPU also handles all other non-integer calculations. The *Fig.1* shows the architecture of an ALU.

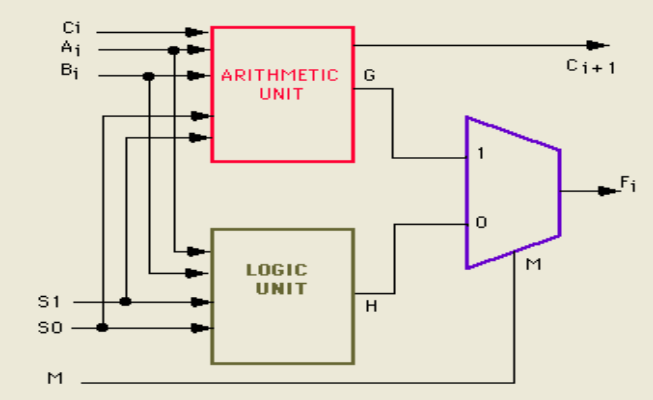

Fig - 1: Architecture of an ALU

It consists of two separate units to carry out arithmetic and logic operations. The unit that is built specifically for performing arithmetic operations is called as Arithmetic Unit and the unit that handles Logic operations is called as Logic Unit.

In this project first a traditional 8 bit AU is designed and then it is modified by applying the Power Gating and Input Gating techniques to build a power optimized 8 bit AU. The AU in this project is designed to perform the following arithmetic operations:

2.1. Addition

Addition is the most basic operation among all the arithmetic operations. Any component that performs addition operation is referred as an Adder. The function of this adder is to combine two numbers of the same length into a single quantity. These two numbers are called as addends whereas the resulting single quantity is called as the summation. It is also possible to add more than two numbers into a single quantity by means of repeated addition. For example,

0010(decimal 2) + 0111 (decimal 7) = 1001 (decimal 9)

2.2. Subtraction

Subtraction is also one of the most basic arithmetic operations performed by an AU. It is opposite to that of the addition operation because if we consider a binary number and then add any other number to that after which subtract the same number that we added then we will be left out with a single number that we started with. Usually subtraction is represented by a minus sign in infix notation. For example,

0111(decimal 7) - 0010 (decimal 2) = 0101 (decimal 5)

2.3. Multiplication

Multiplication is the second most important operation of an AU. It considers two binary numbers as its inputs and then produces a single quantity as their output. These two inputs are usually referred as multiplier and the multiplicand, sometimes both with no trouble referred to as factors and their resulting output is called as the product. In this paper a 4 bit Baugh-wooley multiplier is used because of its high performance applications. This Baugh-wooley multiplier consists of AND gates, half adder and full adders.

3. METHODOLOGY

The Methodology in this paper includes two power reduction gating techniques. They are,

1. Power gating.
2. Input gating.

3.1. Power Gating

In Power Gating, the power supply is controlled by feeding it through a pair of NMOS transistors, such that the VDD is fed through one NMOS transistor and GND is also fed through another NMOS transistor. The gate terminal of these both transistors is controlled by the ENABLE signal of that respective arithmetic module. That is power supply is provided only if the ENABLE signal is made HIGH otherwise the power supply is blocked for that module thereby reducing the static power consumption of all the modules whose operation is not required. The schematic of an Arithmetic module with Power Gating is as shown in *Fig. 2.*

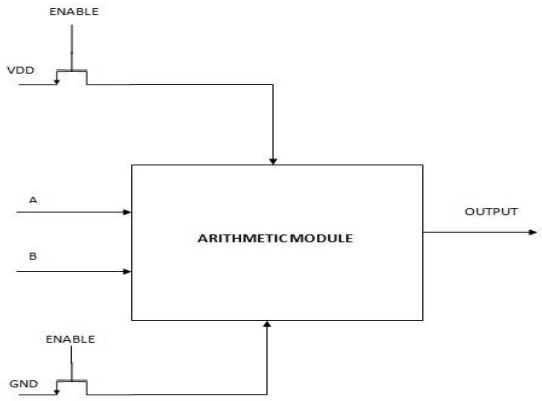

Fig - 2: Power Gating Technique

3.2. Input Gating

Similar to the Power Gating, in Input Gating, inputs are fed to only one block whose ENABLE signal is made HIGH. Otherwise the inputs for the modules are blocked thereby reducing the power consumption resulting from the un-necessary switching in the other blocks. The ENABLE signal of a block is made HIGH if and only if its operation is required. The schematic of an Arithmetic module with Input Gating is as shown in *Fig. 3.*

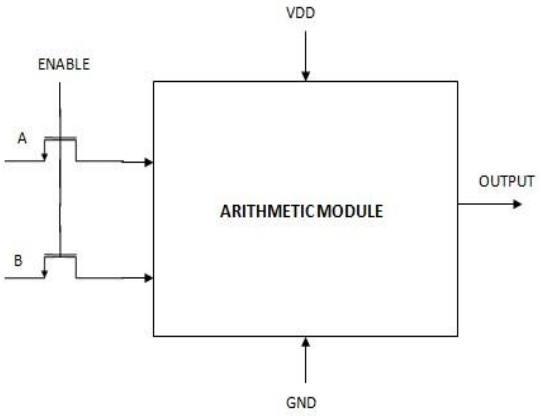

Fig - 3: Input Gating Technique

An example for combination of Power gating and Input gating using a single arithmetic block of an AU is as shown in *Fig. 4.* Here Power supply, input A and input B are fed by means of NMOS transistors whose gate is controlled by the ENABLE signal of that respective block.

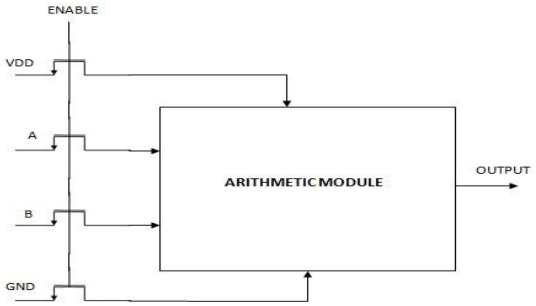

Fig - 4: Combination of Power Gating and Input Gating

If it is required to perform only the Multiplication operation, then the ENABLE signal of only the Multiplier is made HIGH whereas for Adder-Subtractor module the ENABLE signal is kept LOW in order to block the power supply and inputs to that module there by reducing un-necessary power consumption. The ENABLE signal is fed to the required module depending upon the select line value by using an additional 1:2 DEMUX.

4. DESIGN AND SIMULATION OF AU

In this paper an 8 bit traditional AU is built first and then it is modified by applying Power and Input gating techniques to achieve a proposed power optimized 8 bit AU.

4.1. Traditional 8 Bit AU

In order to build an 8 bit traditional AU, an 8 bit adder /Subtractor module is used. This circuit can perform both addition and subtraction operations depending upon the control signal (M) received from the control unit. If the control signal (M) is LOW then addition is performed and if control signal (M) is HIGH then subtraction is performed. The schematic view of adder/Subtractor module is as shown in *Fig. 5.*

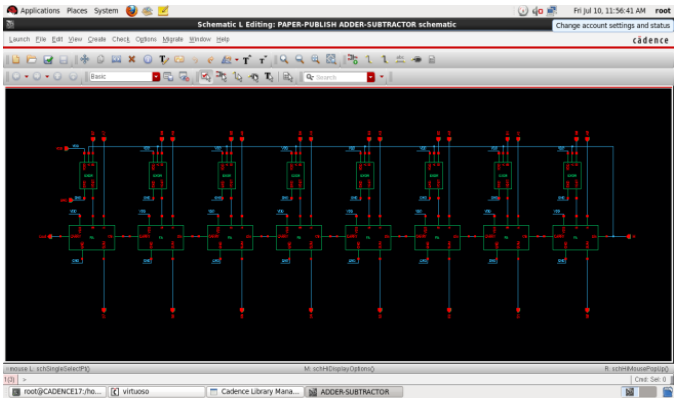

Fig - 5: Adder/Subtractor

The 4 bit Bough-Wooley multiplier is used to carry out multiplication operation which is as shown in *Fig. 6.*

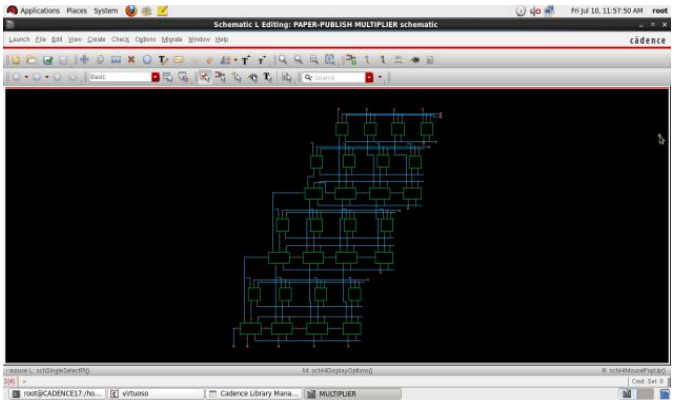

Figure 6.Bough-Wooley Multiplier

Multiplexer is the most important element in an AU. It selects any one output among two outputs generated from an AU depending upon the select line value and then reproduces it at the output terminal. Since it is a complex circuit, it consumes a lot of power in an AU. So in order to reduce its power consumption a Pass Transistor Logic (PTL) based multiplexer as shown in *Fig. 7* is used in this paper.

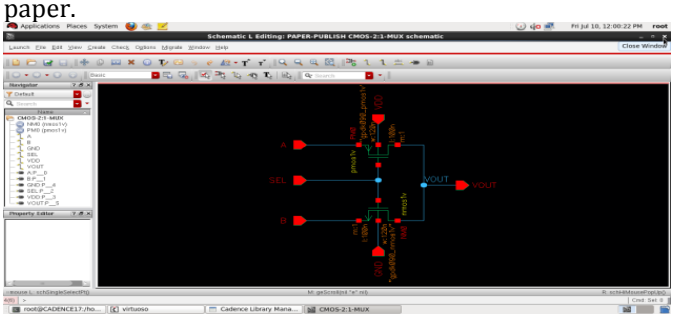

Fig - 7: PTL based 2:1 MUX

The complete schematic view of an 8 bit traditional AU is shown in *Fig. 8*. It consists of an 8 bit Adder/Subtractor, 4 bit Multiplier and an 8 bit 2:1 multiplexer.

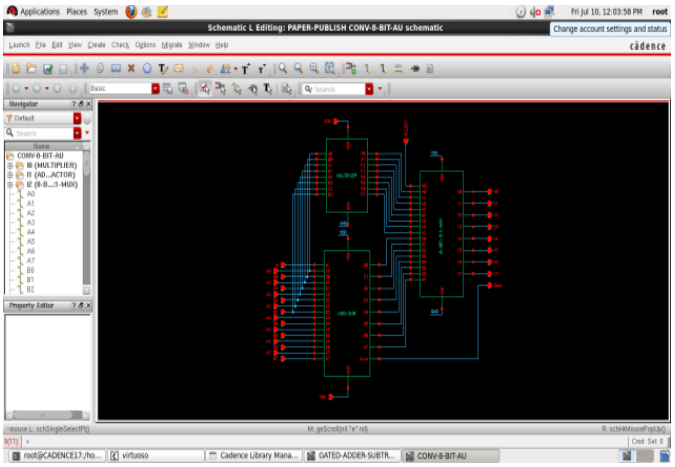

Fig - 8: Traditional 8 bit AU

The resulting simulation waveform of traditional AU for 1 bit operation is as shown in *Fig. 9.*

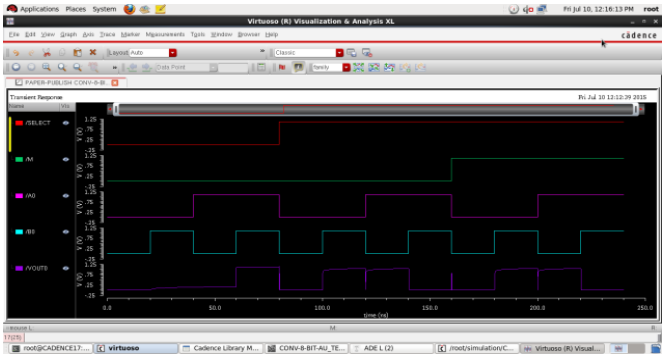

Fig - 9: Simulation Waveform of Traditional AU

4.2. Proposed 8 Bit AU

The proposed AU includes an additional 2T 1:2 DEMUX to route the ENABLE signal to the required module. It is built using PTL as shown in *Fig. 10.*

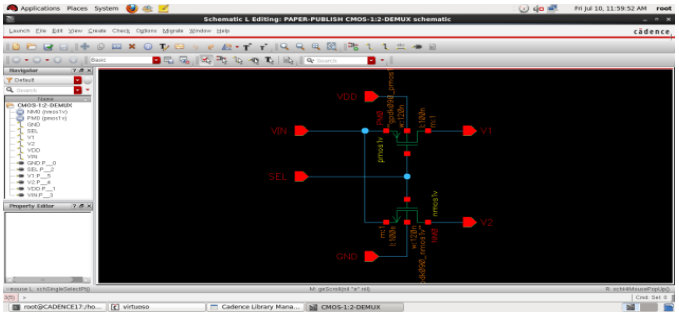

Fig - 10: PTL based 1:2 DEMUX

The schematic view of proposed power optimized 8 bit AU is shown in *Fig. 11.*

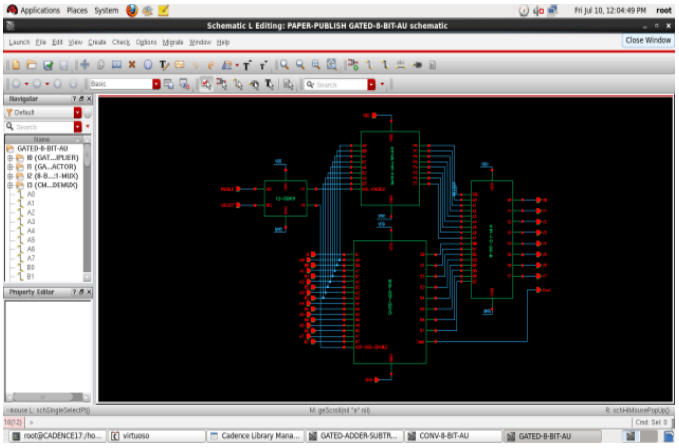

Fig - 11: Proposed 8 bit AU

The simulation waveform of power optimized AU for 1 bit operation is shown in *Fig. 12*. The output waveform is similar to the traditional AU waveform with some logic level degradation which can be overcome by employing buffer circuit at the output terminal.

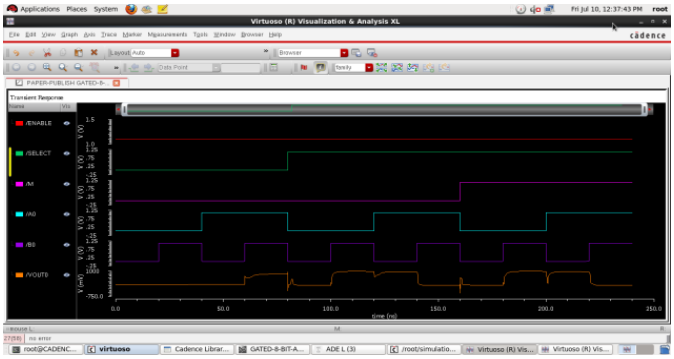

Fig - 12: Simulation Waveform of Proposed AU

5. RESULTS AND ANALYSIS

This complete project is designed and simulated using cadence 90nm technology. The basic gates and basic modules of the architecture have been designed, simulated and verified. In this paper, after designing and simulating an 8 bit traditional as well as Proposed AU, the average power consumption values obtained for each AU operation are as listed in *Table. 1.*

Table -1: Average Power Comparison

AU operation	Traditional AU(µW)	Proposed AU(µW)
Addition	16.31	6.93
Subtraction	17.03	7.13
Multiplication	16.33	5.10

By observing the average power consumption values from the above table, it can be noticed that the power consumption has been reduced for an AU with Power and Input Gating when compared to the traditional AU. The power consumption of an 8 bit Proposed AU is reduced by 61% when compared to the traditional 8 bit AU.

6. CONCLUSION

In this paper a traditional 8 bit AU is designed and then verified for its functionality by simulating it using cadence virtuoso ADE spectre. The proposed 8 bit AU with Power and Input Gating is also designed and verified for its functionality. It is found that both the simulation results are almost similar with some output degradation for the proposed AU which can be overcome by employing buffer circuit at the output terminal. The power is measured for the obtained output waveforms of both the AUs using Cadence Virtuoso ADE Visualization Analysis, XL Browser and XL calculator. Here it is found that the power has been reduced by 61% in an 8 bit AU with Power and Input Gating when compared to the traditional 8 bit AU.

REFERENCES

[1] P. Kalyani , Dr. P. Satishkumar , Dr. K. Ragini-"Various Low Power Techniques for CMOS Circuits", P. Kalyani et al Int. Journal of Engineering Research and Applications, ISSN : 2248-9622, Vol. 3, Issue 6, Nov-Dec 2013, pp.330-333

[2] Akhila Abba , K Amarender" Improved Power Gating Technique for Leakage Power Reduction" International Journal Of Engineering And Science Vol.4, Issue 10 (October2014), PP 06-10

[3] Pramod Kumar. M .P, A. S. Augustine Fletcher" A Survey on Leakage Power Reduction Techniques by Using Power Gating Methodology" International Journal of Engineering Trends and Technology (IJETT) – Volume 9 Number 11 - Mar 2014

[4] Ping Huang, Zuocheng Xing,Tianran Wang,Qiang Wei, Hongyan Wang, Guitao Fu" A Brief Survey on Power Gating Design" School of Computer, National University of Defense Technology, Changsha 410073, China

[5] Indrayani Patle, Akansha Bhargav, Prashant Wanjari," Implementation of Baugh-Wooley Multiplier Based on Soft-Core Processor" IOSR Journal of Engineering (IOSRJEN) e-ISSN: 2250-3021, p-ISSN: 2278-8719 Vol. 3, Issue 10 (October. 2013), ||V3|| PP 01-07

[6] "Adder Subtractor Design" Islamic University of Gaza, Faculty of Engineering Department of Computer Engineering Fall 2011 ECOM 4113: Digital Design LAB Eng. Ahmed Abumarasa

[7] Sreenivasa Rao N,Y. Vishnuvardhan Reddy, G.Shivamanikanta, B. Vijaysree "Design the 2X1 MUX with 2T Logic and Comparing the Power Dissipation and Area with Different Logics" International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering Vol. 4, Issue 3, March 2015

BIOGRAPHIES

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