Evaluation path way of Schmitt Trigger with Leakage Reduction Techniques

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Abstract - *The presented report provides detail study of Schmitt trigger circuit. Schmitt trigger is mainly use in wave shaping and communication systems for cleaning the wave. We are working in 90nm technology, so area is reduced and leakage power is increase. To overcome this problem, we are applying leakage reduction techniques (MTCMOS & VTCMOS). Simulation has been done on MATLAB tool with enhance performance parameter of Schmitt trigger i.e. leakage power (1.4pW), dc response [i/p (M16.16V, 6.16V), o/p (5.39V,1.554V)],transconductance(6.72x10^14siemens, Tranresistance (3.075x10^11ohm), Hysteresis (1.31V) at supply voltage (Vdd = 0.7V).*

Key Words: leakage power; dc response; MAT LAB tool; transconductance; Tranresistance; Hysteresis.

1. INTRODUCTION

Schmitt trigger is important part of communication system applications to filter out any noise present on a signal path and Produce a clean digital signal [5]. Schmitt trigger blocks find their way into many instrumentation and test measurement systems [13].Schmitt trigger has **important parameter like hysteresis width (ΔH)**, in which the input threshold changes depending on whether the input is rising or falling [11]. The fundamental idea of a Schmitt trigger is to create a bi-stable state which has a switching threshold as a function of the direction of the input [96], with recent advance of technology reduction of power supply Vdd has become vital to reduce active power and to ignore reliability problems in Deep sub-micron (DSM) regimes. On other hand, reduction in Vdd **creates serious degradation in circuit's performance [16].** The power consumption has become an imperative consideration due to increased integration, operating speeds and the quick-tempered growth of battery operated appliances [31], One way to manage the performance is to scale down both threshold voltage Vth and Vdd supply voltage, so the reducing the Vth causes the subthreshold leakage current exponentially [40], [94]. This type of problem creates in DSM technologies. Multi threshold CMOS (MTCMOS) and virtual threshold CMOS (VTCMOS) technology have emerged as increasingly popular techniques to reduce leakage current/power and improve the circuit parameters. In 2nd section circuit

description (4T Schmitt trigger) & reduction techniques have been presented. 3rd section provide simulationresult on MATLAB tool. 4th section describes the summary of reported work.

2. CIRCUIT DESCRIPTION

2.1 4T Schmitt Trigger

The presented circuit is formed by a combination of one PMOS (P1) and three NMOS (N1, N2 and N3), there is no straight connection between supply voltage (Vdd) and ground (Vss) as PMOS is connected to power supply and Schmitt trigger output [96], on other hand NMOS is connected to output and ground node.
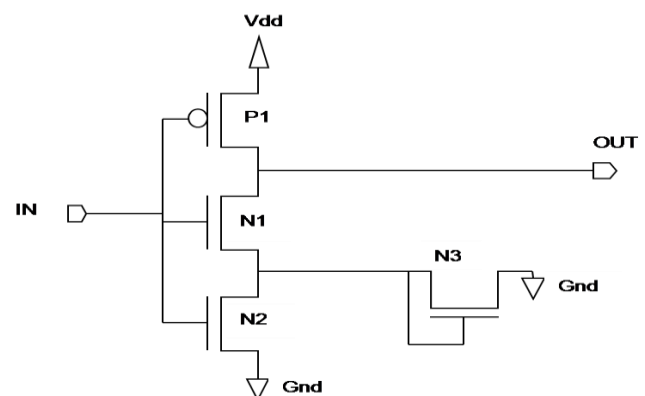

Fig -1: Circuit diagram of the 4T Schmitt trigger.

There is no static power due to any direct connection between power supplies (Vdd) to be ground (Vss) [19].
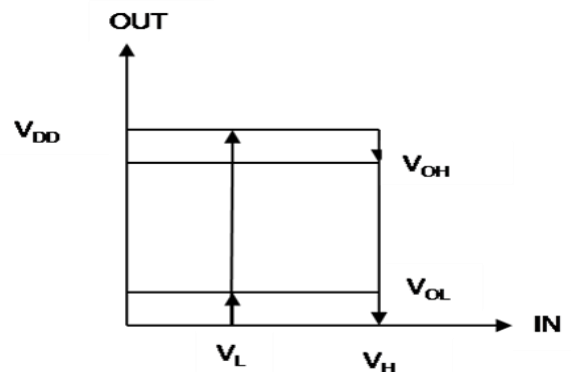

Fig -2: Shows transfer curve of the 4T Schmitt trigger.

Figure 2, waveform shows the transfer characteristic of the 4T Schmitt trigger at 0.7V power supply.
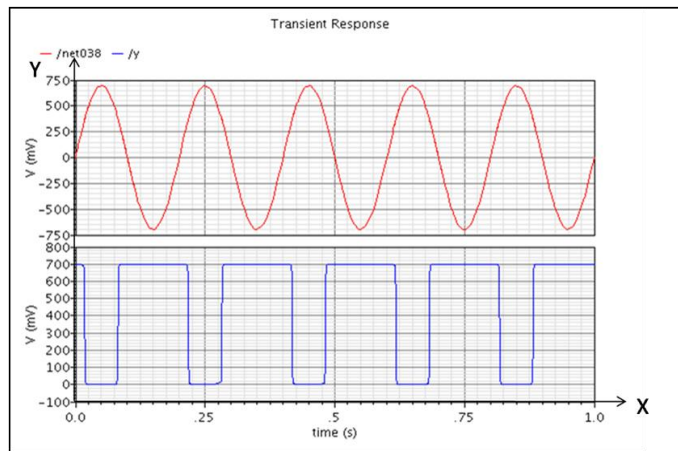

Fig-3: Show input-output Characteristics of the 4T Schmitt trigger.
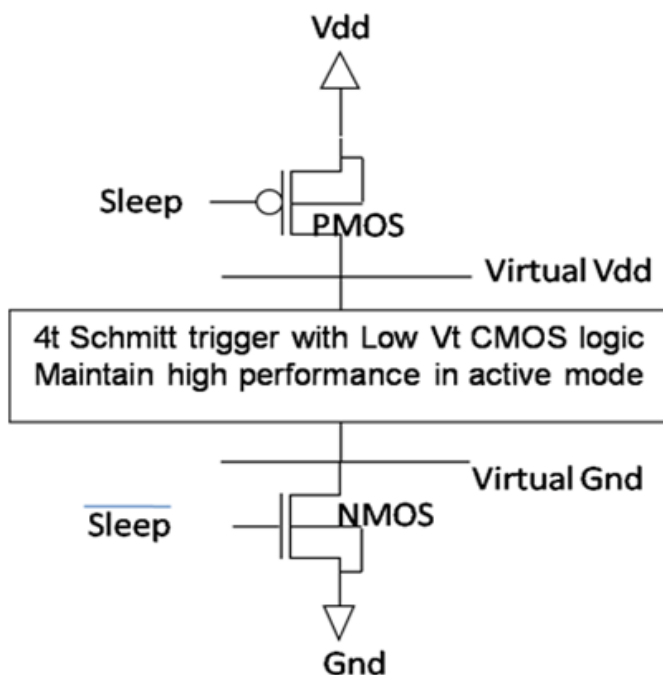
2.2 4T Schmitt trigger with MTCMOC

Fig-4: Shows the circuit diagram of 4T Schmitt trigger with MTCMOS technique

Power Supply and threshold voltages are condensed with the scaling of CMOS technologies. Reduction in threshold voltage leads to an increase the sub threshold leakage current. In modern electronics design, high performance integrated circuits (ICs), more than 50% of the total on mode energy can be dissipated due to the leakage power, with more transistors integrated on-chip, leakage currents will rapidly govern the total power consumption of high performance ICs. A more popular low leakage circuit technique is the Multi threshold Voltage CMOS (MTCMOS).

4T Schmitt trigger with MTCMOS provided reduction technique for leakage power.

2.3 4T Schmitt trigger with VTCMOS

Very recently in communication system, a new practical CMOS device called Variable Threshold Voltage MOSFET (VTCMOS) has promised to be amongst the after that generation of ultra-low power circuits operating at low power supply [34]. The basic principle of VTCMOS is that its threshold voltage (Vth) is forbidden by the applied substrate bias ($-|Vbs|$), leading to low off state current or higher active on-current. The Vth shift is given as: $\Delta Vth = \gamma |Vbs|$ where γ is the body effect factor [48]. The most favorable function of the circuit is to successfully reduce the stand-by off-current keeping high active on-current,or to enhance the active on-current keeping-
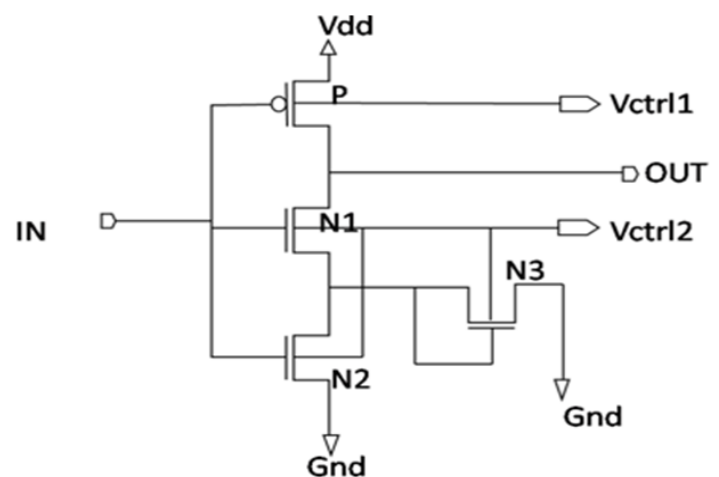

Fig-5: Show the circuit diagram of 4T Schmitt trigger with VTCMOS technique.

- low stand-by current, both of which are indispensable for obtaining high-speed low-power performance.

3. SIMULATION RESULTS

Simulation of Schmitt trigger has been done on 90nm CMOS technology and improved circuit parameters. The gate leakage being the only dominant mechanism at room temperature, MTCMOS method suppresses the total leakage of 4T is 1.64nW, on other hand VTCMOS scheme provides a leakage power reduction of 47.8% and hysteresis width in VTCMOS is 1.58V better than MTCMOS technique.

3.1 Active power

This power consumption during when Schmitt trigger is on state. Basically active power is estimated by giving input voltage and calculating the average power consumption. The simulation time for calculate active power is 100ns. The active power is combination of dynamic and static power consumption. As shown in table 2 MTCMOS and VTCMOS have been compared to basic

structure of Schmitt trigger and provided effective reduction in active power with VTCMOS and MTCMOS (1.42µW).

Table 1: Shows the table of Active power

Voltage	4T Schmitt trigger	Schmitt trigger with MTCMOS	Schmitt trigger with VTCMOS
0.7V	2.36mw	1.50µw	1.42µw
0.8V	3.16mw	1.82µw	1.53µw
0.9V	5.69mw	3.69µw	2.36µw
1.2V	8.25mw	5.37µw	4.02µw

3.2 Leakage power

Leakage power provide off state power of any device, Leakage current, which can arise from sub-threshold and substrate injection effects [16], [94]. It is wastage of power supply and leakage power of Schmitt trigger is given by as

$$P_{LEAK} = I_{LEAK}.V_{dd} \qquad (1)$$

Table 2: Leakage power analysis

Voltage	Schmitt trigger	Schmitt trigger with MTCMOS	Schmitt trigger with VTCMOS
0.7V	1.36µw	1.64nw	1.4pw
0.8V	2.56µw	2.7nw	3.79pw
0.9V	4.19µw	4.9nw	7.43pw
1.2V	7.15µw	6.12nw	9.23pw

Leakage power of 4T Schmitt trigger =1.36µW, Leakage power of 4T Schmitt trigger with MTCMOS =1.64nW, Leakage power of 4T Schmitt trigger with VTCMOS=1.4pW Mainly reduction in leakage power of Schmitt trigger with VTCMOS is 47.8% in comparison to MTCMOS technique Above table 2, shows the leakage power description of 4T Schmitt trigger, 4T Schmitt trigger with MTCMOS & VTCMOS techniques in 90nm technology with Vdd=0.7V.
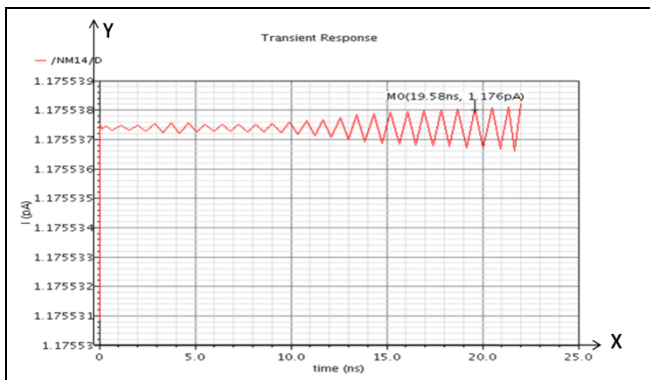

Fig -6: Show the leakage current waveform of schmitt trigger.

Figure 6, shows the leakage current waveform of 4T Schmitt trigger at input voltage is 0.7V with 19.5ns delay time.

3.3 Hysteresis width

Hysteresis is the property of quality of the Schmitt trigger, in which the input threshold changes depending on whether the input is rising or falling [54]. Hysteresis width **is given by ΔH, On another way hysteresis is the difference** between the input signal level at which a Schmitt trigger is standby mode and active mode (OFF and ON state)

$$\Delta H = V_H - V_L \qquad (2)$$

$$V_H = 2.54V, \ V_L = 1.23V, \ \Delta H = 1.31V \qquad (3)$$

Above equation shows the hysteresis width of Schmitt trigger 1.31V at input voltage (0.9V).
Where VH is upper threshold voltage and VL is lower threshold voltage.

Table 3: Hysteresis analysis

Voltage	4T Schmitt trigger	Schmitt trigger with MTCMOS	Schmitt trigger with VTCMOS
0.7V	5.23mv	2.54v	5.16v
0.8V	4.13mv	1.794v	3.54v
0.9V	2.16mv	1.65v	1.31v
1.2V	1.05mv	0.58v	1.02v

Above table 3, shows the hysteresis width of 4T Schmitt trigger with MTCMOS and VTCMOS, and VTCMOS provide wider hysteresis width.

3.4 Transconductance

Transconductance is the ratio of current change at output terminal to the voltage change at input terminal and abbreviate as gm, Transconductance is represented in the mathematical form is as follows;

$$g_m = \frac{\Delta I_{out}}{\Delta V_{in}} \qquad (4)$$

Table 4: Transconductance analysis

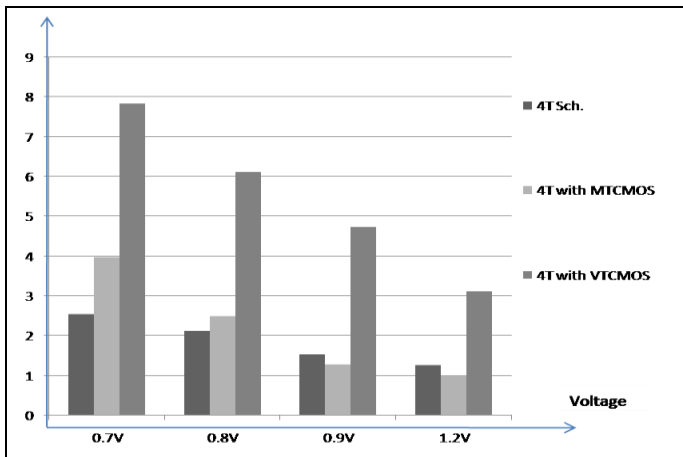| Voltage	4T Schmitt trigger	Schmitt trigger with MTCMOS	Schmitt trigger with VTCMOS
0.7V	2.54x10^-12	3.97x10^-14	7.84x10^-14
0.8V	2.12x10^-12	2.49x10^-14	6.12x10^-14
0.9V	1.53x10^-12	1.28x10^-14	4.73x10^-14
1.2V	1.26x10^-12	1.01x10^-14	3.12x10^-14

Fig -7:Show the greph of transconductance of schmitt trigger in Vdd 0.7V.

3.5 DC Response

DC Response is the ratio of o/p voltage to i/p voltage for the circuit.

$$DC\ Response= Vout/Vin \qquad (5)$$

DC Response waveform of Schmitt trigger at 0.7v supply voltage is at input Mi (6.163V, 6.163V) and o/p Mo (5.39V, 1.55V).
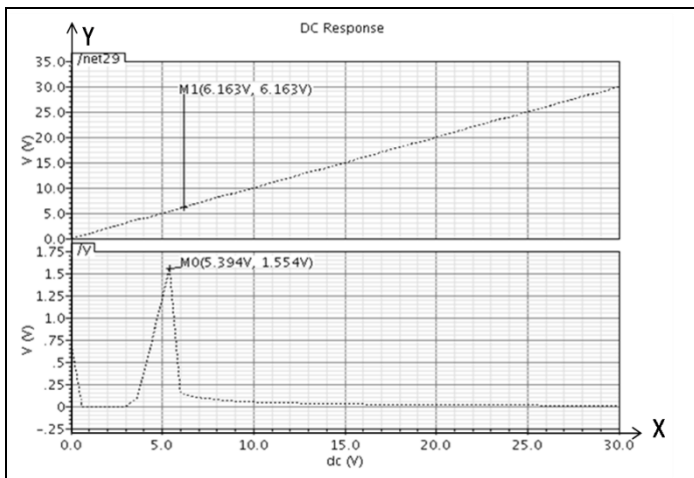

Fig -8: Show the greph of DC response.

Above figure 8 shows input-output DC response waveform of 4T Schmitt trigger in 90nm technology with Vdd = 0.7V.

3.6 Efficiency

Efficiency is providing the capacity of any circuit. High efficiency means fewer power drains and the input supply and fewer temperature buildups, allowing for small lighter power supplies and structure enclosures. Efficiency is meanly measured as

$$Efficiency= (output\ value/input\ value)*100 \qquad (6)$$

Efficiency using MTCMOS technique =63.06%   (7)
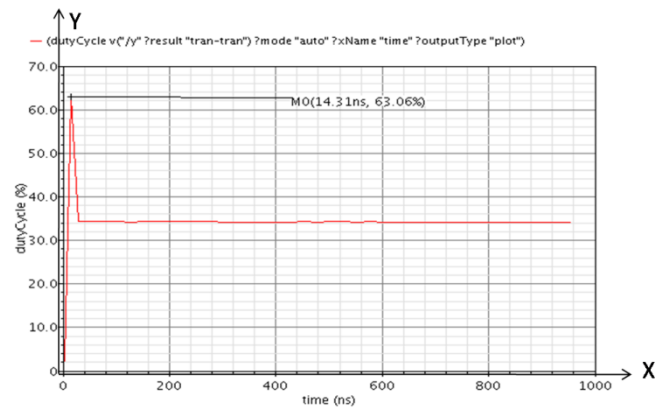
Efficiency using VTCMOS technique = 76.84%   (8)

Fig -9: Effeciency factor in Schmitt trigger with MTCMOS

Figure 9 shows the duty cycle of Schmitt trigger with MTCMOS and figure 11 is shows the efficiency of Schmitt trigger with VTCMOS when the input voltage rises from 0.7V to 1.2V.
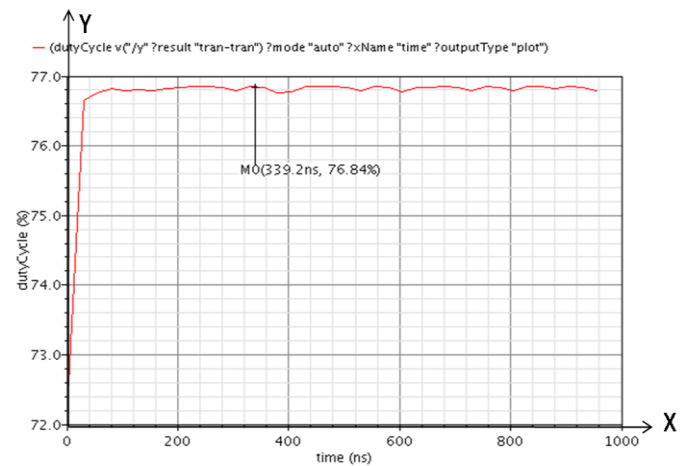

Fig -10: Effciency in schmitt trigger with VTCMOS

4. SUMMARY

Schmitt trigger have been simulated on MATLAB spectre tool in 90nm technology with MTCMOS and VTCMOS technique for enhancing the circuit parameter. Schmitt trigger is basically used in oscillator and wave shaping digital & analog communication circuits. In this discussion comparative description of MTCMOS and VTCMOS have been presented on the bases of min leakage power (1.4pW), max hysteresis width (1.31V), transconductance (3.97×10^{-14}s) and tranresistance (3.075×10^{11}ohm) at supply voltage Vdd=0.7V and threshold voltage (0.35V). Simulation result provides Schmitt trigger with VTCMOS is better than MTCMOS technique with little propagation delay in (fsec).this type of design is using in low power communication systems.

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