International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 02 Issue: 04 | July-2015 www.irjet.net p-ISSN: 2395-0072

Comparative Performance Analysis of Different Flip Flop Configurations

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Abstract - *Computer performance is increasingly limited by the performance of memory systems due to the fact that the rate of memory system performance increase has lagged the rate of processor performance increase in the past years. In other to bridge this gap, the computer memory is methodically examined from the transistor level to the memory element (Flip Flop) level using a robust methodological research process that provides a systematic approach/technique in comparing the performance of conventional Flip Flops to a Flip Flop known as Flip Flop Extension. Since the ultimate metric of memory system performance is related to how fast it can service critical requests from processors; the rationale used to justify the focus of this study is that by improving the memory elements (cells) used for designing Computer Dynamic Random Access Memory (DRAM), the average request service time can be reduced. This study shows remarkable performance improvement on high capacity of computer memory with the developed Flip Flop Extension when compared to the conventional Flip Flops. This study is therefore dedicated to the investigation of the existing conventional Flip Flops performance comparison to a Flip Flop Extension that is capable of being selected for the purpose of reading from and writing into it. This paper presents two models of comparison analysis frameworks known as Decision Tree and Propagation Time to examine and evaluate the significant performance advantages of the Flip Flops Extension at 87.5% active states utilization over conventional Flip Flops at 50% and 75% active states utilization respectively.*

Key Words: Active State Utilization, Dynamic Random Access Memory, Rapid Miner Model, Propagation Time and Average Request Service Time.

1. MEMORY PERFORMANCE ANALYSIS

The importance of memory system performance as a limiter of computer system performance cannot be over looked as is widely recognized worldwide [38]; [26] and [28]. It is quite obvious that memory devices are specifically designed by engineers whose predominant concerns are those of cost minimization and functional correctness but not necessarily speed enhancement. As a result, the topic of memory system performance analysis is important not only to system architects, but it is also needed by memory design engineers to evaluate design trade-off points of the various features that make up the memory system against potential performance benefits of those features.

Figure 1.1 shows that while memory device datarate have doubled every three years in between 1998 and 2004, row cycle times have decreased by roughly 7% per year during the same time period ascertained [53].

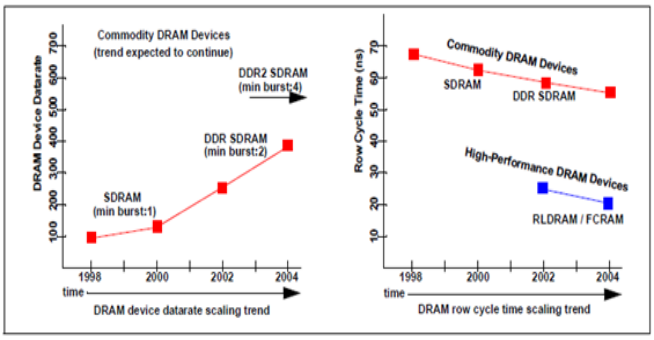


Figure 1.1: Memory Data rate and row cycle time scaling trends between 1998 -2004, (Wang, 2005).

The difference in the scaling trends means that each generation of memory devices has a different combination of data rate and row cycle time. As memory device density doubles with each generation, design engineers may choose to double the number of cells per row, double the number of rows in each bank, or double the number of banks within a given memory device. These doubling process add on to the propagation delay of the entire memory device system. Though doubling of the number of banks has the smallest impact on memory device timing parameters, but the increase in bank count increases the complexity of the control logic, and the larger number of logic transistors increases die size [53].

The different combinations of device datarates, row cycle times, and device organization impact for each generation of

memory devices lead to the situation that each generation of memory devices must be re-examined in terms of performance characteristics in the context of the larger memory system. Hence, a re-design of the existing conventional memory element known as Flip Flop to achieve Flip Flop Extension is of paramount importance if memory performance is to be evaluated at par with its processor counterpart for enhance computer performance.

2. MEMORY PERFORMANCE EVALUATION FRAMEWORKS

Two types of analytical frameworks are used to evaluate the performance of memory systems. These are Close-loop execution based [47]; [8] & [9] and trace based [17] analytical frameworks. The use of execution based simulations means that the performance of the memory system is impacted by the request rate of the processor or processors, and the performance of the memory is tightly coupled to the performance of the processor or processors. In this manner, execution based simulation frameworks can accurately measure computer performance sensitivity to memory device parameters for specific computer configurations. This ironically presents a problem in that the overall computer performance depends on both processor performance and memory performance. Meaning the individual contributions of processor performance and memory performance are difficult to separate out from each other.

On the other hand, the trace based analytical frameworks differ from execution based analytical frameworks in that trace-based are open-loop systems and memory system performance can be separated from processor performance. The use of an open-loop trace-based analytical framework means that the input request rate can be independently controlled. In this manner, a trace based analytical framework can measure the limits of performance sensitivity to individual memory system configuration and timing parameters.

The trace based analytical framework is deficient in some ways while it is advantageous in other ways when it is compared to an execution driven analytical framework in that memory address traces do not contain information in regards to dependencies in the memory request stream. The result is that even inherently dependent memory references can be collapsed entirely and the analytical framework can compute higher bandwidth efficiency than the theoretical bandwidth efficiency of the workload running on an infinitely fast processor. This is evidence in analyzing memory performance in terms of citations that were reviewed in previously published literatures [47]; [17]; [8] and [9]. However, a comparable framework in the work performed independently [38] and presented in a tutorial session at High-Performance Computer Architecture (HPCA) shared similarities fundamental methodology with the Request Access Distance methodology. But due to the fact that the underlying framework for the results presented in the tutorial was not disclosed, a direct comparison against the Request Access Distance analytical framework was not possible. This issue can be resolved by using an execution based analytical framework that uses highly accurate models of the processors and the memory system.

However, an execution based is also problematic [47]; [8] & [9] in that the processor state machine is dramatically more complex than the memory system state machine, and the vast majority of the simulation cycles are used for processor state simulation. Moreover, that problem is exacerbated when the goal of the simulation is to examine fundamental limitations of the memory system.

3. FLIP FLOPS AS MEMORY ELEMENTS

Flip Flops are sequential digital circuits that hold (remember) logic values. The ability of computer systems to operate without the continuous human intervention is solely achieved through sequential logic circuits known as Memory Elements [37].

In earlier computers, the most common form of random-access storage for computer main memory employed an array of doughnut-shaped ferromagnetic loops referred to as *cores.* The basic element of a semiconductor memory is the memory cell (appropriately gated-Flip Flop). Although a variety of electronic technologies are used, all semiconductor memory cells share certain properties and characteristics, some of which are as follows;

i. Exhibit two stable (or semi-stable), self-maintaining states that are used as storage/ memory elements capable of storing a binary digit (1 and 0).
ii. Capable of being written into (at least once), to set the state.
iii. Capable of being read to sense the state.
iv. Derived from Sequential Logic Circuits which are the main electronics circuits that make the development of computers possible.
v. Have three transition states known as Resting, Forbidden and Active states with four possible binary combinations of input variables [50].

Figure 1 depicts the operation of a memory cell. Most commonly, the cell has three functional terminals capable of carrying an electrical signal.

i. The select terminal, as the name suggests, selects a memory cell for a read or write operation.
ii. The control terminal indicates read or write.
iii. The other terminal provides an electrical signal that sets the state of the cell to 1 or 0 for writing, while when reading, the terminal is used for output of the cell's state [50].

The details of the internal organization, functioning, and timing of the memory cell depend on the specific integrated

circuit technology used and are outside the scope of this research work.

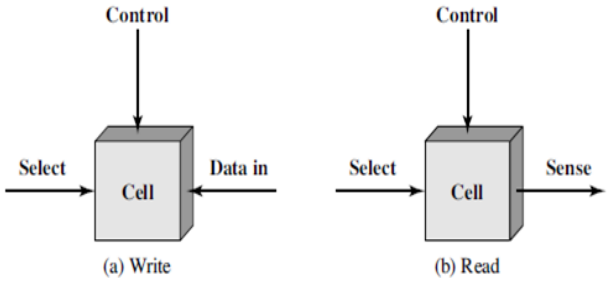


Figure 1: Memory Cell (Flip-Flop) Operation (Stallings, 2010)

Among the four known Flip Flops ever designed (SET/RESET, D-Type, JK and T-Type), the JK types are the most widely used for digital storage unit [43]. The behavior of a particular type can be described by what is termed the characteristic equation, which derives the "next" (i.e., after the next clock pulse) output, $Q_{next,}$ (Q_{n+1}) in terms of the input signal(s) and/or the current output, Q [39]. The basic memory cell is a Flip-Flop adequately gated. The writing (W) into the memory which requires select (S_e) and data (I) with the previous output of the different Flip Flops will determine the input combinations as presented in the various Flip Flops Combination Tables on data analysis characteristics of the different flip flops [34] & [35]. A Decision Tree analysis from Rapid Miner Model will be used to determine the degree of performance of the conventional Flip Flops in comparison to that of the designed Flip Flop Extension [34] and [35].

4. PERFORMANCE OF THE DIFFERENT FLIP-FLOP CONFIGURATIONS USING DECISION TREE OF RAPID MINER MODELS

From the findings and analysis of data presented in [34] anf [35] on all the different Flip-Flops that can be used to build Storage Devices, it is evident that the proposed Flip Flop Extension has higher speed performance over the conventional Flip Flops judging from Decision Tree of Rapid Miner Models. The analysis carried out on the different Flip Flops using the Decision Tree model is as shown in Tables 1.2(a) to (d).

Table 1.2(a): Decision Tree Table for Conventional SR-FF at 50% Active States Utilization

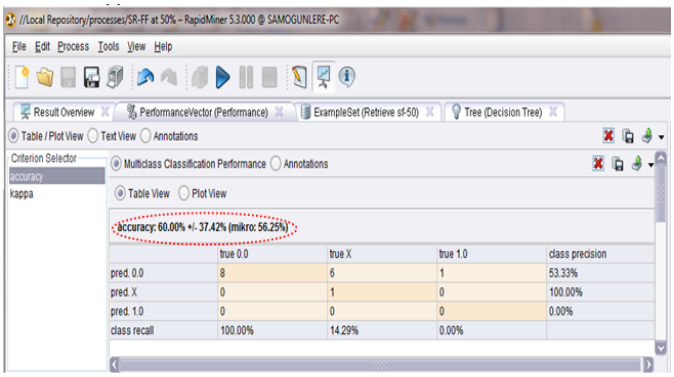


Table 1.2(b): Decision Tree Table for Conventional JK-FF at 75% Active States Utilization

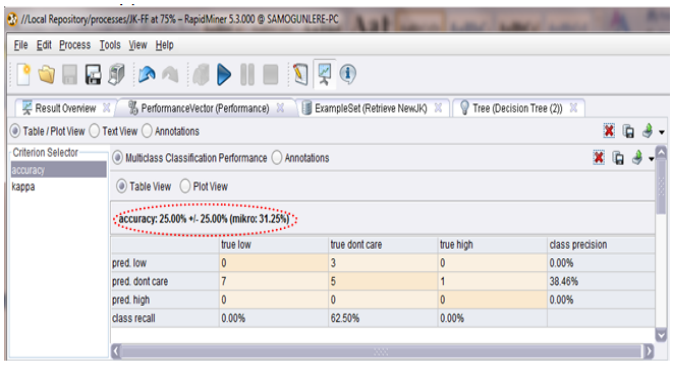


Table 1.2(c): Decision Tree Table for JK-FF Extension-0 at 87.5% Active States Utilization

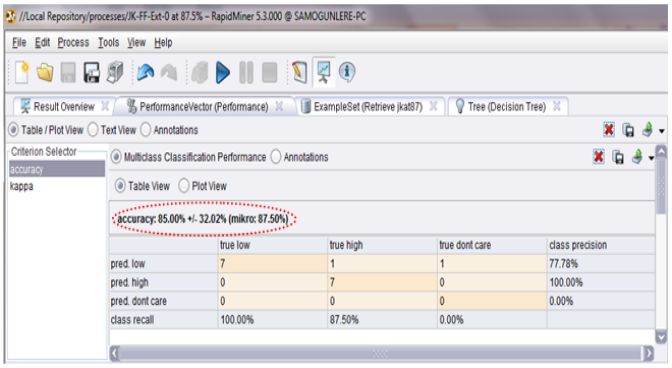
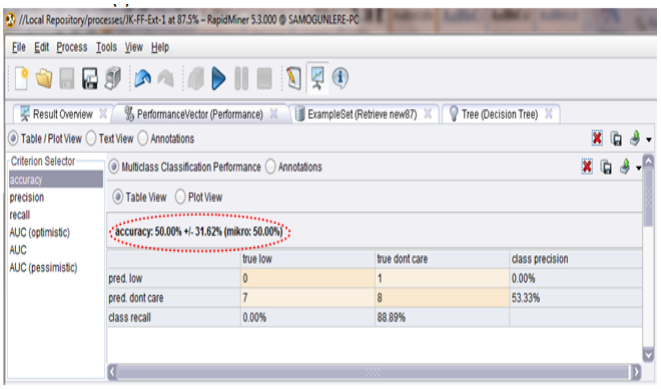


Table 1.2(d): Decision Tree Table for JK-FF Extension-1 at 87.5% Active States Utilization



These Decision Tree Tables under the performance vector of the different Flip Flops show that conventional SR-FF at 50% active states utilization has a performance rate of 60% accuracy (in the red dash cycle); the conventional JK-FF at 75% active state utilization has a performance rate of 25% accuracy; the JK-FF Extension-0 at 87.5% active states utilization has a performance rate of 85% accuracy, while that of JK-FF Extension-1 at 87.5% active states utilization has a performance rate of 50% accuracy. This is summarised in Table 1.2 (e).

Table 1.2(e): Classification Accuracy of Performance Vector in Different Flip Flops Decision Tree

	SR-FF at 50% utilization	JK-FF at 75% utilization	JK-FF Ext-0 at 87.5% utilization	JK-FF Ext-1 at 87.5% utilization
Performance Rating	60.00%	25.00%	85.00%	50.00%

From the summary of Table 1.2(e), it is evident that the JK-FF Extension-0 at 87.5% active states utilization has a higher speed performance than the other Flip Flops.

5. COMPARATIVE PERFORMANCE ANALYSIS OF DIFFERENT FLIP-FLOP CONFIGURATIONS WITH RESPECT TO PROPAGATION TIME FRAMEWORK.

Another alternative way of determining the performance level of the different Flip Flops under review is using what is known as Propagation Time Framework. In digital logic design, analysis of Propagation Time is a measure of performance which in this case speed performance of Computer memory. The propagation time is determined by the number of transitions required to complete a propagation route in Flip Flop configuration to examine the performance sensitivity of the various memory elements (Flip Flops) in other to ascertain their comparative performances. To demonstrate the utility and flexibility of this framework, it is important to know the number of transistors per gate that make up a basic memory element. This is paramount in determining the performance or how fast a memory element is. The following should be noted in a Bipolar Junction Transistor (BJT).

- Buffer has 2Transistors
- Inverter gate has 1Transistor
- AND gate has 3Transistors
- OR gate has 3Transistors
- NAND gate has 2Transistors and,
- NOR gate has 2Transistors

5.1 Determination of Transition Routes

Starting with SR and JK Flip Flops being the conventional memory elements, the propagation time for these Flip Flops is analyzed in Figures 2 and 3 respectively where 'T' represents Transistor(s) and 'G' represents Gate(s). Tables 1.3(a) & (b) show the number of transitions required to complete a propagation route in each Flip Flop configurations.

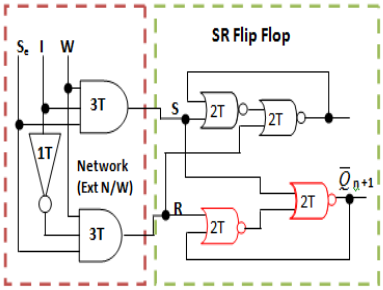


Table 1.3(a): Number of transitions required

	Gate	No of G	No of T
Ext N/W	AND	2	6
	Inverter	1	1
Flip Flop	NOR	2	4
(SR-FF)	Inverter	0	0
	Total		11

Figure 2: Basic Memory Element (Using Conventional 50% SR-FF).

In determining the transition route for conventional SR-FF, the propagation time is determined by the number of gates the signals have to pass through from the inputs of the Flip-Flop to its outputs. Having known the number of gates, the number of Transistors is determined as shown in Table 1.3(a) as explained below.

- **S goes through 2 NOR gates to reach Q; 1 NOR gate to reach $\bar{Q}$.**
- **R goes through 2 NOR gates to reach $\bar{Q}$; 1 NOR gates to reach Q.**

Therefore, 2 NOR gates = 4T = 4Transistors is to be considered since both S & R are simultaneously applied. Adding 4Transistors to the external network input gates generated from the data analysis gives a total number of 11 Transistors as depicted in Table 1.3(a).

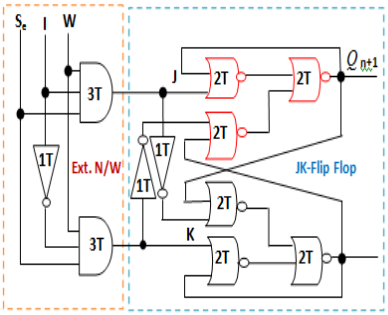


Table 1.3(b): Number of transitions required

	Gate	No of G	No of T
Ext N/W	AND	2	6
	Inverter	1	1
Flip Flop (JK-FF)	NOR	2	4
	Inverter	1	1
	Total		12

Figure 3: Basic Memory Element (Using Conventional JK-FF at 75%-NOR gate configuration (currently available RAM commercially)

Likewise, the number of gates the signals passes through from the inputs of the JK- Flip-Flop to its outputs being represented by the number of Transistors per gate, is determined as follows:

- **J goes through 2 NAND/NOR gates to reach $\bar{Q}$, 1 Inverter & 2 NAND/NOR gates to reach Q.**
- **K goes through 2 NAND/NOR gates to reach Q, 1 Inverter & 2 NAND/NOR gates to reach $\bar{Q}$.**

Since J & K are simultaneously applied, 2 NAND/NOR gates and 1 Inverter = 4T + 1T = 5Transistors is to be considered. Adding 5Transistors to the external network input gates generated from the data analysis gives a total number of 12 Transistors as depicted in Table 1.3(b).

Similarly, the JK-Flip Flops Extension at 87.5% active states utilization analysis using the Propagation Time Framework are depicted in Figures 4 and 5 with their respectful Tables 1.3(c) and 1.3(d) showing the number of transition required to complete a propagation route.

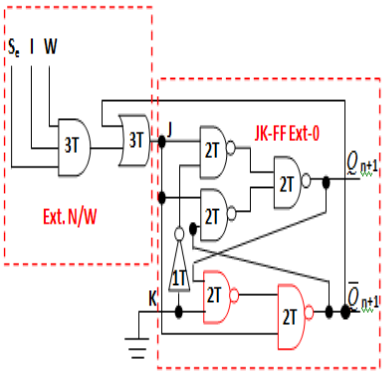


Table 1.3(c): Number of transitions required

	Gate	No of G	No of T
Ext N/W	AND	1	3
	OR	1	3
JK-FF	NAND	2	4
Extension-0	Inverter	0	0
	Total		10

Figure 4: Basic Memory Element (JK-FF Extension-0) at 87.5% NAND gate configuration)

In determining the transition route for JK-FF Extension-0, the number of gates the signals passes through from the inputs to its outputs being represented by the number of Transistors per gate, is determined as follows:

- **J goes through 2 NAND gates to reach Q, 1 NAND gate to reach $\bar{Q}$.**
- **K goes through 2 NAND gates to reach $\bar{Q}$, 1 Inerter and 2 NAND gates to reach Q.**

Since K is grounded in Basic Memory Element, only J-Terminal is required to be considered. Hence, 2NOR gates = 4T = 4Transistors is to be considered. Adding 4Transistors to the external network input gates generated from the data analysis gives a total number of 10 Transistors.

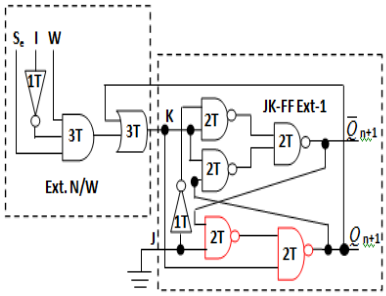


Table 1.3(d): Number of transitions required

	Gate	No of G	No of T
Ext N/W	AND	1	3
	OR	1	3
	Inverter	1	1
JK-FF	NAND	2	4
Extension-1	Inverter	0	0
	Total		11

Figure 5: Basic Memory Element (JK-FF Extension-1) at 87.5% NAND gate

Likewise, the number of gates the signals passes through from the inputs of the JK-FFExrtension-1 to its outputs being represented by the number of Transistors per gate, is determined as follows:

- **K goes through 2 NAND gates to reach $\bar{Q}$, 1 NAND gate to reach Q.**
- **J goes through 2 NAND gates to reach Q, 1 Inerter and 2 NAND gates to reach $\bar{Q}$.**

Since J is grounded in Basic Memory Element, only K-Terminal is required to be considered. Hence, 2NAND gates = 4T = 4Transistors is to be considered. Adding 4Transistors to the external network input gates generated from the data analysis gives a total number of 11 Transistors.

6. CONCLUSION

The analysis in this paper shows that, Figure 4 produces a Basic Memory Element that can be used to configure RAMs of different capacities that will result in a faster computer processing speed. Take for instance, a 10GB DRAM made of Flip Flop configuration in Figure 4; 10G transistors are eliminated thereby increasing the speed of the computer processing by a factor of 10^9 compared with the commercially available DRAMs that are made up of Flip Flop configuration of Figures 2 and 3. Comparing the number of transitions required to complete a propagation route in Flip Flop configuration of Figure 4 and that of Figures 2 and 3, it becomes evident that the Basic Memory Element of Figure 4 is operating at a ratio of 6:4 or 3:2. That is, the Basic Memory Element of Figure 4 will be one and half times faster than those of Figures 2 and 3.

Since the ultimate metric of memory system performance is related to how fast it can service critical requests from processors; the rationale used to justify the focus of this work is that by improving the Memory Cells used for designing memory system, the average request service time can be reduced. The study performed in this paper shows remarkable performance improvement on high capacity of memory system, while it may be negligible on lower memory capacity.

This study has also been able to prove that though conventional Flip Flops are effective with two resting states at 50% and 75% utilization in digital device applications, but they are not as efficient when compared to JK-FF Extension-0 at 87.5% active state utilization with one resting state. This can be seen in Table 1.2(e) judging from the performance vector analysis using decision tree of all the different Flip Flops under investigation in this paper.

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