Design and Analysis of CNTFET-Based SRAM

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Abstract - Carbon Nano Tube Field Effect Transistors (CNTFETs) are being widely studied as possible successors to silicon MOSFETs. In a CNTFET, the threshold voltage can be adjusted by controlling the chirality vector (i.e. the diameter). Therefore Design of SRAM Cell based on CNTFET is important for Low-power cache memory. In this paper we have successfully developed a compact model for MOSFET like CNTFET. This paper begins with the analysis of the CNTFET. The dependency of I-V characteristics on chirality is studied and then 6-T based SRAM is designed with different chirality for n-CNTFET AND p-CNTFET. The performance of the SRAM cell is measured In terms of write time for high speed and static noise margin for stability of the cell.

Key Words: CNT, CNTFET, SRAM, Chirality, Write Time, SNM

1. INTRODUCTION

The increasing demand of more and more functionality on-chip with the fastest ever-possible speed at the cost of minimum power consumption is putting a question mark on the existing semiconductor technology. For few decades the scalability of the S.C. technology has solved the problems to some extent, but soon it will reach its limit due to quantum mechanical effect. The existing S.C. technology has also put limit on the speed with substantially more power consumption due to increase in the number of devices; causing more inter-connect delays and more static power consumption. Thus it is allowing speed up to a few GHz only with the limit on operation of minimum threshold for the chip. This focuses attention on search of alternatives that can replace or integrate with silicon in nano-scaled transistors to resolve the existing problems and meet the today's requirement. The carbon nanotube is one among the most promising alternatives due to its superior electrical properties. The use of carbon nanotube with silicon technology not only causes reduction in threshold voltage but also allows the speed to reach in THz or PHz.

This exceptional behaviour of carbon nanotube has been utilised in the design of CNTFET and proved to be boon as static power consumption gets reduced considerably. Now the research is going on the design of memory subsystem which is a major part of any electronic system requires higher speed with low power consumption. Static Random Access Memories (SRAMs), being a crucial component in the memory hierarchy of modern computing systems, needs to be very-fast accessible with low power consumption. In this regard SRAM Cell design using CNTFET proves useful as CNTFET require less threshold voltage. SRAM cell performances are usually measured in terms of static noise margin and write time. Implementations of SRAM cell with different chirality for n- and p-CNTFET are made.

2. CARBON NANO TUBE FIELD EFFECT TRANSISTORS

CNT is a tubular form of carbon with diameter as small as 1nm. The length of the tube ranges from a few nm to µm. A CNT is characterized by its Chiral Vector: $C_h = n\,\hat{a}_1 + m\,\hat{a}_2$, $\theta \rightarrow$ Chiral Angle with respect to the zigzag axis ,

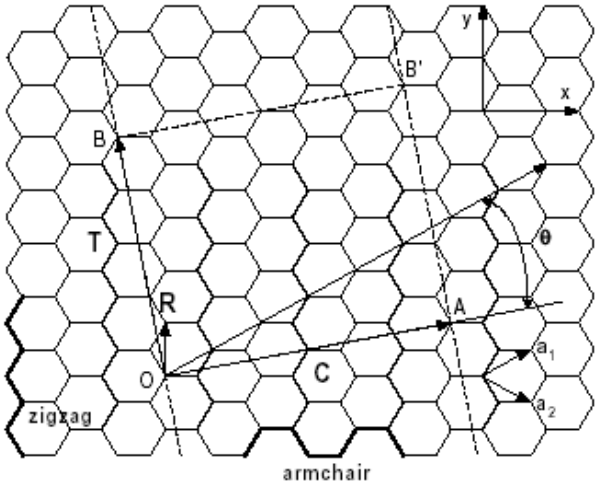

Fig. 1 Graphene sheet rolling up to CNT

where $\hat{a}_1$ and $\hat{a}_2$ are lattice basis vectors of graphene sheet and the chiral angle represents the angle that the axis of rolling up sheet forms with one of the basis vectors. On the basis of chirality CNT can be classified as, zig zag ($\theta = 0°$), Chiral ($0° < \theta < 30°$), or armchair (with $\theta = 30°$).

A single-wall carbon nanotube (or SWCNT) consists of only one cylinder, and the simple manufacturing process of this device makes it a very promising alternative to today's MOSFET. An SWCNT can act as either a conductor or a semiconductor depending on the angle of the atom arrangement along the tube. This is referred to as the chirality vector and is represented by the integer pair (*n, m*). A simple method to determine if a carbon nanotube is metallic or semiconducting is based on considering the indices (*n, m*), i.e. the nanotube is metallic if *n=m* or *n-m=3i* where *i* is an integer. Otherwise, the tube is

semiconducting. The diameter of the CNT with chirality (n, m) can be calculated as

$$D_{CNT=}(a_0)/\pi *(n^2+nm+m^2)^{1/2}$$

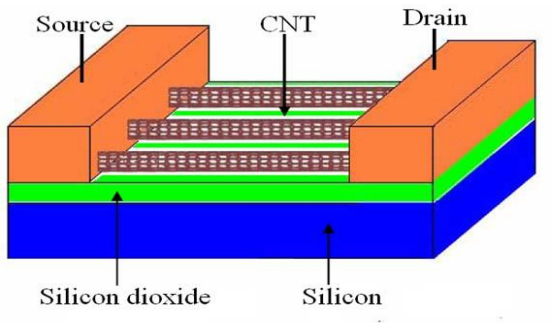

Fig -2: CNTFET Structure

Carbon nanotube field effect transistors (CNTFETs) utilize semiconducting single-wall CNTs to assemble electronic devices; CNTFETs are having similar properties to MOSFETs. The CNTFET device current is saturated at higher V_{ds} (drain to source voltage) as channel length increases as shown in Fig.3, and the on-current decreases due to energy quantization in the axial direction at 32-nm (or less) gate length. The threshold voltage is defined as the minimum gate-source voltage required to turn on the transistor, and the threshold voltage of the CNT channel can be defined as the half band-gap which is an inverse function of the diameter

$$V_{th}=E_g/2e=((3)^{1/2}/3)*(a_0.V/eD_{CNT})$$

where 'a_0' = 2.49 Å is the carbon-to-carbon atom distance, 'V' = 3.033 eV is the carbon π-π bond energy in the tight bonding model, 'e' is the unit electron charge, and 'D_{CNT}' is the diameter of CNT. Thus the threshold voltage of the CNTFET will change with the chiral indices. The threshold voltage of the CNTFET is inversely proportional to the chirality vector of the CNT (as shown in fig.4). The saturation current is also found to be function of chiral index, which means that on-off current ratio is very high for CNTFET.

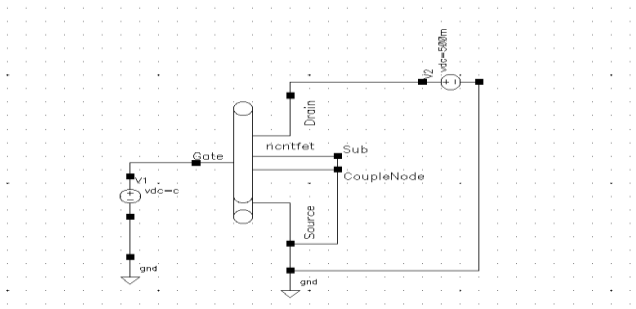

Fig -3: Circuit Schematic for I-V Characteristic of N-CNTFET

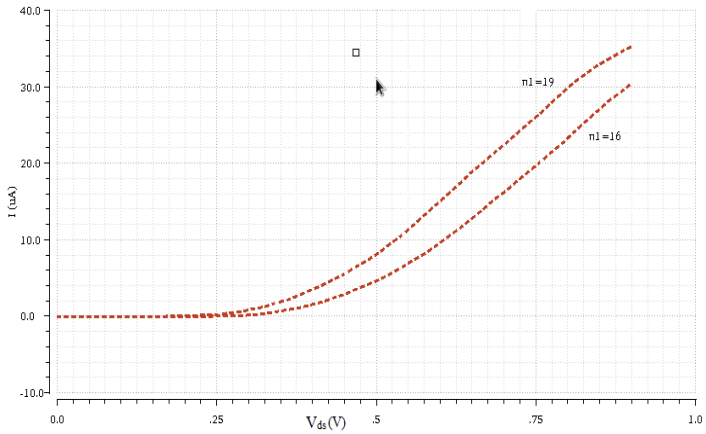

Fig -4: I_d vs. V_{gs} plot for n-CNTFET

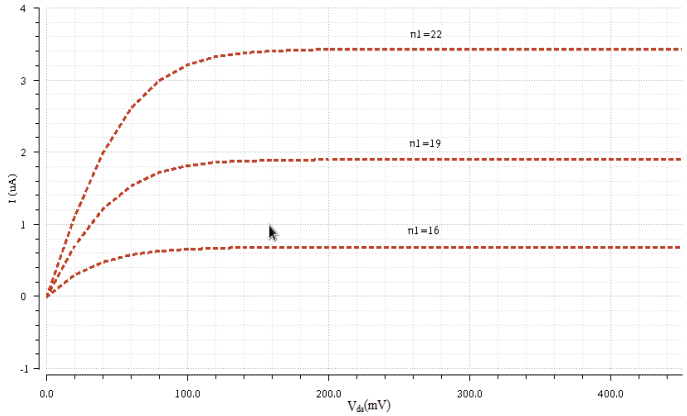

Fig -5: I_d vs. V_{ds} plot for n-CNTFET

Owing to high I_{on}/I_{off} ratio, CNTFET can have better scope as a switch. The inverter can be formed by combination of p-CNTFET and n-CNTFET (as shown in Fig.6). The output voltage has very less delay in transition from one state to other acting as almost ideal switch.(fig.).The voltage transfer characteristic of the inverter reveals that it has very high noise margin.

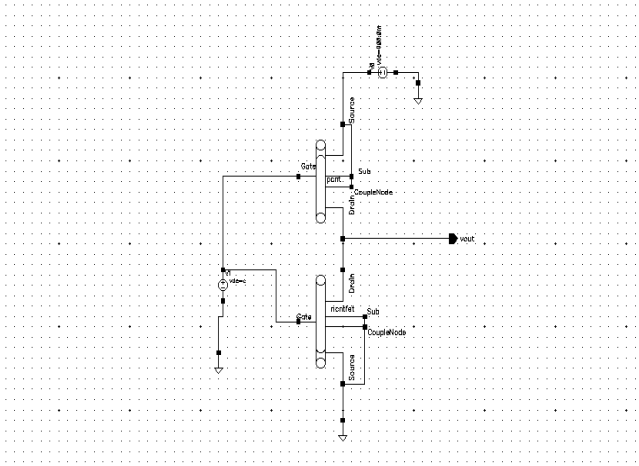

Fig -6: Circuit Schematic for CNTFET-Based Inverter

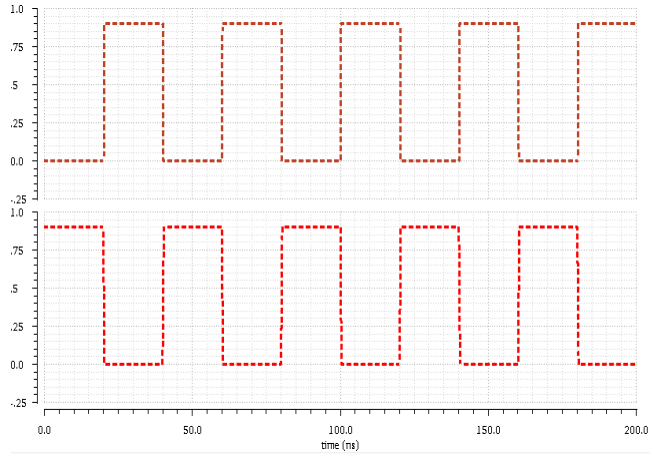

Fig -7: CNTFET-Based Inverter Logic Verification

3. SRAM CELL DESIGN

Two cross coupled inverters along with two switches forms a simple SRAM cell. The coupled inverter stores the bit at the two nodes, q & q_bar, and the switch act as the switch for reading and writing of the data.

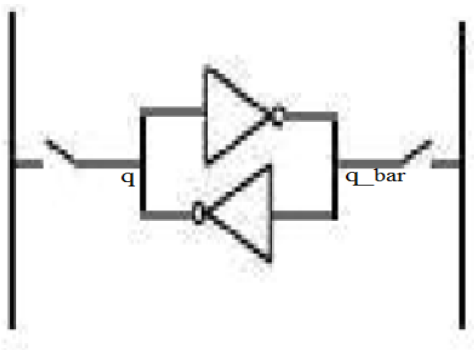

Fig -8: Basic SRAM Cell

The switches are usually designed using NMOS pass transistors with wordline as enable input. The low wordline implies disconnection of the cyclic inverter with bitline and the internal state of the coupled inverter will be preserved. The SRAM cell structure shown above is fully symmetric. and READ and WRITE operations are performed using both bitlines, BL and BL′ While reading or writing, common wordline (i.e., WL) controls accessibility to the cell nodes q and q_bar through two pass transistor.

SRAM cells are used to implement high capacity memories that require low power consumption, short access times, and high endurance to process variations and environmental conditions. Writing operation of SRAM cell can be performed by loading the bitlines BL and BL′ with the new value and its complement using write circuit respectively and raising wordline high simultaneously. READing data out of the cell is performed by first precharging both the bitlines high and then reading the data through the when the wordline is raised turning on the pass transistors.

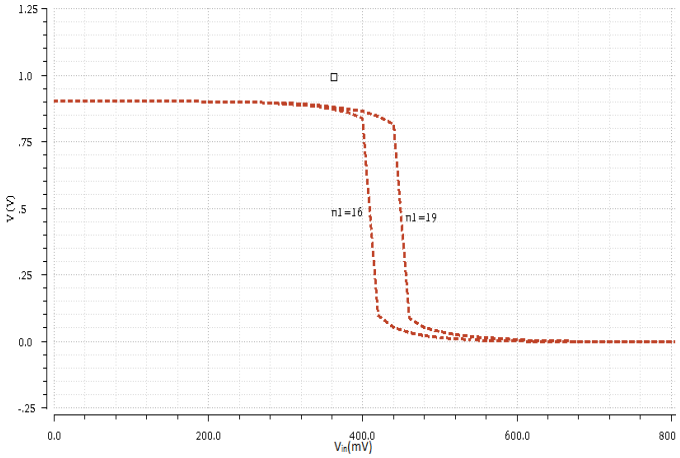

Fig -9: CNTFET-based Inverter Voltage Transfer Characteristics

The 6-transistor SRAM model is shown here. The proper sizings of the transistors are required in order to maintain its state while reading and holding the stored value. For reading operation to perform, the size of n-CNTFET used in cross-coupled inverter (N1& N3) should be greater than that of pass-transistor (N2&N4). The performance of SRAM cell is measured in terms of stability and the write time. The write time is defined as the time required to write the bit inside the cell. The write time is measured as the time interval when 50% of the time when the data input is changing to the 50% of the time when data is stored in the SRAM cell. Static Noise Margin is defined as the maximum level of dc perturbance that a cell node can tolerate before changing its state. Static noise is dc disturbance such as offsets and mismatches due to processing and variations in operating conditions.

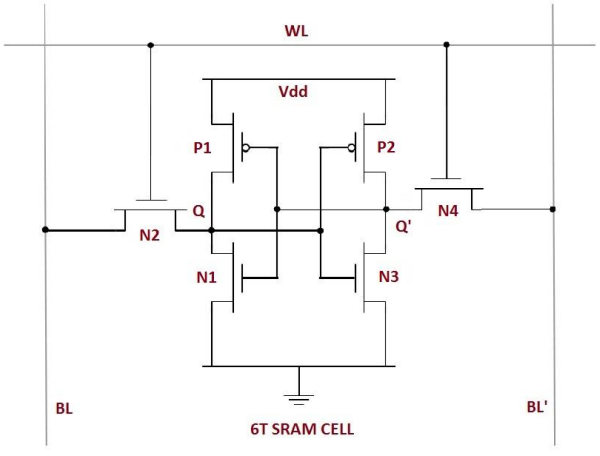

Fig -10: 6-transistors based SRAM cell

4. IMPLEMENTATION AND RESULTS

The model of CNTFET are made using Verilog-A code as per given by Stanford University. Using that code, symbols for p- and n-CNTFET are created in CADENCE-Virtuoso.
The 6-T SRAM cell for write operation with proper chirality is designed in 32-nm Technology. The sizing of

transistors i.e., the no. of tubes for N1&N2 CNTFET are 5 and 4 respectively, while p-CNTFET has 3tubes. The channel length is set to be 32 nm, and the chiral vectors for N1 &N2 transistors are (19, 0). The chiral index of p-CNTFET are taken as (19,0) and (16,0) for two simulations.

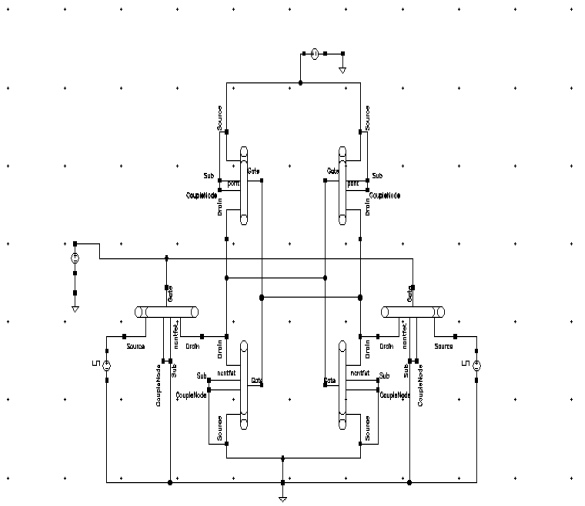

Fig -11: CNTFET-based SRAM cell for WRITE Operation

The write operation is performed by suppling data_in to bitlines. For data_in=111100001111, the waveforms of q and q_bar are plotted in the fig. The write time for p-CNTFET chiral indices of (19, 0) and (16, 0) are calculated and found to be as 2.71 ps and 2.04 ps respectively.

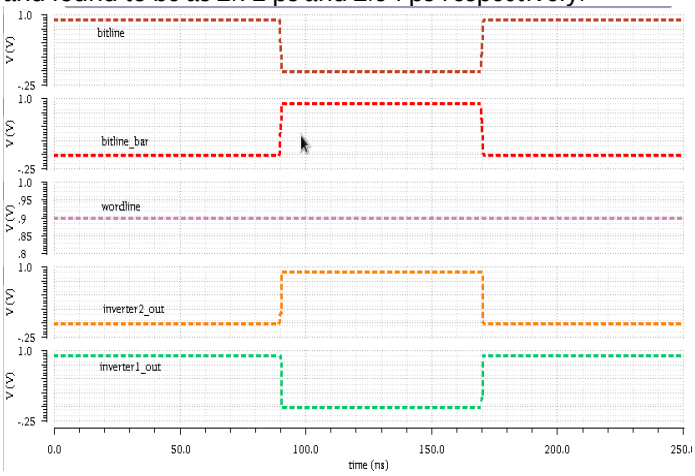

Fig -12: CNTFET-based SRAM cell write timing diagram for data_in=111100001111

For read operation the bitlines are precharged to V_{dd} and capacitors are connected to the bitline to allow discharging it the corresponding node is storing 0 value. The static noise margin is calculated by modelling internal noise as Vn voltage source and then varying this value from Vn=0 V to Vn=V_{dd}/2. The state voltage q and q_bar are plotted against Vn (fig.). The static noise margin are found to be 365.2mV and 412.5mV for p-CNTFET chiral indices of (16, 0) and (19, 0) respectively.

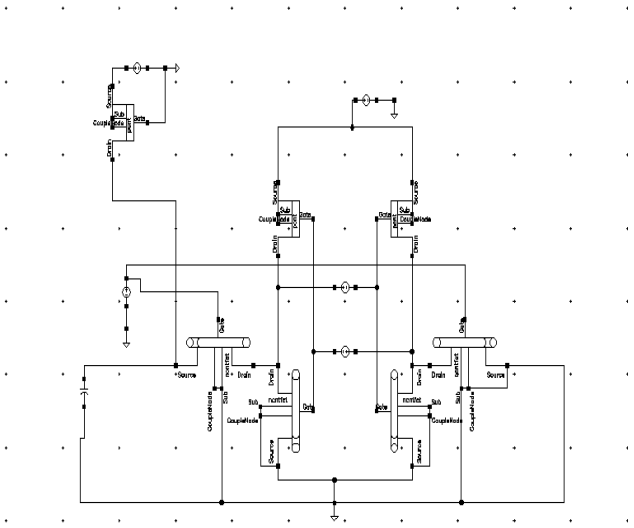

Fig -13: CNTFET-based SRAM cell for SNM calculation

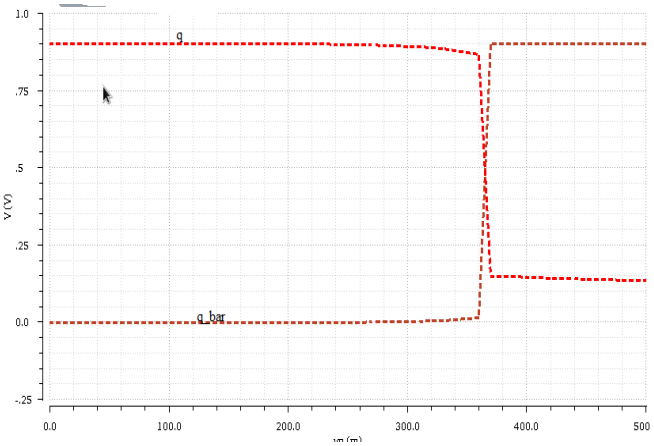

Fig -14: Cell data transitions due to two series voltage noise sources

5. CONCLUSIONS

The 6T-SRAM cell was designed using CNTFETs with different chiral indices. The dependency of I-V characteristics on chirality was studied and then 6-T based SRAM was designed with different chirality for n-CNTFET AND p-CNTFET. The performance of the SRAM cell was measured In terms of write time for high speed and static noise margin for stability. SRAM cell with 4 n-CNTFET of chirality(19,0) and 2 p-CNTFET of (16,0) had low write time and high SNM, it can be used for high speed SRAM design with high stability. The write time for this cell was coming to be 2.04 ps. And static noise margin was found to be 365.2mV. 6T SRAM cell designing method was proved to be more accurate and highly stable due to static noise reduction.

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BIOGRAPHIES

Monish Jaiswal completed his M.Tech from Government College of Engineering Amravati. Working as an Assistant Professor in Electronics Engineering Depar-tment, RGCER Nagpur. Research interests are in VLSI Design, Embedded system Design, and Signal Processing.

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