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Design and Comparison of power consumption of Multiplier using adiabatic logic and Conventional CMOS logic

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Abstract- *Power consumption plays an important role in the present day VLSI technology. Power consumption of an electronic device can be reduced by adopting different design styles. Adiabatic logic style is said to be an attractive solution for such low power electronic applications. CMOS technology plays a dominant role in designing low power consuming devices, compared to different logic family CMOS has less power dissipation. This paper focuses on a novel energy efficient technique called adiabatic logic which is based on energy recovery principle and power is compared by designing a multiplier.*

Key Words: CMOS, Conventional switching, Adiabatic logic, Adiabatic switching

1. INTRODUCTION

The technological evolution has increased the number of transistor for a given chip area significantly and increases the switching cycle from MHz to GHz range. As the transistor count increases rapidly in the system-on-chip area, significant reduction in power overhead in dynamic switching and leakage is of particular importance. As many of the present day electronics devices are portable ,they need more battery backup which can be achieved only with the low power consumption circuit that are internally designed in them. As the power dissipation in the device increases then the extra circuitry is necessary to cool the device and to protect the device from thermal breakdown. The power consumption in conventional CMOS circuit is due to switching activity of the device from one state to another state and due to the charging and discharging of load capacitor at the output node. There are some limitations for reducing power dissipation compared to CMOS, which can be done by using adiabatic techniques. The adiabatic is a thermodynamic term that is used to describe a process where there is no exchange of heat with the environment. In this technique instead of discharging the consumed energy is recycled back to the power supply there by reducing overall power consumption.

2. CONVENTIONAL CMOS TECHNOLOGY

One of the most popular MOSFET technologies available today is the complementary MOS, or CMOS, technology. This technology makes use of both P and N channel devices in the same substrate material. Such devices are extremely useful, since the same signal, which turns on a transistor of one type, is used to turn off a transistor of the other type. This allows the design of logic devices using only simple switches, without the need for a pull-up resistor [1]. Power loss in conventional CMOS transistors mainly occurs because of device switching. Figure 1 shows a typical inverter implementation.

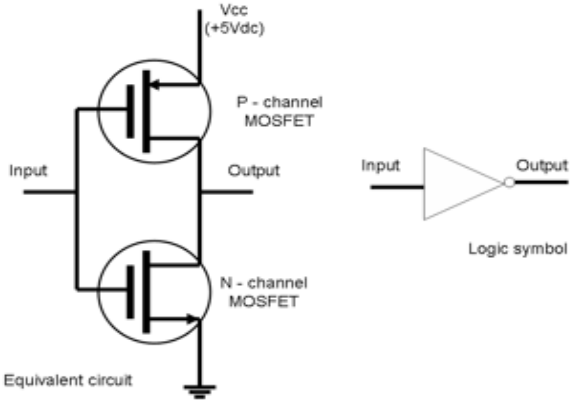

Figure 1.CMOS conventional inverter

The operation of the circuit can be evaluated in two stages of charging phase and discharging phase. During the charging phase shown in figure 2(a), the input to the circuit is logic LOW. During this phase, the PMOS transistor conducts and NMOS transistor goes in to OFF state which charges the output value to power supply results in logic HIGH output. The equivalent circuit consists of a resistor in series with the output load capacitance, which shows a charging path from power supply to output terminal. Here the resistor acts a PMOS ON resistor. During the discharging phase shown in figure 2 (b),the input to the circuit is logic HIGH. During this phase, the NMOS transistor conducts and PMOS transistor goes into OFF state, which results in a discharging path from output terminal to ground. The value that is stored at

the output during the charging phase discharges towards the ground results in logic LOW output. The equivalent circuit consists of a resistor in series with output terminal to ground. Here the resistor acts as NMOS ON resistor.

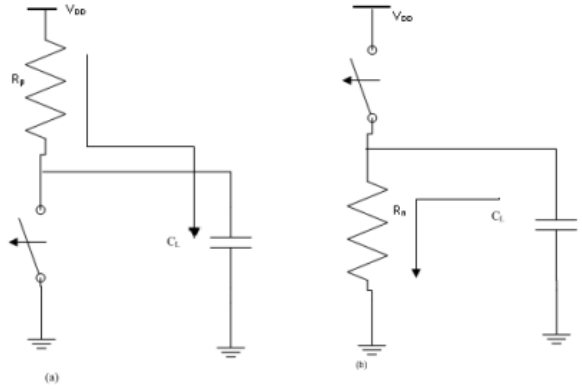

Figure2.charging and discharging

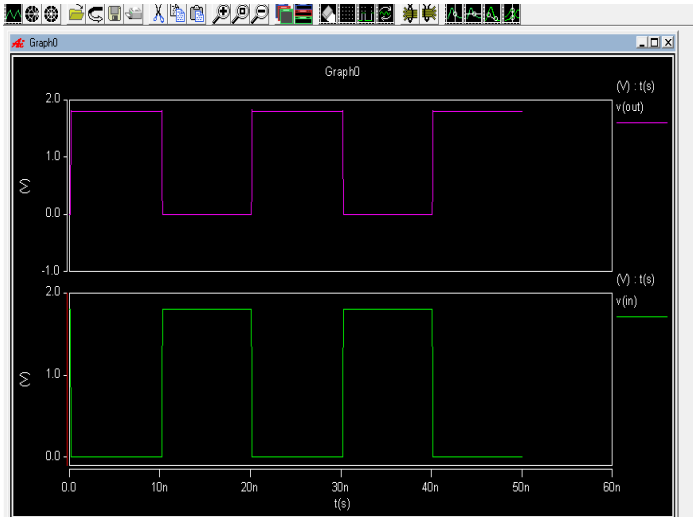

Figure 3. Simulation Waveform of CMOS Inverter

In this simulation waveform, it is noted that when input is 'High' the corresponding output is 'low' and when the input is 'low' then the corresponding output is 'High'.

2.1CMOS AND Circuit

A AND gate output rise only when it's all inputs are high(1). CMOS AND gate and its simulation wave form is shown in figure 4 (a) and (b).

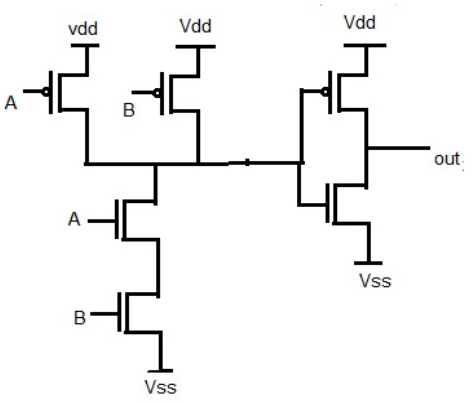

Figure.4 (a)CMOS AND gate circuit

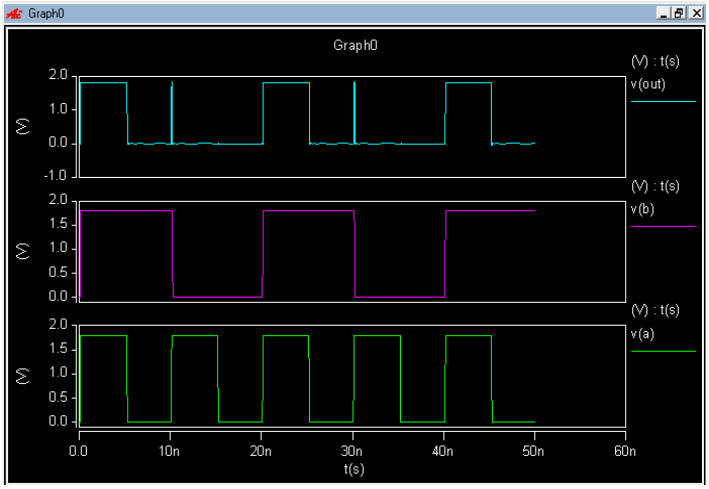

Figure 4 (b) simulation waveform

2.2.CMOS OR Gate circuit

A OR gate output is fall only when it's all inputs are low(0). CMOS OR gate and its simulation wave form is shown in figure 5 (a) and (b).

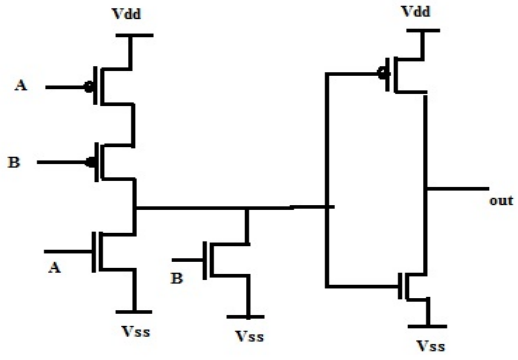

Figure.5(a) CMOS OR gate circuit

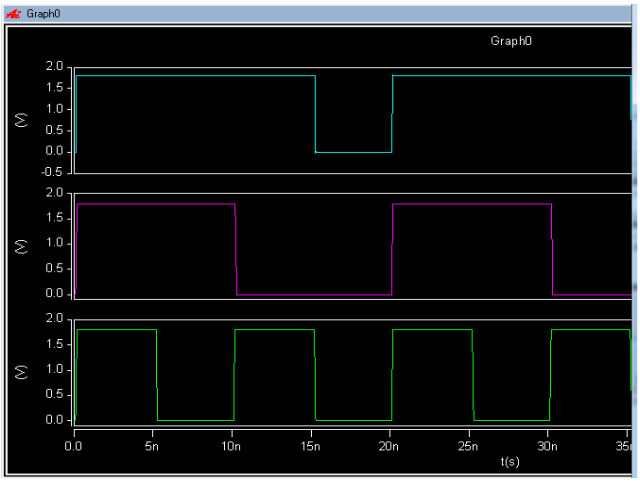

Figure 5 (b) simulation waveform

3. ADIABATIC LOGIC

The word ADIABATIC is derived from the Greek word "adiabatos",which means there is no exchange of energy with the environment and hence no energy loss in the form of heat dissipation. Adiabatic logic is commonly used to reduce the energy loss during the charging and discharging process of circuit operation. Adiabatic logic is also known as "energy recovery" or "charge recovery" logic.

3.1. Adiabatic Switching

Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small [2]. This can be achieved by charging the capacitor from a time varying voltage source or constant current source, as shown in Figure 6. Here, R represents the on-resistance of the pMOS network. Also note that a constant charging current corresponds to a linear voltage ramp. Assuming that the capacitance voltage VC is zero initially, the variation of the voltage as a function of time can be found as

$$VC(t)=IS.tC \quad (1)$$

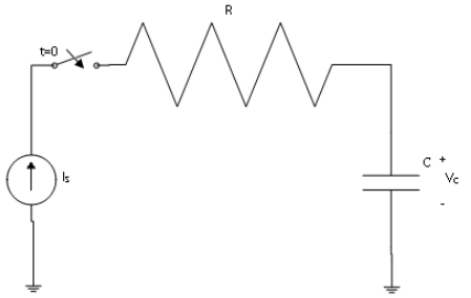

Figure 6. Schematic for adiabatic charging process

Hence the charging current can be expressed as a function of VC and time t

$$IS=C.VC(t)t \quad (2)$$

The amount of energy dissipated in the resistor R from t = 0 to *t* = T can be found as

$$Ediss=R\int I_s^2 dt=RI_s^2T \quad (3)$$

Combining (2) and (3), the dissipated energy during this charge-up transition can also be expressed as

$$E_{diss}=RC/T.CV_c^2(T) \quad (4)$$

From (4) we can say that the dissipated energy is smaller than for the conventional case if the charging time T >>2RC and can be made small by increasing the charging time. A portion of the energy thus stored in the capacitance can also be reclaimed by reversing the current source direction, allowing the charge to be transferred from the capacitance back into the supply. Adiabatic logic circuits thus require non-standard power supplies with time-varying voltage, also called pulsed power supplies.

3.2. Adiabatic Inverter

The operation of the adiabatic inverter can be explained in two stages(schematic and simulation wave form are shown in figure 7(a)and (b)). During the charging phase, the PMOS transistor conducts and NMOS transistor goes into OFF state which charges the output load capacitor towards the power supply results in logic HIGH output. During discharging phase, the NMOS transistor conducts and PMOS transistor goes into OFF state. Instead of discharging the stored value at the output towards ground, the energy is recycled back to the power supply. Its equivalent circuit consists of a resistor in series with output load capacitance and power supply [3].

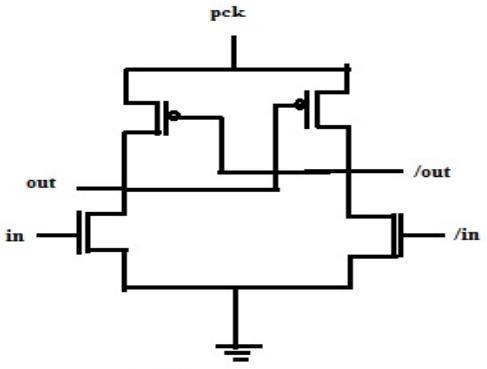

Figure 7a).Adiabatic Invert

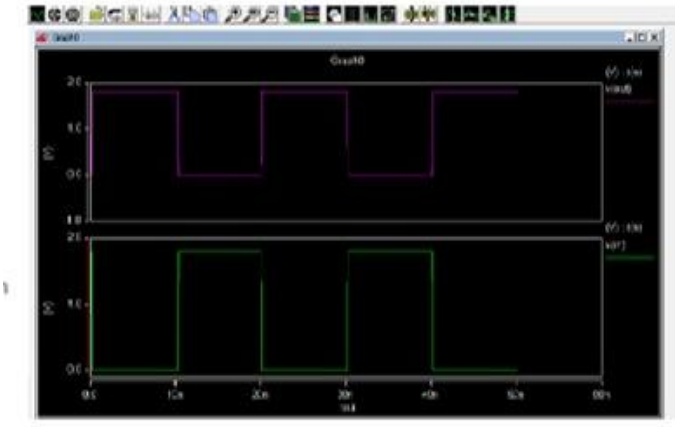

Figure 7 b) Simulation waveform

3.3.Adiabatic AND and NAND Gate

The figure 8 (a) and (b)shown below is ECRL AND and NAND Circuit and simulation waveform. It functions same as that of CMOS AND and NAND circuit.

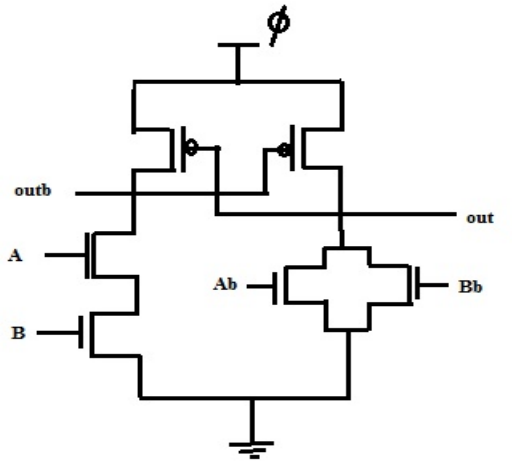

Figure.8 a) Adiabatic AND and NAND

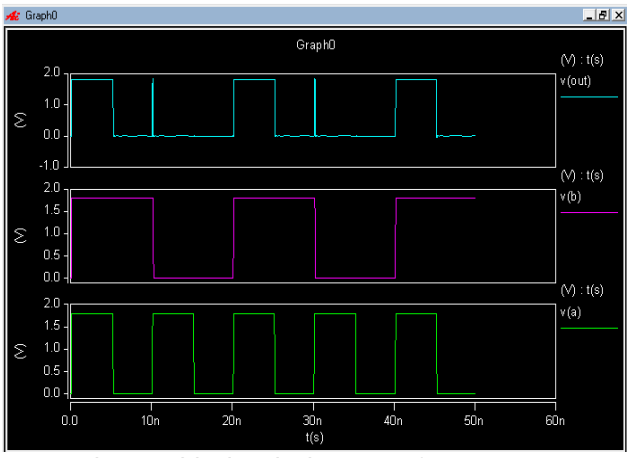

Figure8.b) Simulation waveform

Adiabatic OR and NOR Gate

The figure 9 (a) and (b)shown below is ECRL OR and NOR Circuit and simulation waveform. It functions same as that of CMOS OR and NOR circuit.Out put is fall only when both the inputs are low(0)[4]

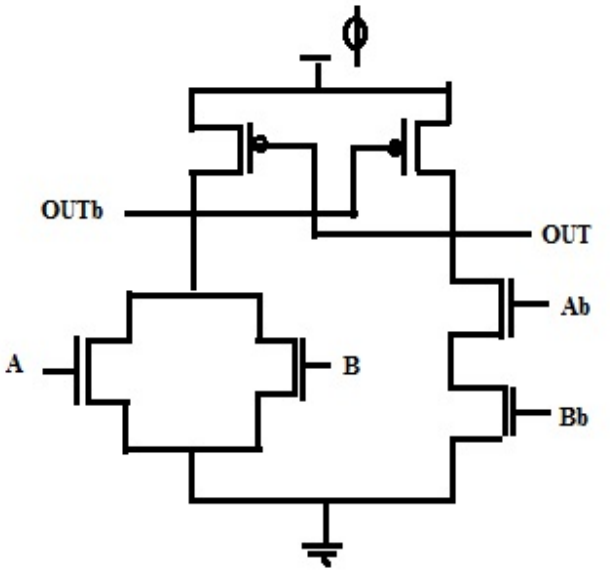

Figure9. a) Adiabatic OR and NOR

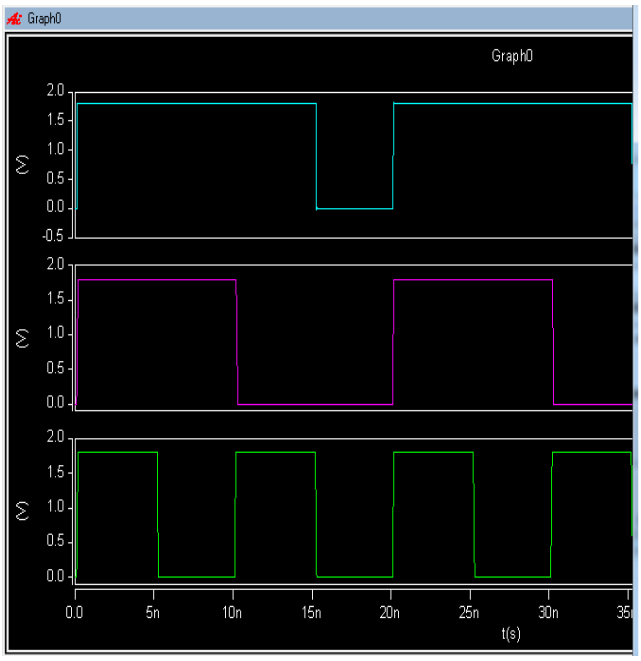

Figure9.b) Simulation waveform

4. DESIGN AND ANALYSIS OF MULTIPLIER

The combinational structure of the standard multiplier is shown in figure 10, instead of registers it comprises of CMOS/ Adiabatic logic gates. The unit takes two 2 bit

inputs A(A_0,A_1) and B(B_0,B_1) and produce a 4 bit output (C_{out},S_2,S_1,S_0)

A_1 A_0
B_1 B_0

N_1 N_0
N_3 N_2

C_{out} S_2 S_1 S_0

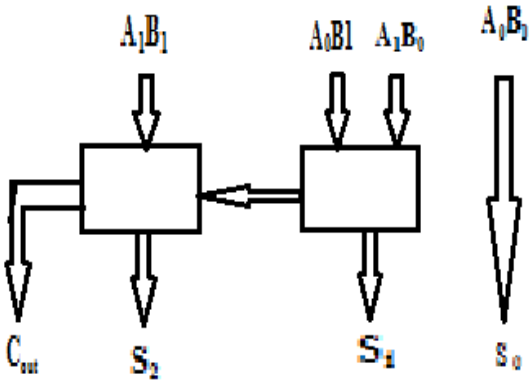

Figure 10.Architecture of standard 2X2 Multiplier

Simulation result of 2X2 multiplier [5] using conventional CMOS gates and Adiabatic logic are shown in figure 11 (a) and (b).

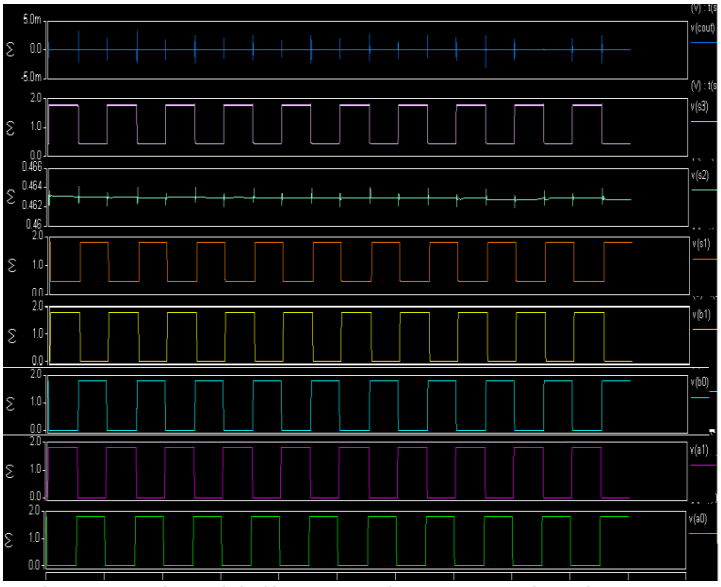

Figure 11.a) multiplier out using Conventional CMOS

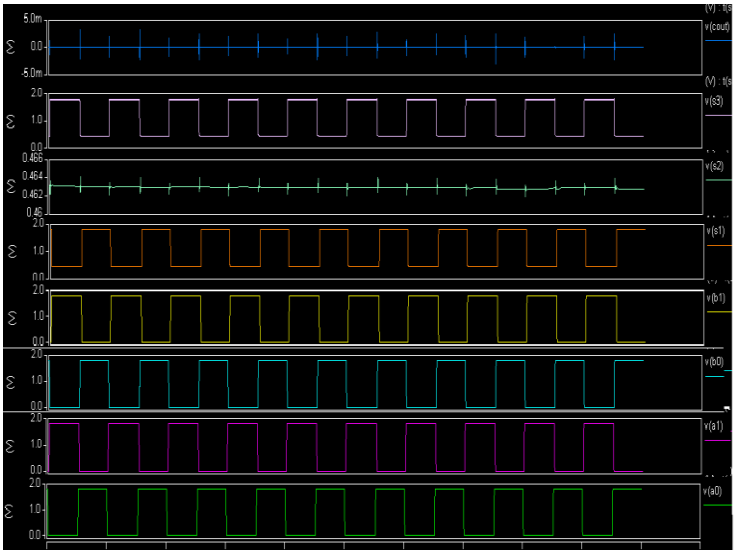

Figure 11. b) multiplier out using adiabatic CMOS

Table:1. Comparison Of power consumption for conventional and adiabatic CMOS Gates/Circuits CMOS

Gate/Circuits	Power consumption for Conventional CMOS Logic	Power consumption for Adiabatic CMOS Logic
AND	3.2400uw	1.0685uw
OR	3.2400uw	716.2335nw
INVERTER	183.4915nw	10.0277nw
MULTIPLIER	7.4922uw	1.16uw

5. CONCLUSIONS

This paper has described the power comparison and simulation of logic gates and multiplier designed using conventional CMOS and Adiabatic logic. The analysis shows that designs based on adiabatic principle gives superior performance when compared to traditional approaches in terms of power even though their transistor count is high in some circuits so for low power and ultra low power requirements adiabatic logic is an effective alternative for traditional CMOS logic circuit design. This comparison is done by using HSPICE simulator Hence, it is concluded that the proposed design circuit will provide a platform for designing high performance and low power digital circuits such as digital signal processors, adders and multiplexers ,multiplier etc.

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