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Performance Enhancement of 32-bit Carry Select Adder by Employing RTL Optimization Techniques

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Abstract: *Adders are the basic building blocks of many computational circuits. As a result, it is imperative to design fast adders and simultaneously optimize the power in these adders to the maximum extent possible. Carry Select Adder (CSA) is the most frequently used adder which works on the principle of pre computation of the sum and carry for each individual stage by* ***assuming the carry in as '0' and '1'. CSA employs*** *additional Ripple Carry Adders (RCA) which induces an undesired increase in area as well as the delay as the carry is propagated through all stages. Thus the overall area and power consumption for CSA is also on the higher side. Hence, it is inevitable to opt for techniques to reduce the power consumption to achieve higher performance which is the eventual desired goal. This work involves Register Transfer Level design of 32-bit CSA with power and delay optimization techniques. The obtained results for the power consumed for each technique are hence analyzed and compared to obtain the best design which can be further implemented.*

Keywords: Carry Select Adder (CSA), Common Clock Gating (CCG), Enhanced Clock Gating (ECG), Register Transfer Level (RTL).

I. INTRODUCTION

Every digital system employs Binary adders which functions as the major logic element. Apart from being used as addition elements, Binary adders are also play a vital role in design architectures other than Arithmetic Logic Units (ALU), including dividers, multipliers and memory addressing. Taking into account the vast usage of adder units across various complex designs, even a slight improvement in the power and performance of Binary addition, can lead to a significant enhancement. Enhanced speeds in addition and multiplication have always been pivotal in determining the performance of processors and systems.

The major problem for Binary addition lies in the carry chain. The carry chain forms the critical data path [1]. With increase in width of the input operand, a corresponding increase in the length of the carry chain is observed and also impacts the power consumption of the circuit.

Ripple-carry adders (RCA) are functionally slow due to the fact that the carry generated has to propagate through all the adder blocks. One of the solutions to reduce the delay is by utilizing the hardware such that 0 or 1 will be the carry. The concept of Conditional Sum adder can be incorporated in CSA [2]. The final stage comprises of a MUX which determines the output sum based on the value of the input carry.

As far as digital adders are concerned, the time required for the propagation of carry determines the constraint for speed [4]. Carry generation has as a major influence on the speed of any adder. In RCA, Sum and Carry for a particular bit is computed only after the preceding bit values are obtained.

II. RELATED WORK

RCA have a larger delay because the carry of each stage must be propagated to the next for computation. In [1] RCA was replaced with Binary to Excess-1 Converter (BEC) in CSA to reduce power and area. This design reduced the power but the delay was found to be more. Techniques like parallelism, pipelining were implemented and slight reduction in power was observed in [2]. However, the penalty was increased area.

The undesirable problem of propagation of carry is resolved using CSA, which produces multiple carries and consequently selects one among them [2]. Nevertheless, the major ramification of CSA lies in the increase in area. This is due to fact that CSA comprises of a series of RCA and additional MUX which leads to an increase in the number of components. The Figure illustrates a 16-bit CSA.

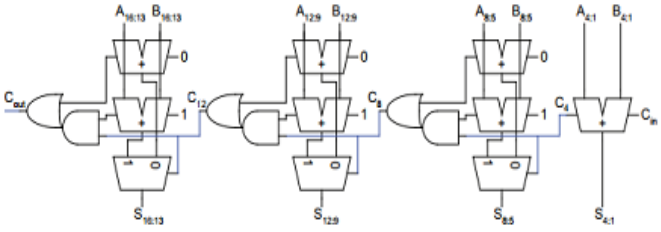

Fig -1: 16-bit Carry Select Adder.

For a 16 bit CSA, in each of the four stages two RCA are used for pre-computation of carry. However there is no advantage of predicting the carry early in the first stage. As a result only one CSA is sufficient in the first stage. This reduces one RCA in the first stage which is a significant feature of CSA.

As seen from Figure 1, better performance is obtained in carry select compared to ripple carry but at the increased cost of area and power. Since the number of adders used here are almost twice as compared to ripple carry along with the multiplexer, the cell count and hence area of the design is very high resulting in higher power consumption [3]. Hence, there is a need to reduce the power and delay of the adders. Few of the methods that are suggested in literature will lead to an increase in the cost and effective area. However the power and delay is reduced significantly. Therefore it is imperative to perform tradeoff between previously mentioned parameters. The criteria for performance depend upon the specification and requirements of designer. Usually performance of the system with respect to power and speed are given more importance than area considerations [5].

This work involves design of 32-bit CSA followed by power optimization at RTL.

III. PROPOSED OPTIMIZATION TECHNIQUES

The power reduction can be achieved by incorporating optimization techniques at the RTL. These methods play a major role in bringing down the dynamic power levels with enhanced performance.

Design of RCA

Design 1: The adder design depicted in Figure 2 uses two half adders.

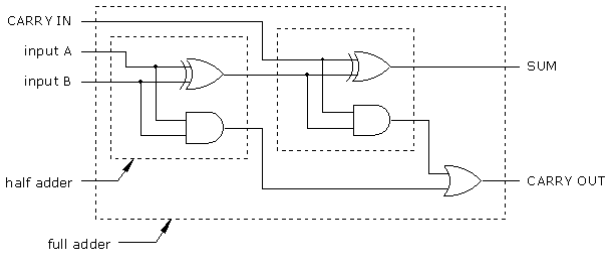

Fig -2: Full adder using two half adders

The sum and carry expressions are given in equation (1) and (2).

$$S = a \oplus b \oplus C_{in}, \quad (1)$$

$$C_{Out} = ab + C_{in}(a \oplus b) \quad (2)$$

Design 2: The adder in Figure 3 computes sum using the obtained carry. This adder is theoretically better than previous full adder design 1. In this adder, the carry of a stage is complemented and used to obtain the sum, thereby reducing area as compared to the previous design. The expressions for sum and carry are given in equations (3) and (4),

$$S = abc + (a+b+C_{in})C'_{out}, \quad (3)$$

$$C_{Out} = a(b+c) + bC_{in} \quad (4)$$

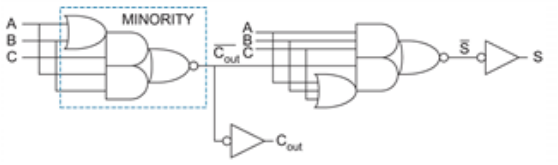

Fig -3: Alternative design for Full adder.

The optimization techniques used for power reduction in RTL are:

1) Parallelism with Pipelining
2) Common Clock Gating
3) Enhanced Clock Gating

The brief descriptions of each of the techniques are as follows:

1) Parallelism with Pipelining

An extension of concepts of pipelining and parallelism is the integration of both the concepts. Here pipelining is done for more than one parallel structure. Figure 4 shows this implementation of a 16-bit adder combining both pipelining and parallelism. This concept is extended for 32-bit CSA. In this technique, the input frequency is divided between the two parallel paths so that frequency for each path is halved.

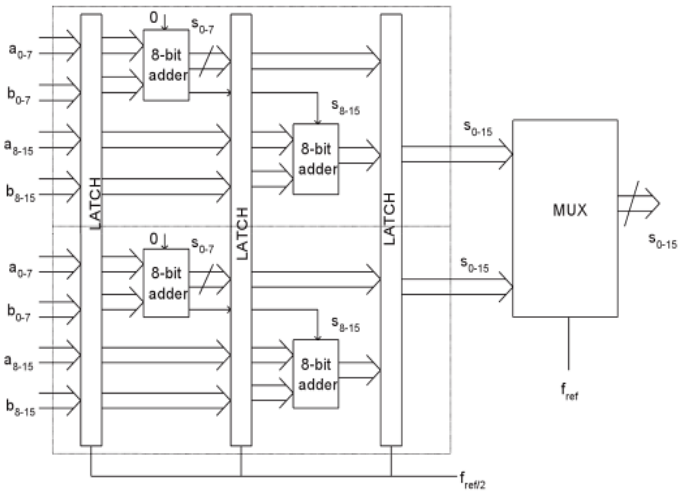

Fig -4: Parallelism with Pipelining for 16-bit CSA

The total power consumed by the parallel-pipelined datapath is given in (5) [6]

$$P_{parpipe} = C_{parpipe}V_{parpipe}^2 f_{parpipe} = (2.5C_{ref})(0.3V_{ref})^2(f_{ref}/2) \sim 0.1125\, P_{ref} \quad (5)$$

2) Common Clock Gating (CCG)

The typical clock gating implementation scheme is depicted in Figure 5. This technique helps to optimize power on the clock path by cutting off the clock path when not required. As observed, the implementation of this technique employs a latch with enable signal and clock as input. Only when the enable is high, the clock is passed to the AND gate which when turned ON passes the clock signal to the particular register [7]. Hence significant power reduction can be achieved when enable is low since it cuts off the clock supply when it is not required.

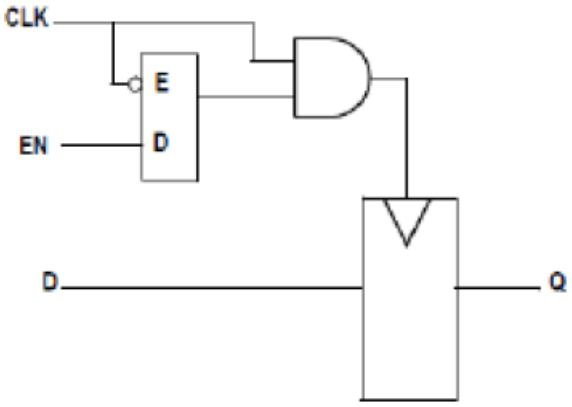

Fig - 5: Implementation of Clock gating.

3) Enhanced Clock Gating (ECG)

In conventional clock gating technique, when enable is low, the clock toggle is always wasted. Hence it is not very efficient. The most effective way of clock gating implementation is enhanced clock gating technique shown in Figure 6. Here XOR gate is used to compare every individual bit of present output Q with its corresponding input bit in the input data D, and consequently a single n-bit OR gate is used to detect if there are any bit changes by monitoring all the outputs of XORs.

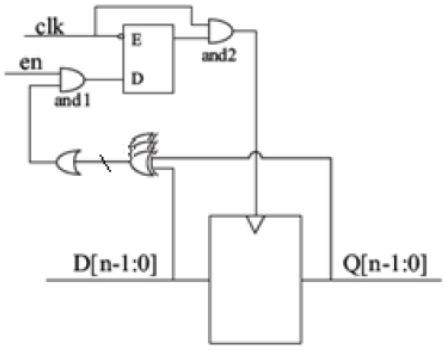

Fig -6: Enhanced clock gating implementation [8].

If the data does not change or enable is low, then the next clock toggle at the register should be disabled. Finally, with the aid of latch and AND gate, the clock can be disabled without encountering any glitches.

IV. IMPLEMENTATION

The RTL codes are developed for full adder using both the designs. The Verilog codes are then simulated using the Cadence NC Sim and the waveform obtained on the Graphical User Interface is used to verify the operation of the Adder incorporating the aforementioned optimization technique. Once the functionality of the circuit is verified using Cadence NCSim, the codes are then synthesized in Cadence RTL Compiler to obtain the final area, power and timing report.

The 32-bit adder is modified by adding 32-bit registers at inputs A & B and the output sum. This makes the design synchronous- a Register To Register path which requires the adder to perform and provide the required output in one clock cycle. Next parallelism with pipelining is implemented on this circuit. This involves addition of pipeline registers for every 8-bit adder. This enhances the throughput of the circuit and prevents data corruption. Input is split in 8-bits each and is then passed through 8-bit registers. Addition of first 8-bit is performed first and carry is passed on to next 8-bit stage. Since the carry and the sum of first 8-bit is available only after second clock cycle, we need to push the upper 24-bit inputs each by one clock cycle so that the sum evaluation happens at corresponding clock cycles. This process is continued and finally the output sum and carry are available after 5th clock cycle. The next technique implemented is enhanced clock gating. Here the inputs and outputs from registers are XORed to check if there is any change in bits. Only when there is a change, that enable is passed through the latch and then through the AND gate to the register.

V. RESULTS AND DISCUSSION

The codes for various power reduction techniques are written in Verilog and are simulated using Cadence NC Sim tool. Synthesis was performed for the aforementioned designs using Cadence RTL Compiler.
For a given set of inputs A=7FFFFFFF, B=7FFFFFFF, C_{in}=1 at 40000ps, the output values obtained are Sum=FFFFFFFF, C_{out}=0 which is depicted in the Figure 7.

The obtained results for two different variants of 1 bit Full adder are tabulated as shown in Table 1. Further, comparisons can be made with respect to different optimization techniques considering the performance parameters namely, Area, Power and Delay.

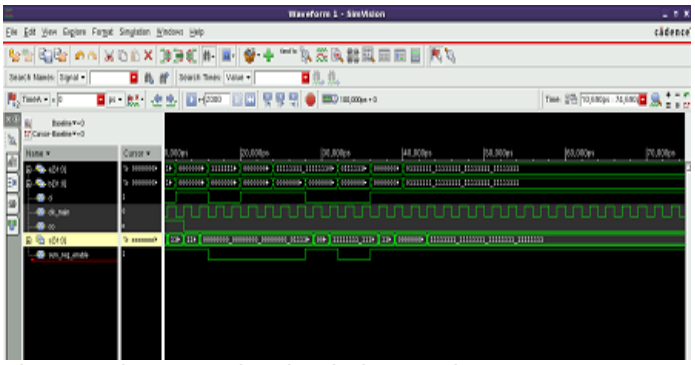

Fig -7: Cadence NC Sim Simulation result.

Table -1: Comparison of speed, power and area.

	Design 1			Design 2		
	Area (μm^2)	Power (μW)	Delay (ps)	Area (μm^2)	Power (μW)	Delay (ps)
Normal CSA	3489	265.491	957	3259	230.535	974
Parallel Pipeline	12767	822.549	575	12306	753.623	569
CCG	5484	113.346	584	5254	104.602	579
ECG	6493	149.909	730	6263	141.172	725

From the Table 1, it can be inferred that power reduction is more by employing clock gating techniques. The power consumption decreased drastically with the use of gating technique. In the both the adder designs, clock gating ensured enhanced performance of the CSA by lessening the power.

A power reduction of around 57.3% was obtained using Common Clock gating (CCG) for Design 1 and around 54.6% using Design 2 as compared to the conventional CSA. It is also evident that the delay was reduced by around 38.9% for Design 1 and by 40.55% for Design 2 in case of CSA which incorporated CCG.

A power reduction of around 43.5% was obtained using Enhanced Clock gating (ECG) for Design 1 and around 38.7% using Design 2 as compared to the conventional CSA. It is also evident that the delay was reduced by around 23.7% for Design 1 and by 25.5% for Design 2 in case of CSA which incorporated ECG.

Parallelism with pipelining technique yielded the largest improvement in speed which can be verified by the decrease in delay of almost 40% for Design 1 and 41.5% for Design 2 as observed from the table. However, the major ramification is the increase in area. While power and delay parameters enhanced the performance of the CSA, increase in area was an undesirable outcome. Thus it is imperative to perform trade- off between the essential performance parameters namely area, power and delay.

Through comparison between the two mentioned adder designs, it can be inferred that the second design provided better results with respect to the performance parameters. The power, area and delay for all the optimization techniques employed were reduced for the second adder design which can be verified from the tabulated results in Table 1. Thus it can be concluded that the CSA with adder design 2 improves the performance.

VI. CONCLUSIONS

Carry select adders are the most frequently used adders in computational circuits due to its characteristic of being practically faster than its traditional counterparts. Since it uses pre-computation logic and calculates sum and carry for each stage simultaneously through deployment of parallel computation, the delay for the carry propagation is reduced. However, the number of gates and overall area increase for the system. This is an undesirable effect. Thus, for a given design, trade-off must be performed for the performance parameters to meet the design specifications required.

This work employs RTL optimization techniques to reduce effective power consumption. By comparison among the techniques employed, it can be inferred that clock gating technique provides the best solution of around 43.5% and 38.75% reduction in power in the respective designs. Clock gating techniques produced best results with regards to power reduction for the designs used. If the speed of Adder is critical factor, then Parallelism with Pipelining can be implemented. However, this comes at cost of increased area. As a result, it is inevitable to perform trade-off to obtain the most feasible solution.

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