ENCODING SCHEME FOR POWER REDUCTION IN NoC

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ABSTRACT - As technology shrinks, the number of cores increases, total length of interconnection wires increases resulting in long transmission delay, larger area and higher power consumption. In multi core era, cores increases significantly on SoC, the system of communication also needs to change to support multi core communication. NoC is the best solution to scalability issue of future many core system and to deal with the complexity of designing next generation of many-cores architectures. Dynamic power dissipation in interconnects is a major contributor to power consumption in NoC links. In this paper we present the data encoding schemes to reduce the power dissipated by the links of NoC. The proposed scheme gives the advanced architecture which is general and transparent which allows to reduce 57% of the dynamic power dissipation and saves 26% area with the significant minimum delay that is 7.948ns and gives the 0.035J energy consumption .

Key Words: *Network-on-chip (NoC), data encoding, Power analysis.*

1. INTRODUCTION

As the number of IP cores integrated into SoC system increases, role of interconnection system become more and more important because these are the limiting factor for the performance and power in current and next generation SoC[10]. As number of cores increases, total length of interconnection wires increases resulting in long transmission delay, higher power consumption. Another problem is the length of wires decreases with technology, it will increase coupling capacitance and height of wire material increases resulting in fringe capacitance. [7].

The importance of interconnects complex many-cores chips has outrun the importance of Transistors as a dominant factor of performance, power, cost and reliability Sophisticate on-chip communication protocols, involving advanced adaptive routing algorithms, selection policies, data protection schemes and mechanisms aimed at guarantee the quality-of-service are pushing the interconnect system to become one of the main elements which characterizes the system in terms of both power dissipation and energy consumption[4].

Dynamic power dissipation in interconnects is a major contributor to power consumption in NoC links. This is mainly due to two factors, self switching activity of the particular link and coupling switching activity among adjacent links dissipate power due to the switching activity both self and coupling induced by subsequent data patterns traversing the link. The interconnection network dissipates a significant fraction of the total system power. The requirements for encoding are very tight[8].

In this paper, we will try to reduce the power dissipation of NoC by reducing the network interface power. We will present a hardware design of a low power Network interface design. The dynamic power reduction is also obtained by the implementation mechanism on stoppable clock technique and by designing the new advanced architecture of the encoding schemes for dynamic power saving. There are many work in literature which deal with power and energy consumption issues in network on chip. They are different by either the level of abstraction in which they operate or by particular element in NoC they focus on. In this paper we are targeting the three factors power, energy and area. The proposed methodology will focus on the dynamic power which is dissipated by netwok link.

2. PREVIOUS WORK

Deepa.N.Sarmaet.al.in paper[1]has entitled "A Novel Encoding Scheme For Low Power in NoC links" which is proposed on the reduction in power in network links. Dynamic power dissipation in interconnects is a major contributor to power consumption in Network on Chips (NoCs)[4]. This paper mainly focused on the two factors, self switching activity of the particular link and coupling switching activity among adjacent links. Novel encoding techniques is also called two stage encoding technique and it is proposed to reduce power consumption due to switching transition and crosstalk. Encoder and Decoder exhibiting the proposed scheme have been described in RTL level in Verilog HDL, synthesized and mapped into UMC180nm technology library. It has been observed that the two stage encoding technique offers an average reduction in dynamic power consumption of 17.34%[1].

M.VenkataTheerthaet.al in paper[2] entitled "SCDBI Encoding Scheme for NOC Links" proposed on the

power reduction and impact on area is very less. By using this method we can reduce the switching power by 34.64% without any significant degradation in area and performance. The SCDBI Encoding Scheme gives better power reduction in between the links. The power dissipated by the links of a NoC contribute significant fraction of the total power budget. This paper proposed the use of data encoding techniques as a viable way to reduce power dissipation in NOC links.

NimaJafarzadehet.al in paper[4] entitled "Data Encoding Techniques for Reducing Energy Consumption in Network-on-Chip" proposed efficient power reduction than the previous paper. This paper presented a set of data encoding schemes aimed at reducing the power dissipated by the links of NoC. The proposed schemes are general and transparent with respect to the underlying NoC fabric. Experiments carried out on both synthetic and real traffic scenarios show the effectiveness of the proposed schemes, which allow to save up to 51% of power dissipation and 14% of energy consumption without any significant performance degradation and with less than 15% area overhead in the NI.

3. EXPERIMENTAL STUDY

We have used the 65-nm UMC technology and methodology of transition data. Our aim is to reduce the power consumption, energy consumption, delay and area. For that we have used the advanced architecture by changing the previous one architecture. This paper is proposed to reduced the power consumption by changing the architecture by using the x-or gate with D flip flop or by T flip flop. The D latch or T latch can also be used. As in the previous architecture the different links are connected and we will get the output on the different links in different times. In this case it dissipates much more power in that links. In previous paper we use the X-OR gates and got out-put in different links at random time it dissipates the more power. So we are modifying this architecture and try to collect the output on a single link so power will reduce.

We will achieve this by using D flip flop and X-OR gates or replace this by using T flip flop. The advantage of the D flip flop is that it increases the static power but reduces the dynamic power as well as it gives less delay with less area and less energy consumption. This helps us to achieve our goal.

In this paper we have focused on data encoding scheme which gives an effective power reduction in NoC Links. We have used the same encoding but modifying the architecture of the encoder with the different transition. We have targeted the four factors that are power reduction, reduction in delay, energy consumption and less area. By modifying the architecture of the encoder scheme we have achieved the target. This advanced Encoding scheme achieved the target whose goal is to reduce power dissipation by minimizing the coupling transition activities on the links of the interconnection network.

4. RESULT

First the input is given to the serial input parallel output(SIPO) and after that output is given to the encoder. In this paper we have designed the three schemes of encoder with the different transition. All the simulation is compared with each other. Encoder scheme first gives the efficient result than the others. Encoder and Decoder exhibiting the proposed scheme have been described in RTL level in Verilog HDL.

Fig 1. shows the result of power reduction. It gives the dynamic power dissipation is 7mW. The ideal power dissipation is 11mW. The dynamic power dissipation after simulation is 7mW. The percentage of power is calculated by the ideal and actual power. The proposed scheme reduces 57% power dissipation. ((ideal power-actual power)/actual power)*100

Ex.((11mW-7mW)/7mW)*100=57.14%

As the result is compared with the previous paper[4]it gives the more effective power reduction that is 57.14%. It provides the minimum delay and that is 7.948ns as shown in the fig 3. This delay is compared with other encoder scheme that we have designed. The proposed work saves upto the 26%area and the previous work saves 15% area as shown in fig 2. Energy consumption is calculated by dynamic power and real time

Ex. Energy =power*time

=0.007W*5s

=0.035J

Figure 4. shows the RTL of encoder.

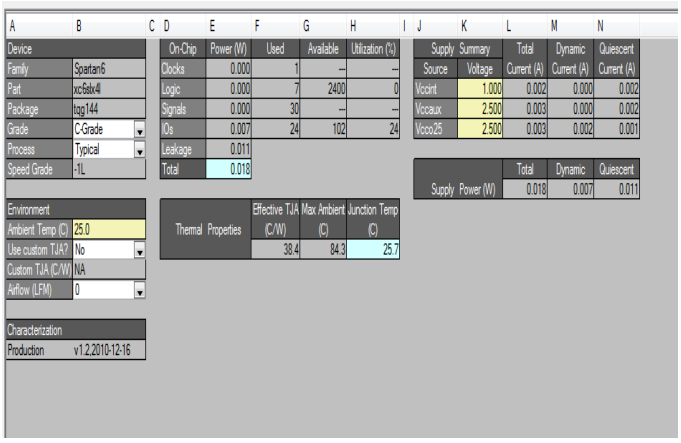

Fig -1: Power Analysis

encoder Project Status			
Project File:	blocks.xise	Parser Errors:	No Errors
Module Name:	encoder	Implementation State:	Synthesized
Target Device:	xc3s50-5pq208	•Errors:	No Errors
Product Version:	ISE 13.1	•Warnings:	9 Warnings (9 new)
Design Goal:	Balanced	•Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	•Timing Constraints:	
Environment:	System Settings	•Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	14	768	1%
Number of Slice Flip Flops	4	1536	0%
Number of 4 input LUTs	26	1536	1%
Number of bonded IOBs	24	124	19%

Fig -2: Area analysis

```
m_1__and0000(m_1__and000011:0)     | NONE(m_1)          | 1     |
m_1__and0001(m_1__and000111:0)     | NONE(m_1)          | 1     |
m_3__and0000(m_3__and000011:0)     | NONE(m_3)          | 1     |
m_3__and0001(m_3__and000111:0)     | NONE(m_3)          | 1     |
m_5__and0000(m_5__and000011:0)     | NONE(m_5)          | 1     |
m_5__and0001(m_5__and000111:0)     | NONE(m_5)          | 1     |
m_7__and0001(m_7__and00011:0)      | NONE(m_7)          | 1     |
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Timing Summary:
---------------
Speed Grade: -5

   Minimum period: No path found
   Minimum input arrival time before clock: 5.237ns
   Maximum output required time after clock: 7.596ns
   Maximum combinational path delay: 7.948ns

Timing Detail:
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All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'w8<7>'
  Total number of paths / destination ports: 71 / 4
-------------------------------------------------------------------------
```

Fig -3: Delay analysis

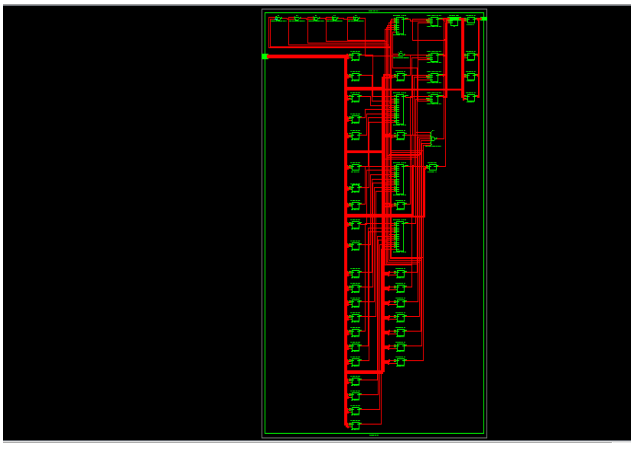

Fig -4: RTL of encoder

5. CONCLUSION

Most of power is dissipated by links, routers and network interface. In all the papers they focused on the power reduction by using encoding technique. The novel encoding technique reduced power 17.34%. the result of novel encoding is compared with BI encoding. The power reduction of novel encoding is better than the BI encoding. SCDBI encoding reduced power 34.67% and area is 8%. But data encoding is more effective as it gives 51% power reduction and also 14% of energy consumption[4].The praposed shceme gives the advanced architecture with general and transparent with respect to the underlying NoC fabric. It has achieved the effectiveness of the praposed schemes which allows to reduce 57% power dissipation and saves 26% area with the significant minimum delay that is 7.948ns and gives the 0.035J energy consumption .

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