

Power Efficient Carry Select Adder using D-Latch

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Abstract - Carry Select Adder (CSLA) is faster than any other adders used in many data-processing processors to perform arithmetic functions speedily. By observing the structure of the CSLA, it is clear that there is way for reducing the area and power consumption. This work uses a sophisticated and efficient gate-level modification to significantly reduce the area and power of the carry select adder. Conventional carry-select adder is still area-consuming due to the dual ripple carry adder structure. The excessive area overhead makes CSL relatively unconditional but this has been circumvented by the use of add-one circuit introduced recently. The logic operations involved in conventional carry select adder (CSLA) and binary to excess-1 converter BEC based CSLA are analyzed to study the data dependency and to identify minimized logic operations. The sum for each bit position in an elementary adder generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. Experimental analysis shows that the architecture achieves the three folded advantages in terms of area, delay and power [3]. This paper introduces a proposed logic block as a D latch with replacing RCA block in conventional design to evaluate the power consumption and area. In order to minimize area and power of 16 bit carry select adder we have replaced a BEC with D latch [3].

Key Words: power efficient, area efficient, CSLA, D-Latch, etc...

1. INTRODUCTION

Carry Select adder designing involves ripple carry adder pairs which will work for summation either for $C_{in} = 0$ or and $C_{in} = 1$. Ripple carry adder is one of the adder which added three digit and reflects carry bit into next process. In conventional design two RCA's are used for summation for $C_{in} = 0$ and $C_{in} = 1$ and final selection process will be carried out by multiplexer. Binary to Excess one converter

is just the replacement of one RCA block for $C_{in} = 1$ in regular design because it gives added sum by considering $C_{in} = 1$. This paper describes the designing methodology of various fundamentals logic design simulation which helps in making the process running as in digital adder speed of addition is limited by propagation of carry through adder. Adders is an almost obligatory component of every contemporary integrated circuit. The prerequisite of the adder is that it is primarily fast and secondarily efficient in terms of power consumption and chip area. This paper presents the choice of selecting the adder topologies. The adder topology used in designing carry select adder work are ripple carry adder, binary to excess one converter and D-latch. Addition is an indispensable operation for any digital system, DSP or control system. Adders are also very significant component in digital systems because of their widespread use in other basic digital operations such as subtraction, multiplication and division. Hence, for improving the performance of the digital adder would extensively advance the execution of binary operations inside a circuit compromised of such blocks. Ripple carry adder is the simplest but slowest adders with n operand size in bits. The carry-ripple adder is composed of many cascaded single-bit full-adders. As in initial conventional case each part of adder is composed of two carry ripple adders with c_{in_0} and c_{in_1} , respectively. Through the multiplexer, we can select the correct output result according to the logic state of carry-in signal. The carry-select adder can compute faster because the current adder stage does not need to wait the previous stage's carry-out signal. Next we replace this ripple carry adder with BEC (Binary to Excess-1) converter in second terminology and in next one this BEC is also replace D latch as proposed here because latches are used to store one bit information.

2. LITERATURE REVIEW

Author Ram Kumar et al. proposed a design which replaces a ripple carry block in conventional CSLA design with BEC-1 block named as binary to recess one converter. The main idea of this work is to use BEC instead of the RCA because with BEC-1 in order to reduce the area and power consumption is reduced than the regular CSLA. The idea is to use binary to excess one converter instead of RCA with carry is equal to one [3]. The deficiency in this project that

it will increased delay slightly greater than previous technique.

Author Yajuan .He and et.al described an area efficient square root CSL scheme based on a new first zero detection logic. This carry-select adder partitions the adder into several groups, each of which performs two additions in parallel. Therefore, two copies of ripple-carry adder act as carry evaluation block per select stage. One copy evaluates the carry chain assuming the block carry-in is zero, while the other assumes it to be one [1].

Paper by I-Chyn Wey, Cheng-Chen Ho, Yi-Sheng Lin, and Chien-Chang Peng proposed area efficient carry select adder by sharing the common boolean logic term. After boolean simplification, they can remove the duplicated adder cells in the conventional carry select adder. Alternatively, they generate duplicate carry-out and sum signal in each single bit adder cell [16].

The paper by Basant Kumar Mohanty and et.all proposed a new idea to made the performance of CSLA is fast instead with the use of BEC-1. They have designed a new logic formulation for CSLA. The carry select operation is scheduled before calculation of final sum which is different from conventional approach. They have used one RCA and one add one circuit instead of two RCA circuit. This method is known as sort of analysis because it divides main logic of operation into two parts first part gives half sum and carry calculation as it has done by HSC generator means half sum and carry generator and rest of the calculation part will be done by FSC (Full Carry Sum) generator . Therefore original sum and carry will be obtained by performing both this operation. There is consumption of quite large time to produced result sum.

3. METHODOLOGY

In this paper our basic approach is simply to design 16 bit carry select adder with D latch, which will minimized the power consumption as well as area in comparative with 16 bit carry select adder, here we refer as a base paper [3]. So here we have to make a comparative design study between BEC based CSLA and D latch based CSLA, as proposed. The involvement of blocks is as follows.

3.1 BINARY TO EXCESS ONE CONVERTER

The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. The logic diagram of BEC as follows.

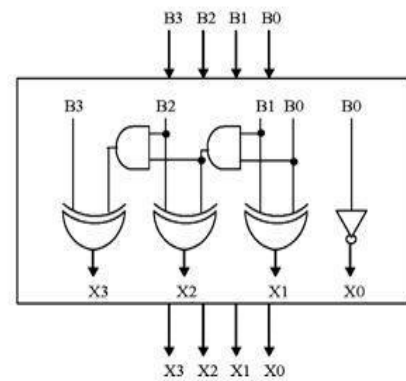


Chart -1: Block diagram of 4 bit BEC

Truth Table:-

B[3:0]	X[3:0]
0000	0001
0001	0010
0010	0011
0011	0100

3.2 CSLA USING BEC [BINARY TO EXCESS ONE]

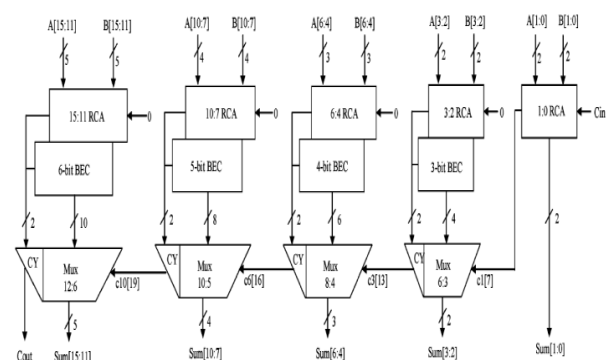


Chart-2: Block diagram of CSLA using BEC

The structure of 16 bit CSLA using BEC instead of RCA with Cin=1 to optimize the area and power is shown in Fig. 2. One input to the multiplexer goes from the RCA with Cin=0 and other input from the BEC. It is clear that BEC structure reduces the area and power. But the disadvantage of BEC method is that the delay may increase slightly than the regular CSLA.

3.3 D LATCH TERMINOLOGY

To compensate power consumption in previous technology we are proposing a new technique with D latch. D latches are used for load and store operation because it will give output as one when clock is equal to one.

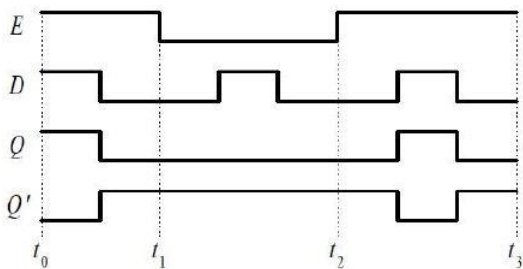


Chart 3:- waveform of D latch

Latches are used to store one bit information. The outputs are constantly affected by the inputs as long as the enable signal is asserted. In other words, when they are enabled, contents changes immediately according to the inputs. D-latch and it's waveforms are shown in chart 3.

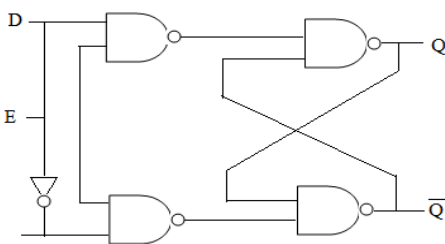


Chart 4:- Flip flop structure of D latch

3.4 CSLA USING D LATCH

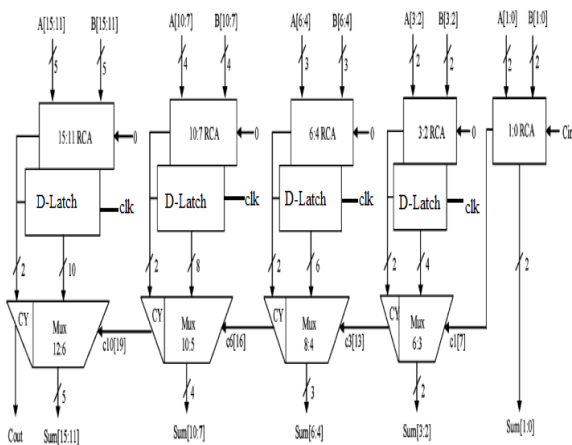


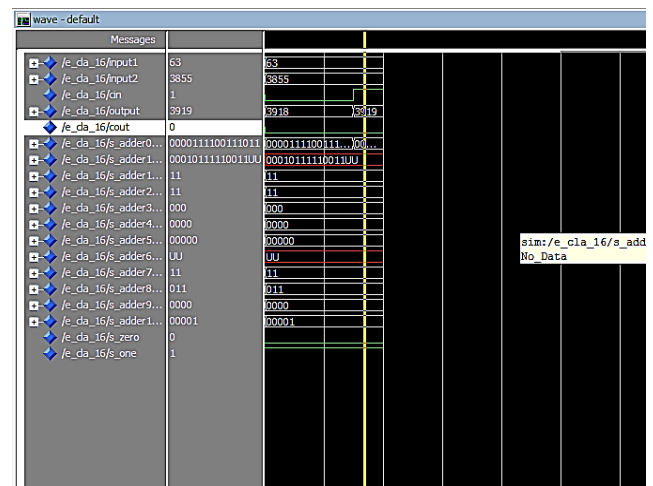
Chart 5:- Block diagram of CSLA using D Latch

This proposed architecture of 16 bit CSLA using D latch consists of five clusters of bit word size starting from n bit RCA and D latch later on 3b, 4b, 5b, 6b word size simultaneously. Instead of using two separate adders in regular CSLA, in this method only one adder is used to reduce area, power consumption and delay and each of two addition is performed in one clock cycle. In this 16-b

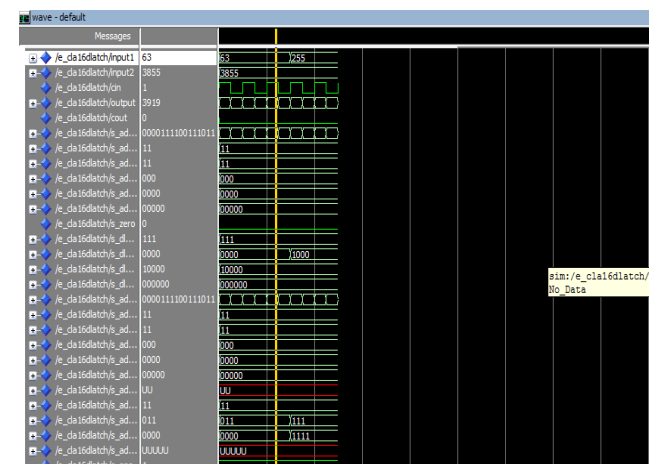
adder the LSB is ripple carry adder which is 2 bit. The upper half of adder i.e. MSB which is 14-b wide works on the principal of clock. Whenever clock goes high the addition for carry input zero is performed and when clock goes low carry is assumed to be zero and addition is stored in adder itself. Carry out from the previous stage i.e., least significant bit adder is used as control signal for multiplexer to select final output carry and sum of the 16-bit adder. If the actual carry input is one, then computed sum and carry latch is accessed and for carry input zero MSB adder is accessed. Cout is the output carry.

4. SIMULATION RESULT

1. 16 BIT CSLA USING BEC



2. 16 BIT CSLA USING D LATCH



5. COMPARISON TABLE

Name	Delay [ns]	Power (UW)	Technology [nm]
conventional version [using BEC][3]	17.76	220	0.18
Modified Version [using D Latch]	24.57	160	65 To 90

Table No:-1

All practical simulation results are shown in the table shows that practical simulation values of parameters with the help of software XILINX.

Logic Utilization	No. of LUT	No. of slices	No. of IOB	Total
Regular version	60	33	50	143
Proposed Version	32	24	50	106

Table No:-2

From the table we have concluded that the CSLA using D latch will give reduce power output than using CSLA using BEC. Here among two powers i.e. data power and I/O power we have reduce data power to great extent, but delay should be increased as number of logic blocks could get increased. Similarly area is also reduced as shown below but this area is the individual addition of (slices + lut's +I/O, s) as used in the design. Hence we cannot define in particular unit. Ratings should be changed for different FPGA technology if we consider implementation of this design yet it is not discussed here

6. CONCLUSIONS

D-latch is a circuit which gives an output if status of clock is active else result won't get latched for next stage come after. By considering all circuit study it is concluded that proposed design will show the values of component parameter such as power and delay in reduced manner with earlier version as it is design methodology of BEC.

REFERENCES

[1]Yajun. He, C. H. Chang, and J. Gu, "An area-efficient 64-bit square root carry select adder for low power application," in Proc. IEEE Int. Symp. Circuits Syst., 2005, vol. 4, pp. 4082–4085.

[2]B. Ramkumar, H.M. Kittur, and P. M. Kannan, "ASIC implementation of modified faster carry save adder," Eur. J. Sci. Res., vol. 42, no. 1, pp. 53–58, 2010.

[3]B. Ramkumar and H.M. Kittur, "Low-power and area-efficient carry-select adder," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 2pp. 371–375, Feb. 2012.

[4]Area-Delay-Power Efficient Carry-Select Adder Basant Kumar Mohanty, Senior Member, IEEE, and Sujit Kumar Patel, IEEE Transaction On Circuit And System-i:Express Briefs, Vol 61, No 6, June 2014.

[5] Y.Kim and L-S Kim, "64-bit carry select adder " IEEE Transactions On Circuits And Systems-Ii: Express Briefs, Vol. 61, No. 6, June 2014.

[6]S.Manju and V. Sornagopal, "An efficient SQR architecture of carry select adder design by common Boolean logic," in Proc. VLSI ICEVENT, 2013,pp. 1–5.

[7]B.Parhami, Computer Arithmetic: Algorithms and Hardware Designs,2nd ed. NewYork, NY, USA: Oxford Univ. Press, 2010.

[8]R.UMA,Vidya Vijayan, M. Mohanapriya, Sharon Paul2, "Area, Delay and Power Comparison of Adder Topologies" International Journal of VLSI design Communication Systems (VLSICS) Vol.3, No.1, February 2012.

[9]O. J. Bedrij, "Carry-select adder," IRE Trans. Electron. Comput.,vol. EC-11, no. 3, pp. 340–344, Jun. 1962.

[10]A. P. Chandrakasan, N. Verma, and D. C. Daly, "Ultralow-power electronics for biomedical applications," Annu. Rev. Biomed. Eng., vol. 10, pp. 247–274, Aug. 2008.

[11]B. Parhami, Computer Arithmetic: Algorithms and Hardware Designs,2nd ed.New York, NY, USA: Oxford Univ. Press, 2010.

[12]K. K. Parhi, VLSI Digital Signal Processing. New York, NY, USA:Wiley,1998.

[13]J. M. Rabaey, Digital Integrated Circuits," IEEE Trans. on VLSI Systems, 2003.

[14]O. J. Bedrij, "Carry-select adder," IRE Trans. Electron. Comput., pp. 340–344, 1962.

[16] I-Chyn Wey, Cheng-Chen Ho, Yi-Sheng Lin, and Chien-Chang Peng, " An Area-Efficient Carry Select Adder Design by Sharing the Common Boolean Logic Term" in Proceedings of International MultiConference of Engineers and Computer scientist 2012 Vol II, IMECS 2012, March 14-16, 2012, Hong-Kong.

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