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DESIGN AND ANALYSIS OF DIGITAL PID CONTROLLER

Bhakti Khandalkar[1], Asst Prof. Amit Lamba[2], Asst Prof. Vipin Bhure[3]

[1] *M.tech Student, Electronics and Communication Department, GHRAET, Maharashtra, India*
[2] *Assistant Professor, Electronics and Communication Department, GHRAET, Maharashtra ,India*
[3] *Assistant Professo , Electronics and Communication Department, GHRAET, Maharashtra ,India*

Abstract - *The digital Proportional-Integral-Derivative (PID) controller is the feedback system which is most wildly used in automation industries.PID controller play an important role in industry because of its excellent properties like simplicity, robustness, good noise tolerance and maintenance requirement. This paper present a novel technique for design and analysis of structure of a digital Proportional – Integral – Derivative (PID) controller. In this paper controller design, synthesis and analysis is done using Xlinx 13.1 ISE software with verilog code. In this paper we explain design strategy of digital PID controller .Main focus of this paper is to reduce delay and increase speed of the system. In order to achieve this task we use pipelined multiplier and optimized adder which will improve the overall performance of the digital PID controller.*

Key Words: Digital PID controller, High speed adder and pipelined multiplier

1. INTRODUCTION

The PID controller has been widely used over the past five decades and it is the most commonly used control system which has longest history. However, now a day also this method is extensively in used .Simplicity, robustness, and effectiveness are some properties of the Proportional-Integral-Derivative (PID) controllers .They are not susceptible to environmental noise and very easy to reconfigure .Introduction of the speed and position control Loops in the motion control systems, to achieve fast response and high accuracy, is a very popular technique in industry.[5]Despite the numerous control design approaches, now a day's PID controllers are still employed in more than 95% of industrial processes. Proportional integral-derivative (PID) controllers are the most adopted controllers in industrial settings because of the advantageous cost/benefit ratio they are able to provide.

Although there are numerous developments in advanced control theory, the Proportional-Integral-Derivative(PID) controller are still dominating in the motion control systems in the industry due to the well acquaintance of the operating personnel with PID controllers. Therefore, digital PID controllers are replacing of their analog counterpart in the industrial motion control systems due to popularity of digital control as we discuss above. The digital controllers available at present also suffer from quantization error, differential linearity error (DNE), integral linearity error (INE) and also the non-monotonicity due to the use of analog - digital converters. Thus the controllers, despite having an ingenious design, suffer from errors. [2] There are various application of PID controller The area in which PID controller are use such as process control, aerospace, robotics, automation, manufacturing, and transportation system[1].

In this project Digital PID controller is used. PID controllers have evolved from analog controllers to digital controllers. The digital domain of control mechanism is less expensive than its analog counterpart; also it is easy to implement the advanced control algorithm. Other advantages of digital domain of control strategies include flexibility in changing parameter, lighter weight and greater insensitivity to noisy external signals. Therefore digital PID controller taking the place of their analog counterpart in the industrial control systems due to the widespread popularity of digital control system [1].

2. BACKGROUND

A. 2.1 Basics Of Controller

A control system consists of two subsystems, a plant and a controller. The plant is an entity controlled by the Controller. The controller can be either analog or digital. Generally, an implementation of digital PID controller includes the use of microprocessors or microcontrollers. The memory holds the application on program while the processor fetches, decodes, and executes the program instructions

This method has a disadvantage in speed of operations because the operations depend on software which has a sequence of instructions and commands which needs many machine cycles to execute. [3]

Controllers can be divided into two main groups

1. Conventional controllers

2. Unconventional controllers

Conventional controllers include controller such as P, PI, PD, PID, Otto-Smith, all their different types and realizations. It is a characteristic of all conventional controllers that one has to know a mathematical model of the process in order to design a controller. Unconventional controllers utilize a new approaches to the controller design in which knowledge of a mathematical model of a process generally is not required. Examples of unconventional controller are a fuzzy controller and neuro or neuro-fuzzy controllers. However, it is known that a good many nonlinear processes can satisfactory controlled using PID controllers providing that controller parameters are tuned well. Instead of using a small number of complex controllers, a larger number of simple PID controllers are used to control simpler processes in an industrial assembly in order to automate the certain more complex process. [4]

2.2 PID Algorithm

The digital PID controller is the feedback controller .It is divided into two parts main part PID controller and closed loop system. A system in which the control action is somehow depending on the output is called closed loop system. Closed loop system consist of reference input r(t),Feedback signal y(t),Error signal e(t),Control o/p u(t), Plant/Process. The PID algorithm consists of three basic modes, Proportional, Integral and Derivative modes. While utilizing this algorithm it is necessary to decide which modes are to be used (P, I or D) and then specify the parameters (or settings) for each mode used. Generally, three basic algorithms are used P, PI or PID [5].

The PID controller minimizes the error by changing the controller output, which is given as an input to the system. Proportional is related with present error, Integral on the past one and Derivative means prediction about the future errors. Sum of the each term, multiplying with respective gain gives the output of PID controller [6].

The general PID equation is given as,

$$u(t) = K\left(e(t) + \frac{1}{T_i}\int_0^t e(t)\,dt + T_d\frac{d}{dt}e(t)\right) \quad \text{------(A)}$$

Where,

e(t) is error signal, u(t) is output of controller, K is gain or proportion gain, Ti is Integration time or rise time, Td is Derivative time[3,6].

Equation A is given in time domain form, in discreet form it can be given as follows

sigma=Ki*e(n)+sigma

u(n)=(Kp+Kd)*e(n)+sigma+Kd*(-e(n-1).

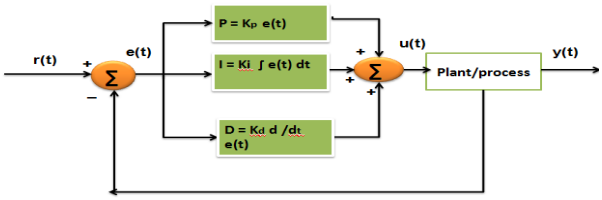

Fig -1: Generic system controlled by PID controller

The function of the digital PID controller is to generate an output that drives the system at the plant so that the output matches a reference signal. The target is to get the error as close to zero as possible.

2.3 Pipeline Multiplier

B. Pipeline technology plays an important role in present parallel computers in improving the speed of the computer. In a pipeline a task is divided into subtask and subtasks are executed simultaneously. For large scale computation pipeline is the best solution to perform fast operation .In the enhanced method a pipeline is incorporated to carry the MSB of the operands. Pipelining is an important technique used in several applications such as digital signal processing and microprocessor.

C. Generally basic pipeline consists of latches and stages as shown in figure. The stages are the intermediate logic elements, where computations are performed. The results of these computation elements are feed forward to the next stages by latches. The operands which are left for computations in the next machine cycle are also feed forward through latches to next stages. Pipelining is the possible approach to speed-up the clock frequency. It is an important technique used in several applications such as digital signal processing (DSP) systems, microprocessors, etc. Accordingly, it results in speed enhancement for the critical path in most systems. [11]

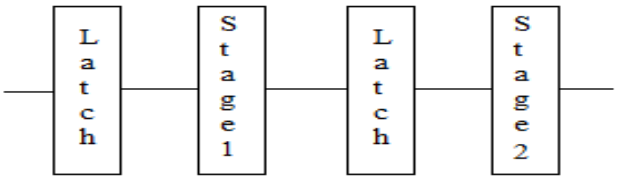

Fig -2: Pipelined multiplier

2.4 Booths Multiplier

Booths algorithm gives a procedure for multiplying binary integers in signed 2's complement form. Booths

algorithm requries examination of the multiplier bits,and shifting of partial product. [3] It is an efficient means of multiplying signed numbers.Signed-number multiplication, consider both positive and negative numbers uniformly.Thus reduce the number of multiplicand multiples. This advantage can save both area and time in the circuit. Booth Developed following algorithm If the two adjacent multiplier bits are
same (00or11) then shift .
01 add multiplicand to left half of product
10 subtract multiplicand from left half of product

2.5 Han-Carlson Adder

The different types of parallel prefix adders available are Kogge-Stone adder, Brent-kung adder, Sklansky adder, T. Han and D.A. Carlson presented a hybrid construction of a parallel prefix adder using two designs the Kogge-Stone construction having the best feature of higher speed and the Brent-kung construction with best feature of low area requirement. A modified Han-Carlson adder uses fewer number of prefix operations by adjusting the number of stages amongst Kogge-Stone and Brent-kung adder and thus reduces the area required by the adder circuit

3. PROPOSED DESIGN TECHNIQUE

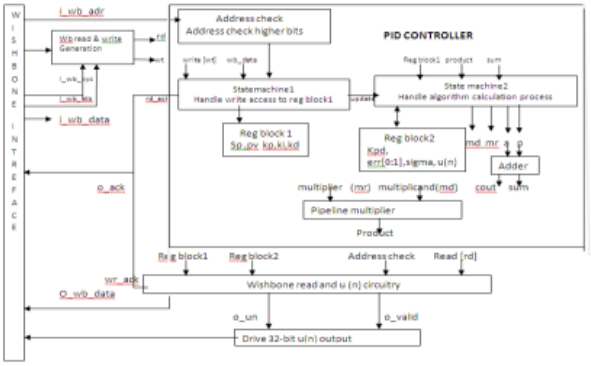

Fig -3: Proposed PID controller block diagram

The block diagram as above, is basically divided into three main blocks
1.State machine1
2.State machine2.
3.Wishbone interface.
All the digital inputs and outputs required for main PID controller is passing through wishbone interface.

Table 1 show all control signal of wishbone interface.

Name	Name in Wishbone	Size	Direction	Description
i_clk	CLK_I	1	input	Clock input
i_rst	RST_I	1	input	Reset input
i_wb_cyc	CYC_I	1	input	Indicates valid bus cycle (core select)
i_wb_stb	STB_I	1	input	Indicates valid data transfer cycle
i_wb_we	WE_I	1	input	Write transaction when asserted high
i_wb_adr	ADR_I	16	input	Address input
i_wb_data	DAT_I	16/32/64	input	Data input
o_wb_ack	ACK_O	1	output	Acknowledgment output (indicates normal transaction termination)
o_wb_data	DATA_O	16/32/64	output	Data output

Table -1: Control Signals of Wishbone architecture

The process of PID controller is based on finite state machine.
State machine1-When state machine 1 gets all required input signal from wishbone interface it will handle register block1 which consist of 16-bit signed coefficient and data input: Kp, Ki, Kd, SP and PV. Ki, Kp, Kd, SP, PV can be updated anytime after reset. After every update of Kp or Kd, register Kpd which stores Kp+Kd will be calculated and updated.
State machine 2- handle register block 2 which consist of Kpd, err(0,1),sigma and u(n). All algorithmic calculation process is performing in this block. After every update of PV, calculation and update of e(n), e(n-1),sigma and u(n) will be triggered in sequence.
In pipeline multiplier,booths multiplier and hancarlson adder work parallel because of which overall delay requirement is less .Thus the output of pipeline multiplier and adder is given to state machine2.
IN order to provide output signal to wishbone interface, reg block1 ,,reg block2,rd, reg check signals are given to the wishbone read and u(n) circuitry(fig4), which generate output signal o_u(n), o_valid .After getting read acknowledge signal this output signal is given to wishbone interface through o_wb_data. Thus in this way output of PID controller is given to wishbone interface.

3.1 Coefficients And Data Update

Coefficients (Kp, Ki, Kd, SP) and measured process value (PV), which are all16-bit signed number in two's compliment, are stored in different registers that can be read and written any time after reset. Normally, Kp, Ki, Kd, Sp are updated right after reset before continuously update of PV. In this paper, we can update coefficients randomly for dynamic tuning. Writing action to specific registers mentioned above won't be responded until finished calculation of the last u(n).

Table 2 explains read and writes operation of input and output terms

Kp	R/W	Stores coefficient Kp
Ki	R/W	Stores coefficient Ki
Kd	R/W	Stores coefficient Kd
SP	R/W	Stores reference SP
PV	R/W	Stores PV
Kpd		Stores coefficient Kp+Kd
err[0]		Stores e(n)
err[1]		Stores e(n-1)
Un		Stores u(n)

Table -2: Input and Output signals

3.2 Example For Calculation

From above explanation we known that,

sigma=Ki*e(n)+sigma----------(1)
u(n)=(Kp+Kd)*e(n)+sigma +Kd*(-e(n-1)---------(2)

thus if, ki=,129 ,kd=130,kp=128,

e(n)=err(0)=0

e(n-1)=err(1)=0

therefore, (1) and (2)becomes

sigma=21878529(previous value)

sigma=129(0)+21878529

i.e sigma=21878529----------(3)

putting (3) in (2) we get

u(n)=(128+130)*0+21878529+5*0

u(n)=21878529

4. RESULTS

In this section we have given the simulated result of digital PID controller obtained from verilog code. In this simulation, test bench is observing in form of waveforms according to which output waveform is generated.

The following figures show RTL view and simulated result of digital PID controller.

4.1 RTL View

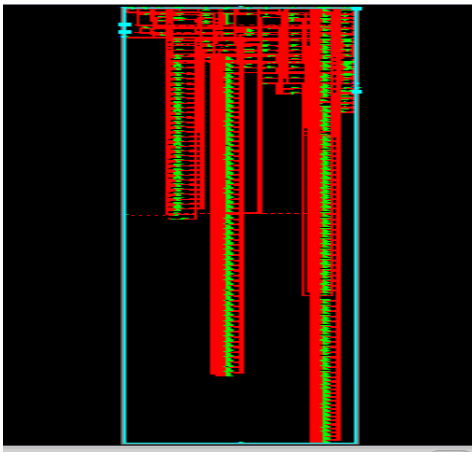

Fig -4: RTL View of Digital PID Controller

4.2 Simulation Result

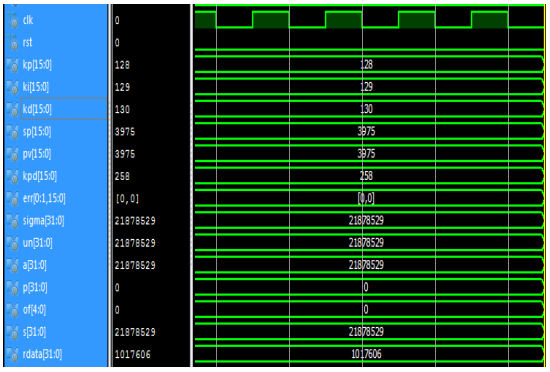

Fig -5: Simulation Result of Digital PID Controller

4.3 Device Utilization Summary

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	339	960	35%
Number of Slice Flip Flops	118	1920	6%
Number of 4 input LUTs	640	1920	33%
Number of bonded IOBs	68	108	62%
Number of GCLKs	1	24	4%

5. CONCLUSION

In this paper we have successfully design digital PID controller on Xilinx 13.1 software with verilog preferred language. From the above results which we obtained the operating frequency of the system is 100.34 MHz. Therefore time requirement is 9.96usec.And overall delay requirement of the controller is 9.966ns.Thus from this results we can achieve high speed as well as better performance.

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