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Analysis of RF CMOS Low Noise Amplifier at Different Operating Frequency & Technology

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Abstract - *This paper presents analysis of low noise amplifier (LNA) used for wireless application as RF front end operating at frequency of 2.47GHz. Different LNA analyzed in this paper are designed with different CMOS technologies. Recent works in designing LNA shows that there has been a difficulty in attaining both low noise figure and low power consumption simultaneously. This paper shows comparative analysis of different LNA designed in past few years so that we can try to improve the different parameters of LNA such as noise figure, supply voltage ,power consumption etc .this paper also gives comparative analysis of different CMOS technologies such that one can choose it for his* ***design purpose. We used "ADVANCED DESIGN SYSTEM"*** *for simulation purpose. It is easy to understand and user friendly tool. ADS is the* ***"Hi****-Frequency & Hi-****Speed"*** *platform for IC, Package and Board Co-Design.*

Key Words: ADS, CMOS, Gain, LNA, Noise figure, etc…

1. INTRODUTION

Radio frequency (RF) devices receive and transmit signals from 3 kHz to 300 GHz, covering a variety of wireless applications. For example, new generations of cellular phones (4G) have just been available for a couple of years. Moreover, wireless local area network (Wi-Fi) is gaining popularity for laptop, tablet and Smartphone, since Wi-Fi can provide access to the Internet via an access point (hotspot). Campus-wide Wi-Fi and city-wide Wi-Fi are further providing convenience for these users. Since wireless communication enables voice, data, image and video to be transferred to anywhere almost instantaneously, the impact of RF on people's daily lives has become significant.

The design of RF applications involves an important component known as the low-noise amplifier (LNA). The LNA is an essential component located at the first stage of a radio receiver. The major function of an LNA is to amplify very weak signals i.e. it increases the strength of signal while adding as little noise and distortion as possible. The optimization of low-noise amplifiers will minimize noise and improve noise figure, which is extremely important features CMOS technology is receiving much attention.

Recent works in designing of LNA shows that it's very difficult to achieve low noise figure and low power consumption. This paper gives comparative analysis of different LNA designed in past few years so that we can try to improve the different parameters of LNA such as noise figure, supply voltage, power consumption etc using different CMOS technologies so that one can choose it for his design purpose. Paper is divided into five sections: section 2 describes LNA topologies, section 3 describes recent research, section 4 objective of proposed design and section 5 conclusion.

2. LNA TOPOLOGIES

There are different LNA topologies available for design purpose with different parameters.

- Resistive termination
- Common Gate
- Shunt series feedback

2.1 Resistive Termination:

In resistive termination topology, a 50 Ω resistor (R) is simply placed across the input terminals of a common-source amplifier (Figure 1) with a source resistance (R_S) and an output resistance (R_L). However, this additional resistor introduces thermal noise and attenuates the signal before the transistor, resulting in unacceptably high noise.

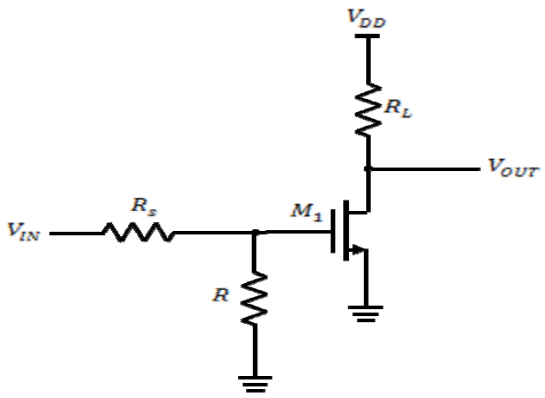

Fig -1: Common-source amplifier with resistive termination

2.2 Shunt series feedback:

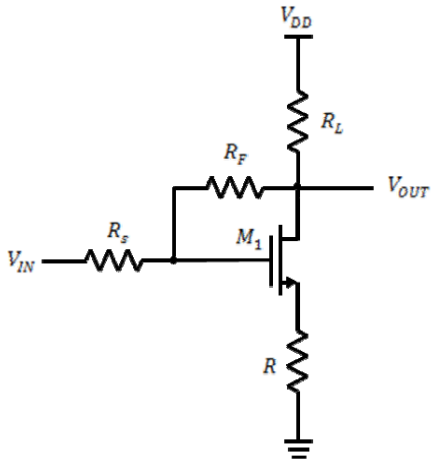

Fig -2: Shunt-series feedback amplifier

In a shunt-series feedback topology (Figure 2), before amplification the resistor R does not cause attenuation of signals. It is expected that the noise figure in shunt-series feedback amplifier is improve than that of a resistive termination amplifier. On the other hand, the resistor feedback network remains a source of thermal noise. Consequently, the noise performance of this topology is still not optimum.

2.3 Common Gate:

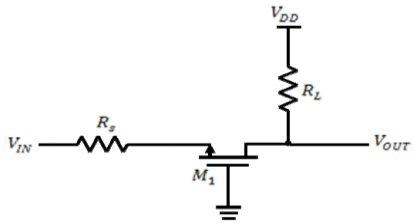

Fig -3: Common-gate amplifier

The common gate topology is another circuit implementing resistive input impedance (Figure 3). Characteristics of the common-gate topology are that the resistance looking into the source terminal equals ($1/ g_m$).

2.4 Source degeneration:

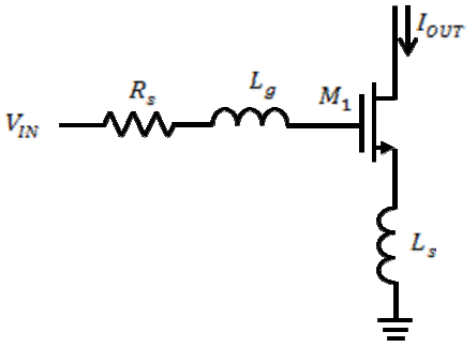

Fig -4: Narrowband LNA with inductive source degeneration

The above mention topologies do not have good noise performance due to presence of noisy resistance along the signal path. The noise performance of amplifiers can be improved, if resistive input impedance can be provided without using an actual resistor.

An inductive source degeneration topology (Figure 4) is commonly used to create resistive input impedance without the noise of real resistors. This topology provides resistive input impedance at the resonant frequency without the thermal noise of an ordinary resistor and degrading the noise performance of the amplifier.

3. RECENT RESEARCH

Table -1: Comparison of different LNA

Parameters	Data Set 1	Data Set 1	Data Set 1	Data Set 1	Data Set 1	Data Set 1	Future Work
Year of	2011	2012	2012	2012	2013	2014	2015
Operating	2.4 GHz	3.2~ 9.7	2.4-2.43 GHz	2.4 to 11.2 GHz	2.4 GHz	2.4 GHz	2.47 GHz
Supply	1V	1V	1.2V	1.5 V	1.2 V	1.2 V	1.2V
Technology	130 nm	0.18 nm	130 nm	180 nm	130 nm	130 nm	90 nm
Gain	25.2 dB	14.9 db	20 dB	14.8 dB	23.9 dB,	24.3 dB	14.0 dB

S11	-14 dB	-10~ - 39.5 dB	-10 dB	-10 dB	-26.9 dB	–20 dB	-10 dB
Noise Figure	3.8 dB	6 dB	3.2 dB	3.9 dB	5.6 dB	3.5 dB,	0.5 dB

Table 1 is a summary of implemented CMOS LNA from 2011-2014. This data set compares design of various LNA. Data set 2 shows that with 130 nm technology and 1V supply voltage 3.8 dB noise figure is achieved. While with 180 nm technology and 1.2 V supply voltage 3.2 noise figures is achieved. From all the data set we observe that minimum achieved noise figure is 3.2 db with 130 nm. In future 0.5 db noise figure will be achieved with 90 nm.

Inductive source degeneration cascade topology is chosen because it produces better gain and a cascade topology is chosen to provide low noise figure.

4. OBJETIVE OF PROPOSED DESIGN

The major parameters of RF circuits are linearity and noise figure. While designing of LNA it is very difficult to attain low noise figure and low power consumption. If we use 90 nm technologies we can improve noise figure at 2.47 GHz. Since minimum noise figure till date is 3.2 dB, we can target the noise figure of LNA to be less than 3.2 dB with 90 nm CMOS technology and biasing voltage is 1.2 V. Agilent's Advance Design System (ADS) 2009 is used to simulate LNA design

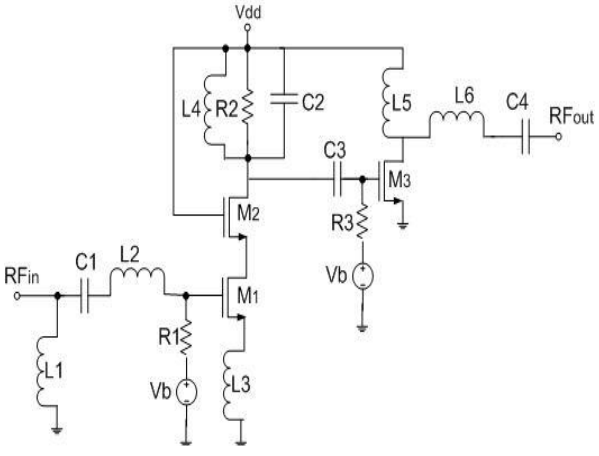

Fig -5: Schematic of LNA

Table -2

Parameters	Targeted specifications
Operating	2.47GHz
Supply	1.2V
Technology	90 nm
Gain	14.0dB
S11	-10 dB
Noise Figure	0.5 dB

3. CONCLUSIONS

This paper gives analytical study of different LNA operating at different frequency. This paper shows that an efficient LNA with noise figure less than 3.2dB and supply voltage less than 1.2 V can be designed using 0.18um CMOS technology. The improvement of this LNA is still going on to achieve the desired results, we will modified the circuit as shown in fig. 1 and try to reduce its noise value as low as possible and gain as high as possible with 90 nm technology.

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