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OPTIMIZED MODEM DESIGN FOR SDR APPLICATIONS

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Abstract-*This paper presents the methods to design optimized QPSK modulator and demodulator which consumes less time, power and gives better throughput using Spartan-3 and Sparatn-6 FPGA boards and Xilinx 14.7 software. The whole system is divided into several small modules based on top-down design method, and Verilog hardware description language is used to design each module. Here two different approaches are used to design QPSK modulator and are compared with conventional QPSK modulator which is designed using arithmetic multipliers and adders. In proposed method-1 the modulator is designed by using Vedic multiplier and carry look ahead adder and demodulator is designed using FIR Low Pass Filter.FIR low Pass filter coefficients are generated in MATLAB using rectangular window and hamming window. In proposed method-2 QPSK modulator is designed using multiplexers. The QPSK module is implemented on Spartan-3 and Spartan-6(Atlys) FPGA board. The whole system has been simulated in Xilinx 14.7 and successfully downloaded on to the chip xc3s400-4pq208 and XC6SLX45 - CSG324. The results show that the proposed methods can greatly improve the speed and reduce the latency and gives better frequency of operation. Frequency of operation is improved drastically when Spartan-6 (Atlys) board is used compared to Spartan-3 board.*

Key Words: SDR, QPSK, FPGA, CLA, VM, HDL.

1. INTRODUCTION:

The advancements in wireless communication technology using various digital modulation techniques to transmit data with extreme low power have led us to use the concept of software defined radio. The process, where more and more hardware components are replaced with software, has resulted in coining the term Software-Defined Radio (SDR) - because if the components can be replaced with software, then indeed the very functionality of these components can be redefined by this software. By simply downloading a new program, a software radio is able to interoperate with different wireless protocols, incorporate new services, and upgrade to new standards. Present software-defined radios (SDR) employ front end circuits that contain multiple receivers and transmitters for each band of interest, which is inflexible, expensive and power inefficient. A programmable front end circuit is implemented on a CMOS device and is configurable to transmit and receive signals in a wide band of frequencies, thereby providing an adaptable transmitter and receiver operable with current and future wireless networking technologies.

In this paper, the FPGA implementation of QPSK modulator using two different methods, i.e., proposed method-1 and proposed method-2[1] and comparison with the conventional QPSK modulator method is done and also demodulator design for proposed method-1 is presented. Complete modulator and demodulator units are modeled using Verilog and functionality is verified using ISim simulation tool. The code is synthesized fully onto Xilinx FPGAs.

2. CONVENTIONAL QPSK MODULATOR

In this method the input 16 bit stream is divided into even and odd components of 8-bits each. These even and odd components are multiplied with cosine and sine waves respectively using normal arithmetic multiplier and finally these In phase and Quadrature phase components are added using normal arithmetic adder.

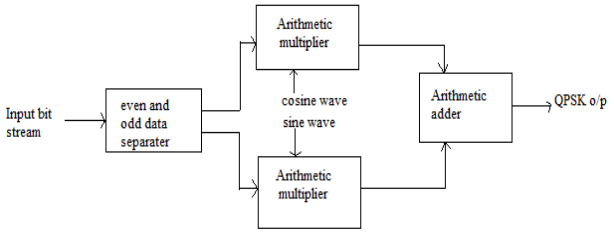


Fig- 1: Conventional QPSK modulator.

3. PROPOSED METHOD-1 QPSK MODULATOR:

Proposed Method - 1 of QPSK modulator is designed by using Vedic multiplier and CLA. The input bit stream is divided into even and odd bits and multiplied by cosine and sine wave respectively using Vedic multiplier instead of arithmetic multiplier and later adding the in phase and

quadrature phase component using carry look-ahead adder instead of arithmetic adder.

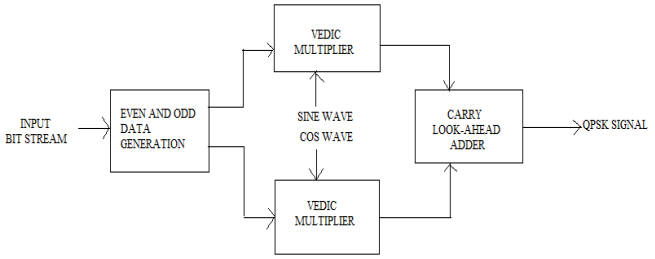


Fig- 2: Proposed Method-1 QPSK Modulator

3.1 Carry Look-Ahead Adder Design:

In ripple carry adders, the carry propagation time is the major speed limiting factor.CLA reduces the carry propagation delay while performing addition by calculating the carry signals in advance, based on the input signals. It is based on the fact that a carry signal will be generated in two cases:
(1) When both bits A(i) and B(i) are 1.
(2) When one of the two bits is 1 and the carry-in (carry of the previous stage) is 1.
The fig-3 shows the full adder circuit used to add the operand bits in the ith column; namely A(i) & B(i) and the carry bit coming from the previous column C(i).

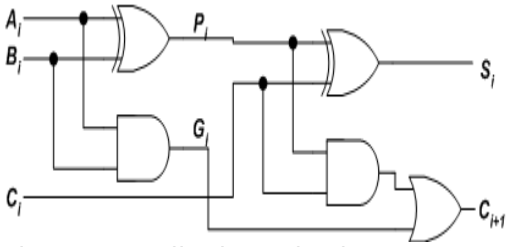


Fig- 3: Generalized CLA circuit.

In the above figure 3, the 2 internal signals P(i) and G(i) are given by:
P(i) = A(i)⊕B(i) (1)
G(i) = A(i)*B(i) (2)
The output sum and carry are given as:
S(i) = P(i)⊕C(i) (3)
C(i+1) = G(i)+P(i)*C(i) (4)
G(i) is known as the *carry Generate* signal since a carry C(i+1) is generated whenever Gi =1, regardless of the input carry C(i).
P(i) is known as the *carry propagate* signal since whenever P(i) =1, the input carry is propagated to the output carry, i.e., C(i+1) = C(i)(Note that whenever P(i) =1, G(i) =0).
Computing the values of P(i) and G(i) only depend on the input operand bits A(i) & B(i) as clear from the fig-3 and equations 1 to 4.

3.2 Vedic Multiplier Design:

The use of Vedic mathematics lies in the fact that it reduces the typical calculations in conventional mathematics to very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Vedic Mathematics is a methodology of arithmetic rules that allow multiplication in an efficient way. Multiplication methods are extensively discussed in Vedic mathematics. Various tricks and short cuts are suggested by VM to optimize the process. These methods are based on concept of

a) Multiplication using deficits and excess.
b) Changing the base to simplify the operation.
Various methods of multiplication proposed in VM
- UrdhvaTiryakbhyam - vertically and crosswise
- Nikhilam Navatashcharamam Dashatah: All from nine and last from ten.

The hardware architecture of 2X2, 4x4 and 8x8 bit Vedic multiplier module are displayed in the below sections. Here, "Urdhva-Tiryakbhyam" (Vertically and Crosswise) sutra is used to propose such architecture for the multiplication of two binary numbers. The beauty of Vedic multiplier is that here partial product generation and additions are done concurrently. Hence, it is well adapted to parallel processing. The feature makes it more attractive for binary multiplications. This in turn reduces delay, which is the primary motivation behind this work.

3.2.1 2x2 Vedic Multiplier:

The method is explained below for two, 2 bit numbers A and B where A = a1 a0 and B = b1 b0 as shown in Fig-4.[2][3]Firstly, the least significant bits are multiplied which gives the least significant bit of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The sum is the third corresponding bit and carry becomes the fourth bit of the final product.

s0 = a0b0 (5)
c1s1 = a1b0 + a0b1 (6)
c2s2 = c1 + a1b1 (7)

The final result will be *c2s2s1s0*. This multiplication method is applicable for all the cases.

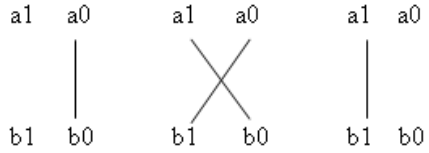


Fig- 4: Vedic Multiplication Method for two 2-bit Binary Numbers

3.2.2 4x4 Vedic Multiplier:

The 4x4 bit Vedic multiplier module is implemented using four 2x2 bit Vedic multiplier modules as discussed in Fig-5. Let's analyze 4x4 multiplications, say A= A3 A2 A1 A0 and B= B3 B2 B1 B0. The output line for the multiplication result is – S7 S6 S5 S4 S3 S2 S1 S0 .Let's divide A and B into two parts, say A3 A2 & A1 A0 for A and B3 B2 & B1 B0 for B. Using the fundamentals of Vedic multiplication, taking two bit at a time and using 2 bit multiplier block, we can have the following structure for multiplication as shown in Fig-5.

Equations of 4x4 Bit Vedic Multiplier

A=a3 a2 a1 a0.
B=b3 b2 b1 b0.
S0=a0.b0.
S1=a1.a0+a0.b1.
S2=a2.bo+a1.b1+a0.b2+ S1(1).
S3=a3.b0+a2.b1+a1.b2+a0.b3+ S2(2 to 1).
S4=a3.b1+a2.b2+a1.b3+ S3(2 to 1).
S5=a3.b2+a2.b3+ S4(2 to 1).
S6=a3.b3+ S5(2 to 1).
Product=S6 & S5(0) & S4(0) & S3 & S2 & S(1) & S(0).
& - Concatenate

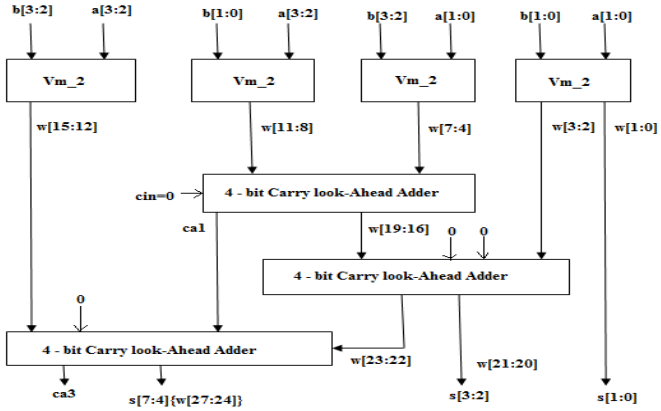


Fig-5: 4 Bit Vedic Multiplier

Similarly using 4-bit Vedic multiplier 8-bit Vedic multiplier can be designed and using 8-bit Vedic multiplier 16-bit Vedic multiplier can be designed and so on as shown in the fig-6 and fig-7 below.

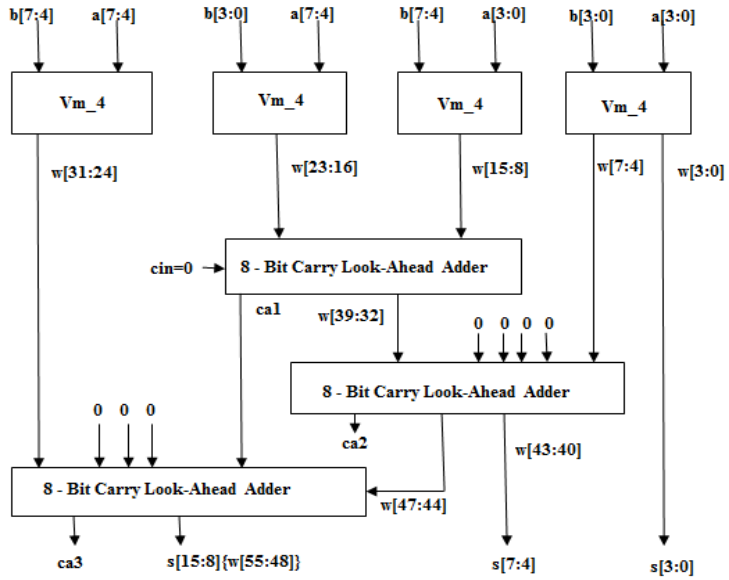


Fig-6:8 Bit Vedic Multiplier

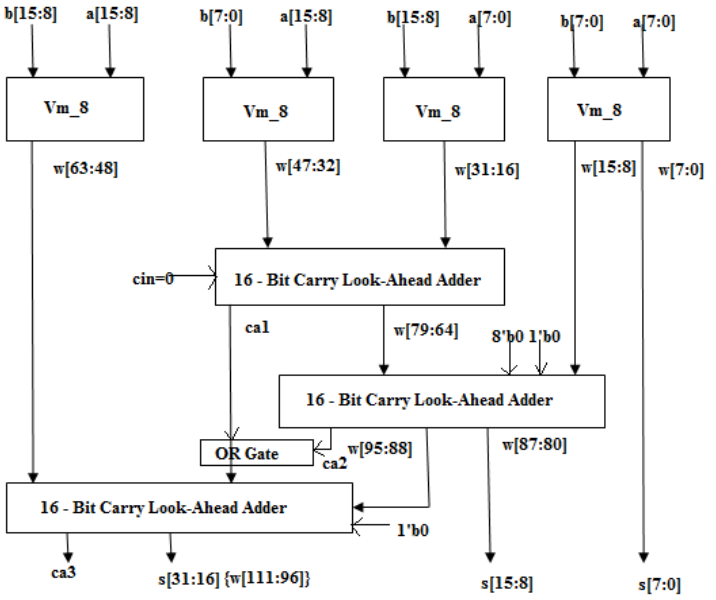


Fig- 7:16 Bit Vedic Multiplier

4. PROPOSED METHOD-1 QPSK DEMODULATOR:

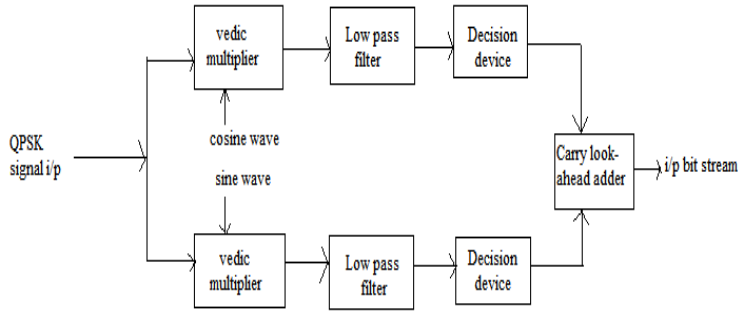


Fig- 8: QPSK Demodulator for Proposed method-1

The previously designed Vedic multiplier and CLA blocks as described previously are used in designing the QPSK demodulator module along with FIR (Finite impulse response) Low pass filter.

5. PROPOSED METHOD-2 QPSK MODULATION

In this modulation technique the input sixteen bit data bit stream is divided into two bits at a time. These two bits 00,10,01,11 act as the select lines for the multiplexer which selects sine with 0 degree, sine with 90 degree, sine with 180 degree and sine with 270 degree phase shifts respectively. Then all these are concatenated to get the final QPSK wave.

Below fig-9 shows implementation of QPSK modulator using multiplexer concept.

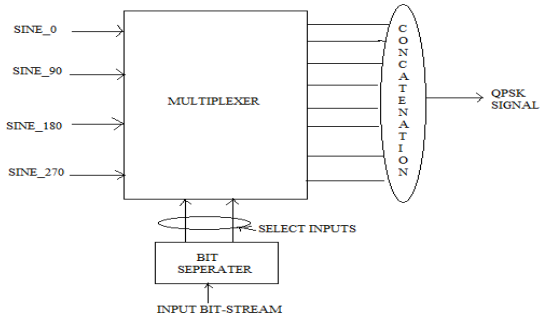


Fig-9: Proposed method -2 QPSK modulator

6. SIMULATION RESULTS:

This represents the output of carry look-ahead adder where, a and b are the inputs which are 8-bit wide and cin is the carry input which should be zero for addition operation. s, p and g are the sum, carry generate and carry propagate respectively each of 8- bit width. cout is the output carry of one bit.

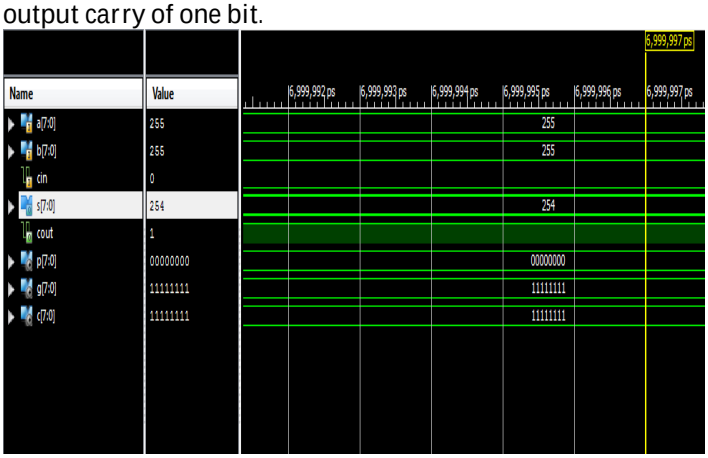


Fig- 10: Carry look-ahead adder results

Here a and b represents the inputs to the Vedic multiplier each of 16 bits width and output of Vedic multiplier is out which is of 32 bits, and ca1,ca2,ca3 represents the intermediate carry outputs from the carry look ahead adders used in the design.

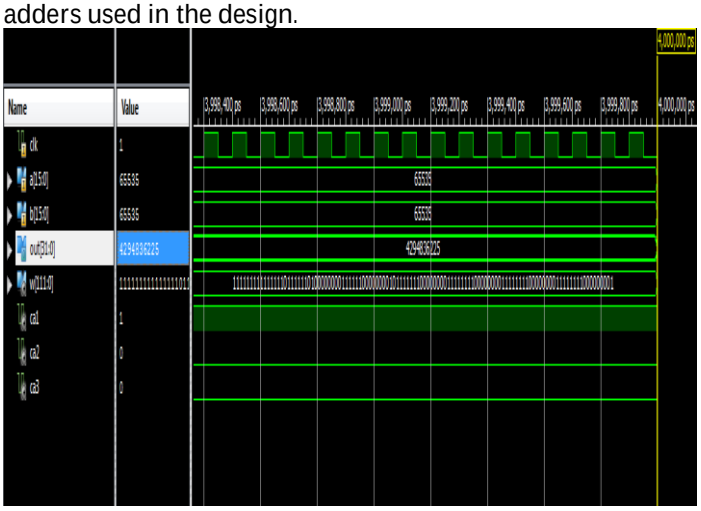


Fig-11: 16 bit Vedic multiplier result

This represents sine and cosine waveforms generated in Modelsim 6.1 version

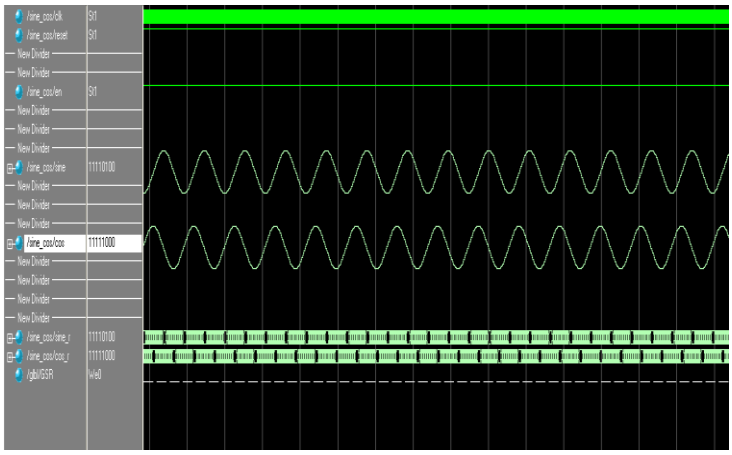


Fig-12: Sine and cosine wave generation in Modelsim

This represents the final QPSK output in digital format generated using ISim inbuilt simulator present in Xilinx 14.7 version. final_out is the QPSK output and clk, rst, en and data_in are the inputs.

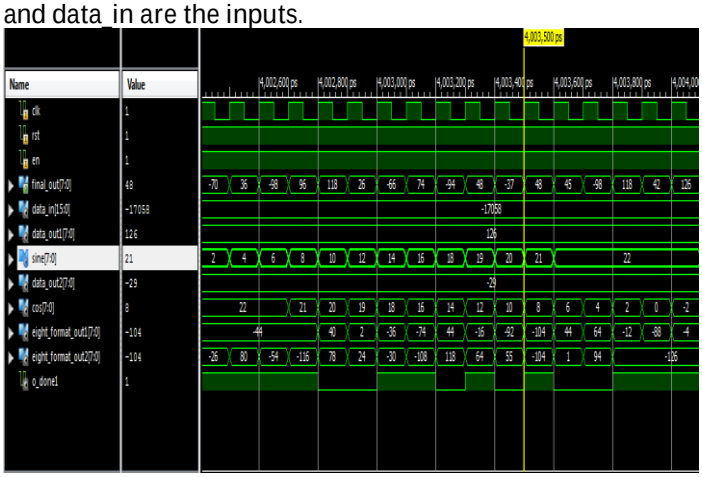


Fig-13: QPSK modulation for proposed method-1 in ISim simulator.

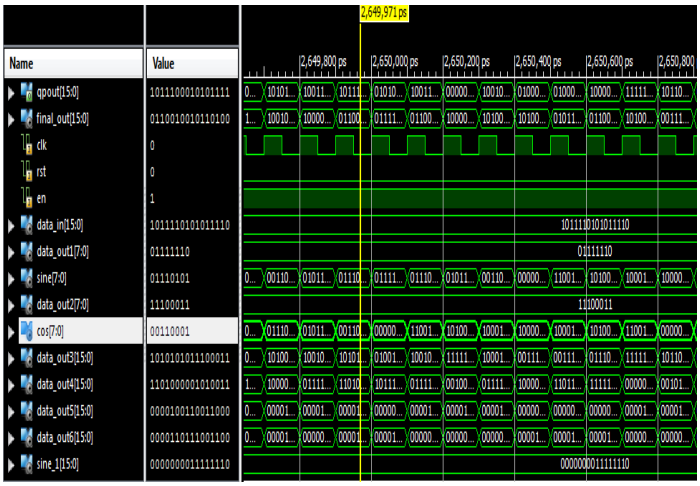


Fig- 14: QPSK demodulation for proposed method-1 in ISim simulator.

This represents the QPSK output generated by proposed method-2 using multiplexer concept.

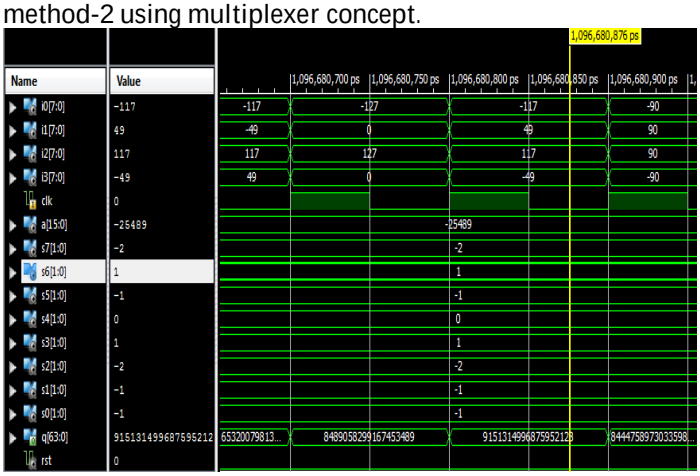


Fig- 15: QPSK modulation for proposed method-2 in ISim simulator.

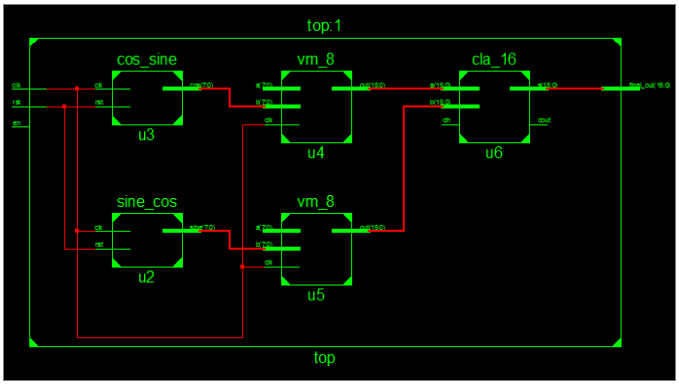
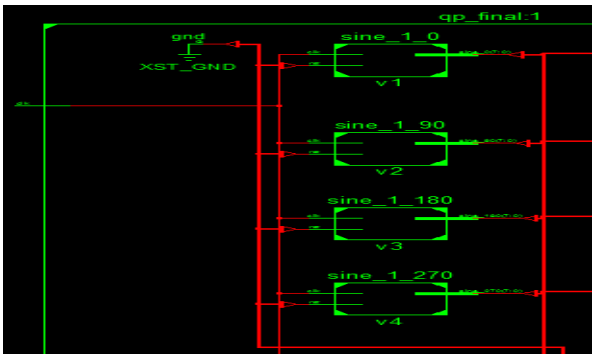
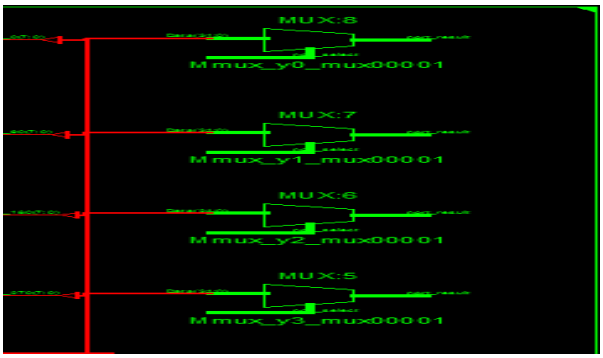


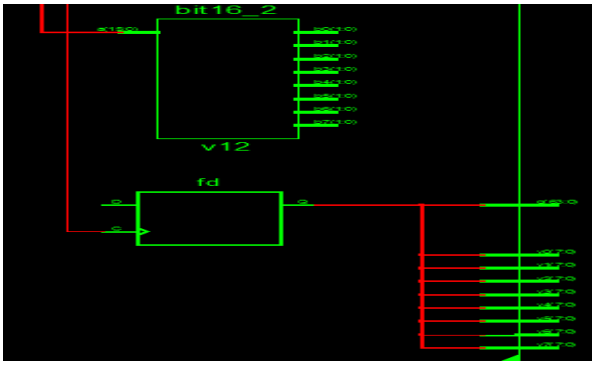
Fig- 16: RTL schematic for proposed method-1



(a)



(b)



(c)

Fig-17: RTL schematic for proposed method-2

6.1 FIR Low Pass Filter output designed using Hamming and Rectangular window in MATLAB.

The below Fig-18 represents the magnitude and phase response of Low Pass Filter designed using hamming windowing technique. Here, the cutoff frequency of the filter is 800 Hz approx.

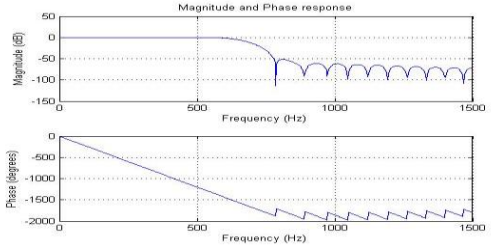


Fig-18: FIR Low pass filter output using Hamming window

Table -1: Filter Coefficients generated using Hamming window

0.0010	0.0011	-0.0008	-0.0024	0.0002	0.0045	0.0021	-0.0069	-0.0072
0.0079	0.0156	-0.0048	-0.0271	-0.0059	-0.0399	0.0298	-0.0519	-0.0831
0.0603	0.3097	0.4357	0.3097	0.0603	-0.0831	-0.0519	0.0298	-0.0399
-0.0059	-0.0271	-0.0048	0.0156	0.0079	-0.0072	-0.0069	0.0021	0.0045
0.0002	-0.0024	-0.0008	0.0011	0.0010				

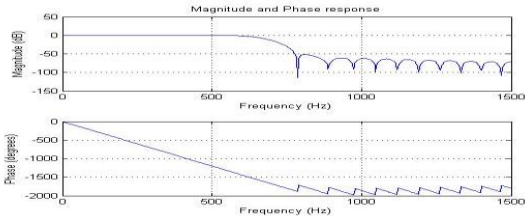


Fig-19: FIR Low Pass Filter output using rectangular window

Table-2: Filter Coefficients generated using rectangular window

0.008	0.0011	-0.0002	-0.0018	-0.0015	0.0017	0.0042	0.0012	-0.0058	-0.0073	0.0023	0.013
0.0085	-0.0122	-0.0236	-0.0032	0.0323	0.0345	-0.0182	-0.0740	-0.0428	0.1074	0.2939	0.378
0.2939	0.1074	-0.0428	-0.0740	-0.0182	0.0345	0.0323	-0.0032	-0.0032	-0.0236	-0.0122	0.0085
0.013	0.0023	-0.0073	-0.0058	0.0012	0.0042	0.0017	-0.0015	-0.0018	-0.0002	0.0011	0.008

6.2 Hardware Implementation of the Project

The designed QPSK modulator using Vedic multiplier and carry look-ahead adder is implemented on Spartan3 FPGA kit and the simulated digital output of QPSK is converted to analog waveform by connecting C4 to C21 which converts digital format into analog waveform and this analog output is seen in CRO as shown in the fig-20.

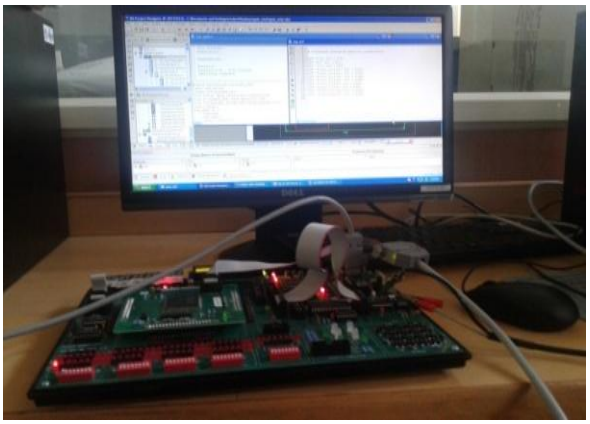


Fig-20: FPGA implementation of QPSK modulator proposed method-1

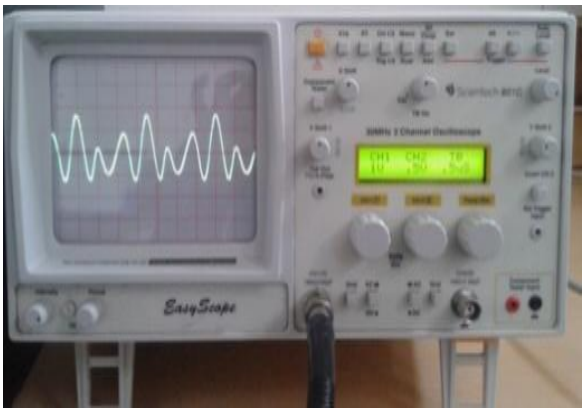


Fig- 21: Output of QPSK proposed method-1 on CRO

The QPSK modulation technique using multiplexer concept is implemented on Spartan3 FPGA board and the analog output waveform is observed in CRO.

Fig-22: FPGA Implementation of proposed method -2

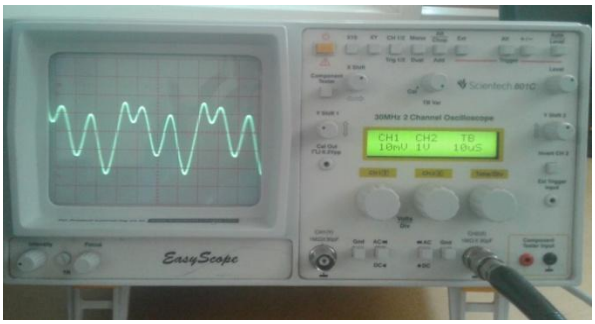


Fig-23: Output of proposed method-2 on CRO

Table-3:Comparison of three modulation techniques in terms of frequency on Spartan-3 FPGA board.

Method	Maximum frequency of operation
Conventional QPSK method	146.803 MHZ
Proposed method-1	252.277 MHZ
Proposed method -2	343.389 MHZ

Table-4: Comparison of three modulation techniques in terms of Frequency on Spartan-6(Atlys) FPGA board.

Method	Maximum frequency of operation
Conventional QPSK method	291.911 MHZ
Proposed method-1	438.779 MHZ
Proposed method -2	446.100 MHZ

7. CONCLUSIONS

With the proposed methods 1 and 2 compared to conventional modulator design (using arithmetic adder and multiplier respectively) there is a great improvement in the throughput. In proposed method QPSK modulator-1 Multiplier and LUT's are used for carrier generation and arithmetic multiplier, arithmetic adder is replaced by Vedic multiplier and carry look-ahead adder respectively. In second method multiplexer concept is used to design QPSK modulator. All these methods are successfully simulated on Xilinx ISE 14.7 software and implemented in FPGA Spartan-3 board as well as Spartan 6 kit. The power consumption, timing and area utilization achieved in the proposed method QPSK modulator-2 also gives a high throughput as shown in Table 3&4.

The FIR LPF for proposed method-1 QPSK demodulator is designed by using Hamming and rectangular windowing technique in MATLAB, and demodulation results are obtained and the whole module is implemented on Spartan-3 XC3S400 and Spartan-6(ATLYS) FPGA hardware.

The designed QPSK modem using proposed method-1 and proposed method-2 gives better performance over conventional QPSK method and also these designed QPSK modem gives better results when implemented on Spartan-6(ATLYS) FPGA board compared to Spartan-3 FPGA kit.

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BIOGRAPHIES

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