International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 02 Issue: 03 | June-2015 www.irjet.net p-ISSN: 2395-0072

A Review on the Progress of Non-Volatile Memory Device Based on Electric-Pulse Induced Phase Transition

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Abstract - *This paper presents a review on the progress of solid-state non-volatile memory device based on electric-pulse induced phase transition. This two-terminal memory device exploit the unique behaviour of chalcogenide semiconductors. The crystalline and amorphous states of chalcogenide glass have very different electrical resistivity. The amorphous, high resistance state represents a binary 0, while the crystalline, low resistance state represents a binary 1. The reversible phase transition between low-conductive amorphous state and high-conductive crystalline state is performed using electric pulses. Phase change memory technology has made rapid progress in a short period of time in terms of memory-cell size, data retention capacity, programming currents and endurance characteristics. The mechanisms responsible for the data loss and degradation of the memory has been discussed.*

Key Words: Non-volatile memory device, chalcogenide semiconductor, Phase transition, Electric pulses, memory degradation

1. INTRODUCTION

Tellurium-based amorphous semiconductors exhibit the characteristics of high speed switching between amorphous state and crystalline state [1]. The memory based on reversible phase transition is known as phase change memory (PCM). It is well known that an amorphous solid exhibits a glass transition usually followed by a crystallization on heating [2]. However, the heating rate is one of the important factors which controls the glass transition and crystallization temperatures of an amorphous solid.

Until recently, a number of studies [3]-[10] have been performed to develop PCM for commercial applications. Many leading electronics and semiconductor companies, such as, Intel, IBM, Phillips, Sony, and ST Microelectronics, Samsung Electronics, have been pursuing research to develop high density PCM chips based on electric-pulse induced phase transition [5]. However, material quality and power consumption issues prevented commercialization of the technology. The crystalline and amorphous states of chalcogenide glass have different electrical resistivity. The amorphous, high resistance state represents a binary 0, while the crystalline, low resistance state represents a binary1 [3].

The PCM has been fabricated using a chalcogenide alloy of germanium, antimony and tellurium (GeSbTe) called GST [3], [6]. The stoichiometry or Ge:Sb:Te element ratio is 2:2:5. When GST is heated to a high temperature, its chalcogenide crystallinity is lost. Once cooled, it is frozen into an amorphous glass-like state and its electrical resistance is high. By heating the chalcogenide to a temperature above its crystallization point, but below the melting point, it will transform into a crystalline state with a much lower resistance. The time to complete this phase transition is temperature-dependent. Cooler portions of the chalcogenide take longer to crystallize, and overheated portions may be remelted. The crystallization time is longer than the conventional volatile memory devices like modern DRAM, which have a switching time on the order of two nanoseconds. However, a January 2006 Samsung Electronics patent application indicates PCM may achieve switching times as fast as five nanoseconds.

A more recent studies by Intel and ST Microelectronics show that the chalcogenide material can be switched carefully into four distinct states by applying electric pulse; the amorphous or crystalline states, along with two new partially crystalline states. Each of these states has different electrical resistivity that can be measured using read pulse without any change in electrical properties. Thus, a single memory cell can represent two extra bits, doubling memory density. Many renowned electronics and semiconductor companies have developed PCM chips for commercial applications. In February 2011, Samsung presented 58 nm 1.8V 1Gb PCM chip and in February 2012, this company also fabricated 20 nm 1.8V 8Gb PCM. In July 2012, Micron announced availability of Phase-Change Memory for mobile devices. In May 2014, IBM demonstrated combining PCM, conventional NAND, and DRAM on a single controller.

In this paper, a review on the progress of solid-state non-volatile memory device based on electric-pulse induced phase transition has been presented.

2.FABRICATION OF MEMORY DEVICE

A schematic cross-sectional diagram of a simple memory device based on phase transition is shown in Fig. 1. The memory device consists of semiconductor thin film, a lower electrode and a upper electrode. First. a nickel film was deposited on the glass substrate for the lower electrode. For insulation, the nickel electrode was coated with polymide film by using spin-coating technique. About ten micrometer opening in the polymide film was defined by photolithography process. Then, a thin film of 300 nm thickness was deposited on this structure by thermal-evaporation technique at a rate of l5 nm/s from semiconductor powder of $Ge_2Sb_2Te_5$ (GST). A thin film of antimony was subsequently deposited on the thin film for ohmic contact , and aluminum film was finally deposited on the antimony film to reduce the resistance of the electrode. Thus, the upper electrode consisted of antimony and aluminum double layers. The thichness of the polymide which separated the upper electrode from the lower electrode was more than one micrometer.

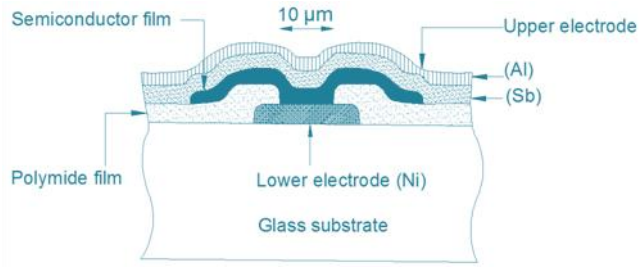

Fig. 1 Schematic cross-sectional diagram of a typical memory device

In the next technology generations, the most serious consideration for PCM is the large current needed to switch from crystalline state to amorphous state [11]-[14]. The operation of the PCM cell relies on Joule heating, so the memory cell structure and operating conditions are dictated by the electro-thermal diffusion equation. Recently, a typical PCM cell is designed so that the only current path through the device passes through a very small aperture. In the SET operation, an electrical pulse of longer duration is applied to heat a significant portion of the cell above the crystallization temperature of the phase change material as shown in Fig. 2. This SET operation indicates the write speed performance of PCM technology, since the required duration of this pulse depends on the crystallization speed of the phase change material. SET pulses shorter than 10 ns have been demonstrated [11].

In the RESET operation, a larger electrical current of short duration is applied in order to melt the central portion of the cell. The molten material quenches into the amorphous phase, producing a cell in the high-resistance state. The read operation is performed by measuring the device resistance at low voltage, so that the device state is not perturbed as shown in Fig. 2.
If this RESET current is low enough, then a minimum-size access device can provide enough power to switch the memory cell from the SET state to the RESET state.

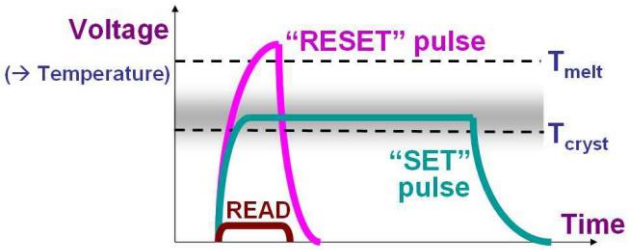

Fig. 2 Programming of a PCM device involves application of electrical pulses [4].

In order to fabricate a PCM cell that will work even with these small currents, an innovative integration scheme is needed which creates a highly sub-lithographic yet controllable feature size. Scaling implies not only a shrink in physical dimensions of the memory cell, but also an increase in the number of memory cells per chip. Lastly, to maximize the number of bits per cell, a cell structure which allows multi-bit functionality is highly desirable.

3.MEMORY PERFORMANCE AND DEGRADATION

The number of write (SET) and erase (RESET) cycles [6] induced by electric field has long been one of the strengths of PCM, especially in comparison to established Flash technologies, where the number of write and erase cycles is around to 10^4-10^5 . The demonstration of 10^{12} SET-RESET cycles [3, 11] in PCM devices without any significant degradation of resistance was almost certainly a significant factor in the surge of interest in PCM technology that followed. It is found that a single memory device could be operated reliably for so many cycles. But the more critical question is what happens to the worst-case device in a large array. Subsequent large-scale PCM integration experiments have tended to show endurance numbers in the range of 10^8-10^{10} cycles[6, 15, 16] still easily exceeding the endurance of Flash memory. The data can be stored for 10 years at 110^o C and a resistance difference of two order of magnitude can be maintained between crystalline and amorphous states [6].

Several different failure modes have been observed to occur after SET-RESET cycling [6, 15, 16]. One of the memory failures may be due to physical separation [6] of the chalcogenide alloy from the electrode. The main responsible of instabilities and open-mode failure has been recognized in an unsatisfactory quality of the electrode-GST interface, confirming that the PCM process integration plays a major role for the device endurance capabilities.

A second failure mode has been also observed, usually called short-mode failure [6], where the devices are permanently stuck [11] in the highly conductive state. This phenomenon can be hardly ascribed to the interface quality, thus requiring an auxiliary physical mechanism that forbids the phase change transition of the GST or creates conductive parallel paths that shunt the cell electrodes. In both cases, a chemical modification of the chalcogenide alloy is required, suggesting as the mechanism responsible for failure the interdiffusion of chemical species from adjacent materials. In this case, a careful definition of the materials belonging to the device active region is mandatory to achieve good reliability performance.

In the RESET operation, the memory cell needs high programming current density. So another mechanism that could impact the device endurance is electromigration [14]. Actually, intrinsic electromigration-induced reliability issues for the GST compound are not expected to be a concern below 10^{12} programming cycles. Finally, current density, as well as the high temperatures reached in the active region during programming must be considered as accelerating factors for failure mechanisms of PCM.

4. CHALLENGES FOR THE TECHNOLOGY

The greatest challenge for phase-change memory has been the requirement of high programming current density , as such as, $>10^7$ A/cm², compared to 10^5-10^6 A/cm² for a typical transistor [3], [6]. The contact between the hot phase-change region and the adjacent dielectric is another fundamental concern. The dielectric may begin to leak current at higher temperature, or may lose adhesion when expanding at a different rate from the phase-change material. Phase change memory has high write latency and energy, which present challenge in its use, although recently, many techniques have been proposed to address this issue. It is assumed that phase transition occurs primarily from the fact that phase-change is a thermally driven process rather than an electronic process. Thermal conditions that allow for fast crystallization should not be too similar to standby conditions, e.g. room temperature. Otherwise data retention cannot be sustained. With the proper activation energy for crystallization it is possible to have fast crystallization at programming conditions while having very slow crystallization at normal conditions. Another biggest challenge for phase change memory is probably its long-term resistance and threshold voltage drift. The resistance of the amorphous state slowly increases according to a power law. This severely limits the ability for multilevel operation, e.g. a lower intermediate resistance state would be confused with a higher intermediate resistance state at a later time.

5. CONCLUSIONS

Electric-field induced phase change memory technology has made rapid progress in a short period of time in terms of memory-cell size, data retention capacity, programming currents and endurance characteristics. Phase change memory is fabricated using amorphous semiconductor thin film that can be changed rapidly between a crystalline phase having lower electrical resistance to an amorphous phase with much higher electrical resistance. Because no electrical power is required to maintain either phase of the material, so phase-change memory is non-volatile and it is much faster than the common flash memory. If the challenges for the phase change memory technology could be overcome, it is expected that in the future, PCM will emerge as a high-speed high-density memory device in place of flash memory.

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BIOGRAPHY

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