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Design of CMOS Galois field arithmetic logic unit using 120nm BSIM-4 model

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Abstract - *In ASIC and general purpose circuits arithmetic circuits play a very critical role. Multiple Valued Logic (MVL) provides the key benefit of a higher density per integrated circuit area compared to traditional two valued binary logic. Quaternary (Four-valued) logic also rendition the benefit of easy interfacing to binary logic because radix 4 allows for the use of simple encoding/decoding circuits. The functional completeness is verified with a set of fundamental quaternary cells. Quaternary (radix-4) dual operand encoding principles are applied to optimize power and performance of adder circuits using standard CMOS gates technologies. Gallois field plays role in communications including error improves the codes, cryptography, switching and digital signal processing. In these applications, area and speed requirements of an IC are necessary. Therefore an proficient hardware structure for such operations is desirable..*

Key Words: Quaternary logic, G.F(4) , standard CMOS technology.

1. INTRODUCTION

The remarkable increase in the density of Very Large Scale Integrated (VLSI) circuits is the result of advanced Integrated Circuits (IC) fabrication processes and the development of automated design tools. As the number of devices accommodated on VLSI chips increases, many problems also arise. For instance, the interconnection between devices inside and outside a chip becomes significantly complicated and the area occupied by interconnections increases in speed. Insistent interconnect scaling following Moore's law introduces many challenges in integration, feat and reliability. Inappropriate routing results in a larger chip size and cause timing and cross-talk problems. In deep submicron designs these problems are of outstanding importance.
The partial solutions to this problem in today's VLSI circuits are to use several metal layers, flip-chips and further methods. Although enhancement in metal stack material have enabled industry to reduce interconnect resistance in narrow lines and at the same time changes in interlayer dielectric (ILD) material have lowered the line to line capacitance resulting in Resistor-Capacitor (RC) delay improvement and thus interconnect power utilization, however, deep submicron technology introduces formidable integration and reliability challenges such as higher narrow Cu line resistivity, higher current density and inferior thermo-mechanical properties which must be overcome. It is well known that the binary number system is the leading choice for conventional voltage-mode design of digital systems. However, in a emblematic binary number system based VLSI circuit about 70 percent of chip area is occupied by interconnections which occupy a large portion of physical area even when it is not in use. Therefore the interconnections will be more efficient if several levels of logic are injected into a only wire, as in multiple valued logics. Dissimilar to binary logic, multiple valued logics require more than two discrete levels of logic signals and allow more than two logical concepts to exist in a logic system. Thus, the direct benefit of such logics is the improved overall information efficiency. It is because each r-valued signal can carry times more information than a binary signal does. As a result the routing area is compact on a logarithmic scale- -as r increases. As can be seen, the routing area of a 4-valued logic design is two times smaller than the corresponding binary logic system. 2 log r log r 2. The choice of the most favorable logic radix in term of implementation cost has been also studied by some researchers. the circuit implementation cost is decreasing with increasing logic radix and according to C.M. Allen and D. Given, the optimal radix is greater than Euler constant, . Since in practice the radix r is an integer, it comprehends that the more advantageous radix must be at least 3 or in other words ternary logic. On the other hand alteration with binary is most efficient if special radices are chosen in such a way that no information is lost or left unused.

1.2. RELATED WORK:

According to review paper [1] present a full adder prototype based on the designed LUT, fictitious in a standard 130-nm CMOS technology, able to work at 100 MHz while overriding 122 μW. The experimental results express the correct quaternary operation and confirm the power efficiency of

the proposed design. By using CMOS technology we can design Arithmetic and logical unit which is not presented in this paper. We can used DLC circuit for designing ALU.
According to review paper [2] Here they propose an arithmetic unit based on QSD number system based on quaternary system. The proposed design is developed with VHDL and implemented on FPGA device and results are compared with conventional arithmetic unit. Here we can used standard CMOS technology for designing Arithmetic and logical unit. The circuit is compatible with standard CMOS proceeding with a single voltage supply and employing only simple voltage mode structures. A clock supprost technique is used to optimize the switches resistance and power consumption. The proposed implementation overcomes several limitations found in previous quaternary implementations published so far, such as the need for special features in the CMOS process or power-hungry current-mode cells.
According to review paper [3] circuits The proposed approach yields very good results for the circuits studied in this paper, with almost optimal results for binary full adders up to 32 bits. For 64 bit,128 bit and more, This method is not cost efficient and more complexity.
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2. PROPOSED WORK:

One key metric to consider for any MVL circuits though is the interface logic to the traditional binary circuits. The edge to and from binary logic to the MVL logic does need to have the level conversion to allow successful integration. Circuits namely "radix converters" help to address the cross-region interface needs. The radix exchange is relatively easy for radices which are power of two. (example, radix-2 (binary), radix-4 (quaternary) and radix-8, radix-16 etc.) The radix conversion process gets complex and more careful handling for other radices like radix-3, radix-5, radix-6, radix-7, radix-9 etc.

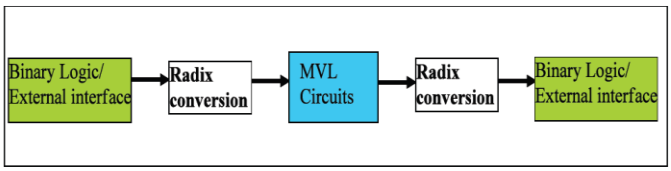

Fig. 1 Block diagram Of proposed design.

So, the area advantages can only be seen in larger circuits. The logic duplication due to binary logic spread is avoided in MVL circuits. Also higher radices would allow the increased number of functions that can be implemented, making it easier for large and more complex functions implementation. Another important advantage is the reduction of signal connections/wires. The reduced wires would condense the size of the chip and also improve the rout ability of the design. One of the critical challenges in the Deep Sub-Micron technologies is the routing congestion and also the printability (fabrication) of close proximity of the wires. The limitations of the existing fabrication equipment would create several manufacturing defects like shorting of the wires, open of the wires etc. compose lot of part defects and yield loss. So, reducing the number of wires would significantly improve the device manufacturability and area improvement.

3. DOWN LITERAL CIRCUIT (DLC) :

Down literal circuit (DLC) is one of the most useful circuit element in multi-valued logic. The DLC can divide the multi-valued signal into a binary state at an arbitrary threshold. It consisting of variable threshold voltage by way of controlling only two bias voltages.

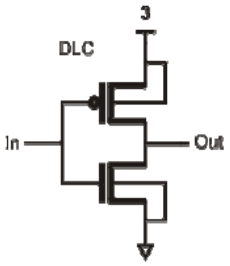

Fig 2: Circuit diagram for DLC

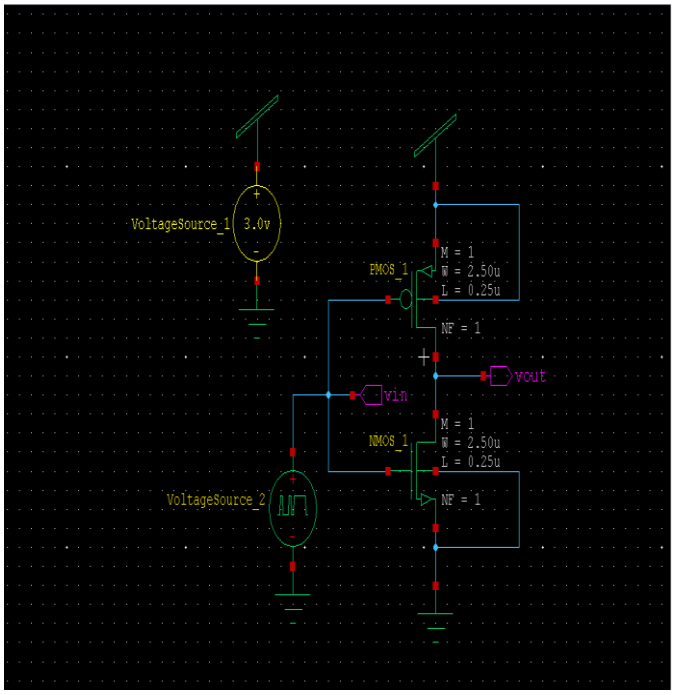

Fig 3: Circuit Diagram of DLC

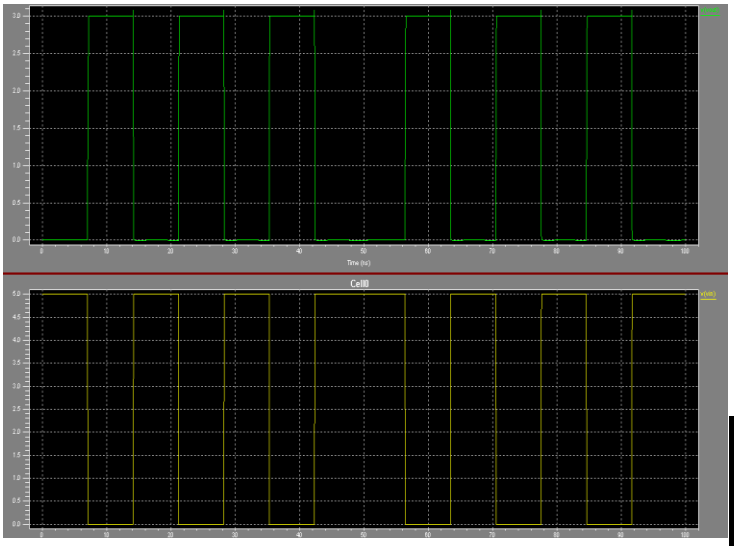

Fig.4: .Simulation Result of DLC circuit.

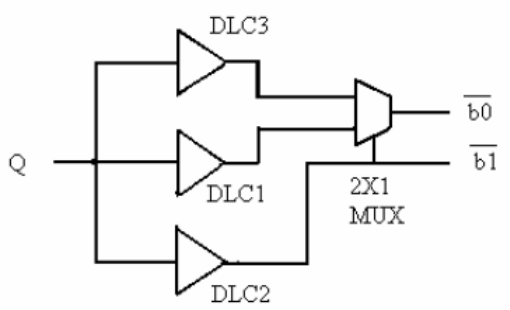

Figure 5: Quaternary to binary converter circuit

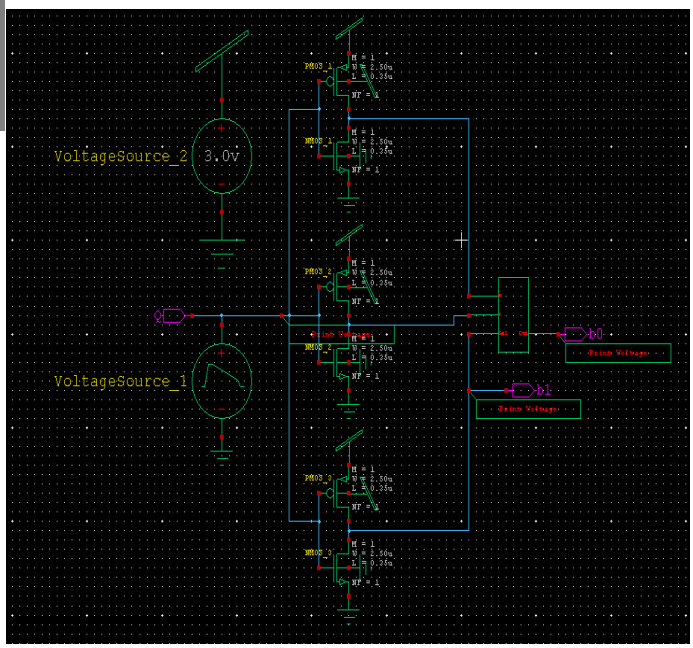

Fig.6: Schematic diagram of Quaternary to binary converter:

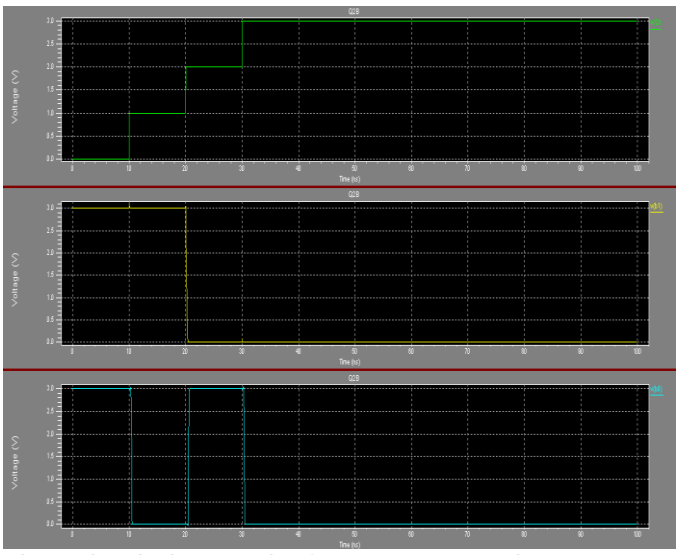

Fig.7: Simulation result of Quaternary to Binary converter.

3.1 DESIGN OF QUATERNARY CONVERTER CIRCUITS:

Objective of optimization is to minimize number of gates needed and also to minimize depth ofnet. Depth of net is the largest number of gates in any path from input to output. The reason forchoosing these two objectives is that they will give very good properties when implemented in VLSI. Minimizing number of gates will condense the chip area, and minimizing depth will give opportunity to use highest clock frequency .

3.1.1 Quaternary to binary converter:

A basic Quaternary to binary converter uses three down literal circuits DLC1, DLC2, DLC3 (each having diverse threshold voltage) and 2:1 multiplexer. Q is the quaternary input varying as 0, 1, 2 and 3 which is certain to three DLC circuits. The binary away puts thus obtained will be in complemented form and are required to pass through inverters to get actual binary numbers. Down literal circuits are realized from basic CMOS inverter by changing the threshold voltages of pmos and nmos transistors.

3.1.2 Binary to Quaternary converter :

Binary to quaternary converter circuit is shown in the circuit. LSB and MSB of a two bit binary number are given to DLC 1.

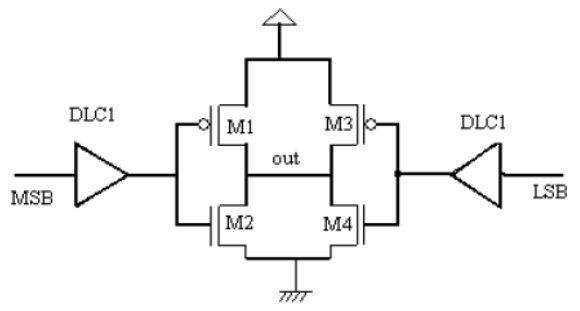

Fig 8: Binary to Quaternary converter circuit:

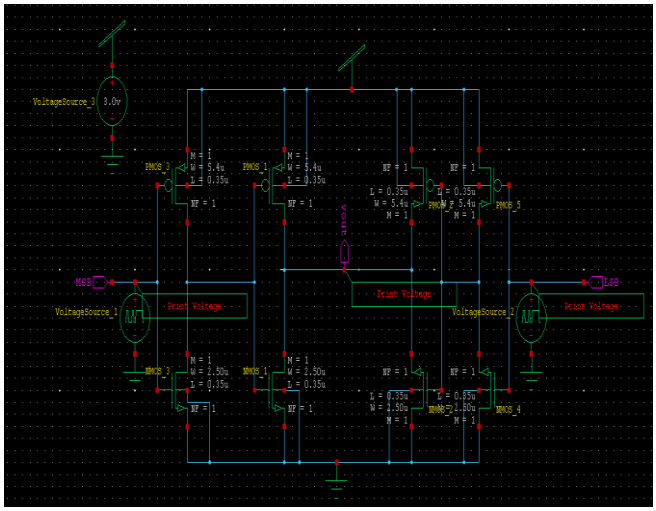

Fig.9: Schematic diagram of Binary to Quaternary :

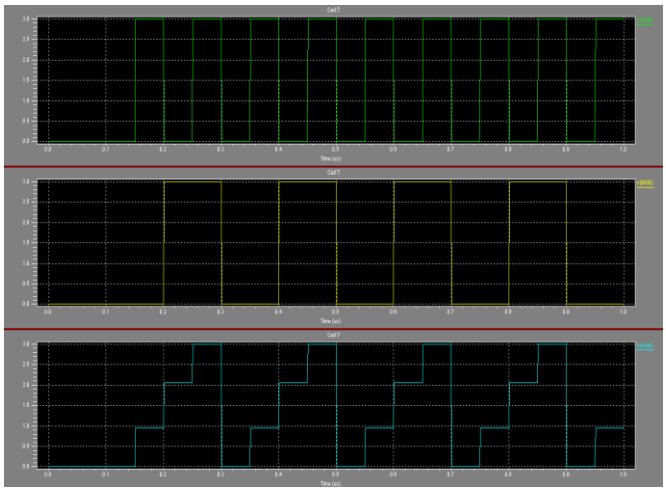

Fig.10: waveform of to Binary to Quaternary converter.

4. Galois Field addition :

Galois addition Galois addition table in Figure is used in Karnaugh diagrams to obtain minimum function. Minimal functions obtained from the minimal polynomials extracted from the Karnaugh diagrams for GF (4) addition is shown below. Let x1 x2 and y1 y2 be the binary representation of two quaternary numbers which have to be added. a 1 and a 2 are the two bit result of addition between x1 x2 and y1 y2 .

$a1 = (x1\ y1)$

$a2 = (x2\ y2)$

Above equation shows that addition in GF (4) requires only two gates and depth of net is reduced to one. This is a very good design among four circuits. Logical execution of the circuit is shown in figure.11

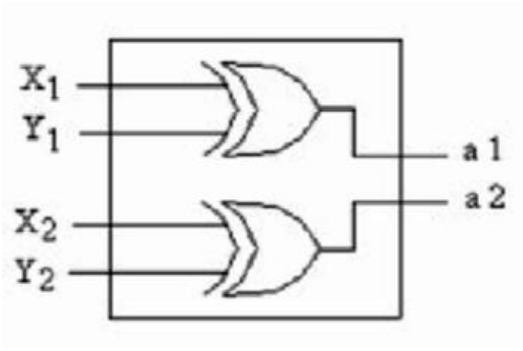

Fig 11: Galois field adder.

X1X2

+	0	1	2	3
0	0	1	2	3
1	1	0	3	2
2	2	3	0	1
3	3	2	1	0

Y1Y2

Fig 12: Table of Galois field adder.

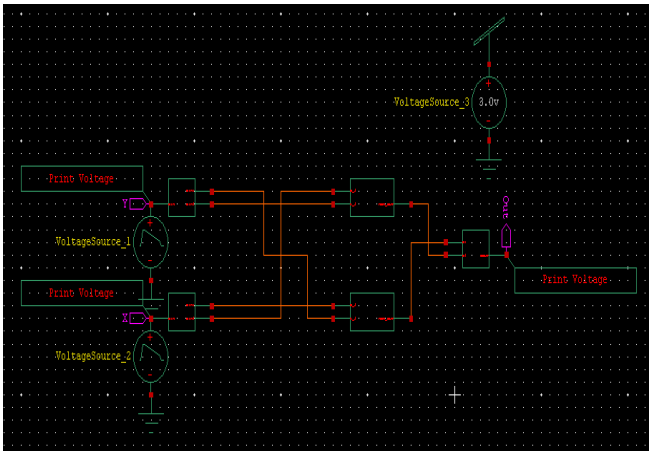

Fig 13: Shematic of Galois Field adder.

5.Conclusion:

The results illustrate that the binary to quaternary circuit is feasible and efficient in terms of designing while being implemented in a standard CMOS technology. As technologies are becoming more complex, multivalve logic (MVL) will be the future of circuit design. Since the research is still in preliminary stage on MVL the work is fundamental. If hardware implementation using MVL circuits is famous and more exposed to companies then one day MVL will surely turn over the binary logic. The advantages of lower power, higher performance, and reduced interconnect congestion motivate the use of quaternary circuits in a wide variety of applications.

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