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ADVANCED FAULT INJECTION TOOL FOR MEMORY UNIT

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Abstract -*Determination of fault tolerance of a digital system has very much importance because it will increase performance and accuracy. The fault injection method is used to find out the fault tolerance of a system. This method is valuable and attractive. In this paper fast FPGA based fault injector for memory unit is introduced. In previous FPGA based fault injection methods the response according to the fault injection is send to the observation system which is a personal computer. So in the case of large volume data there will be communication latency between this observation unit and FPGA. In this advanced tool all the modules in the fault injection environment is designed inside the FPGA itself. So there is no communication latency. This fault injector inject fault to the memory designed inside the FPGA, find out the architecture error and correct it. SPATAN 3E FPGA is used for this design. VHDL language is used for the FPGA design.*

Key Words: Fault injection, FPGA,VHDL.

1. INTRODUCTION

A system must valid in terms of functional behavioral and fault tolerance. Such a system can perform safety critical application. The fault injection can be performed by different methods. A fault emulation method is introduced in [1].this method use two speed-up laws for getting better performance. First law describes injection and emulation of independent faults at the same time and the second one describes injection of dependent faults using a single FPGA configuration. By these two laws the parallism increased and configuration time decreased but area overhead remains. In logic emulation method [2] for the sequential circuit a fault injection element is created which reduces the configuration time but area overhead remains. In instrumentation method [3], which consist of extra hardware parts for fault injection. The observability and controllability increased but hardware overhead and communication latency is high. A run time reconfiguration technique is explained in [4].this technique reconfigure the system during the execution of application .this method introduces high bandwidth interface between system and personal computer which act as the observation system. In [5] a FPGA based fault injection is introduced which support high controllability and observability and it have the capability of injecting permanent and transient fault. It is a high speed injector comparing to the conventional technique but it will exhibit high latency. This paper over comes the communication latency inside the fault injection environment and using this kind of fault injector, architecture errors occurred inside a memory is find out. During fault injection experiment, FPGA should send data back to host computer as response for fault tolerant analysis. If there is high data volume, FPGA should spend most of its time for communication. For solving this problem this paper place all the modules inside the FPGA. This system inject fault to the text saved inside the memory and find out the error. If error occurred it is corrected.

2. ADVANCED FAULT INJECTION TOOL FOR MEMORY UNIT

In fault detection method first faulty free experiment (Golden) is carried out. After that the faulty experiment wills turns on. Comparing the result of these experiment fault detection takes place.

2.1 Fault injector managing module

This module is responsible for controlling the faulty and fault-free experiment. This is done by the signal Golden. If golden=1 faulty –free experiment is executed. Otherwise faulty experiment will carry out.

2.2 Observation module

Block diagram is shown in fig 1. Observation module starts to record data from observation points after getting triggered by fault injection managing module. It consists of two adders. Golden run adder start it's working during the golden run and the faulty adder during the faulty experiment. So the observation is down using simple adder logic. Golden register and faulty register will turns on during the golden run and faulty run respectively. The golden adder will count in an order which depend on the observation point. And the faulty adder count in irregular order. The result saves inside the corresponding registers which are controlled by the golden register.

3) Result analyzer

Result analyzer compares the values inside faulty and golden registers. If it find any inequality the counter start it's counting.

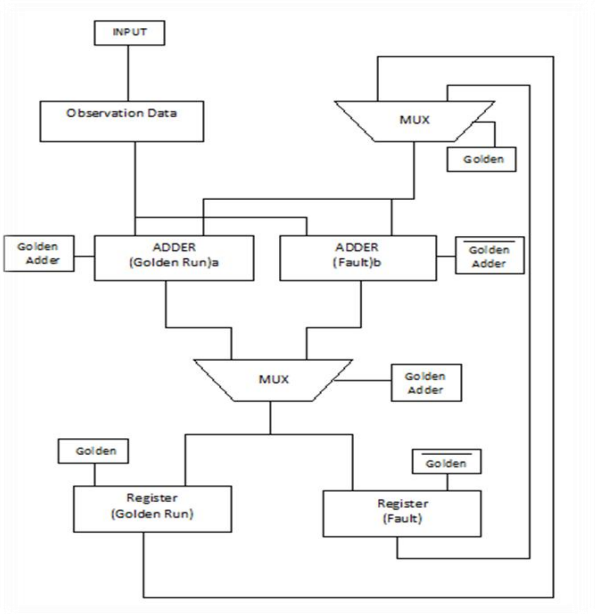

Fig -1: Observation module

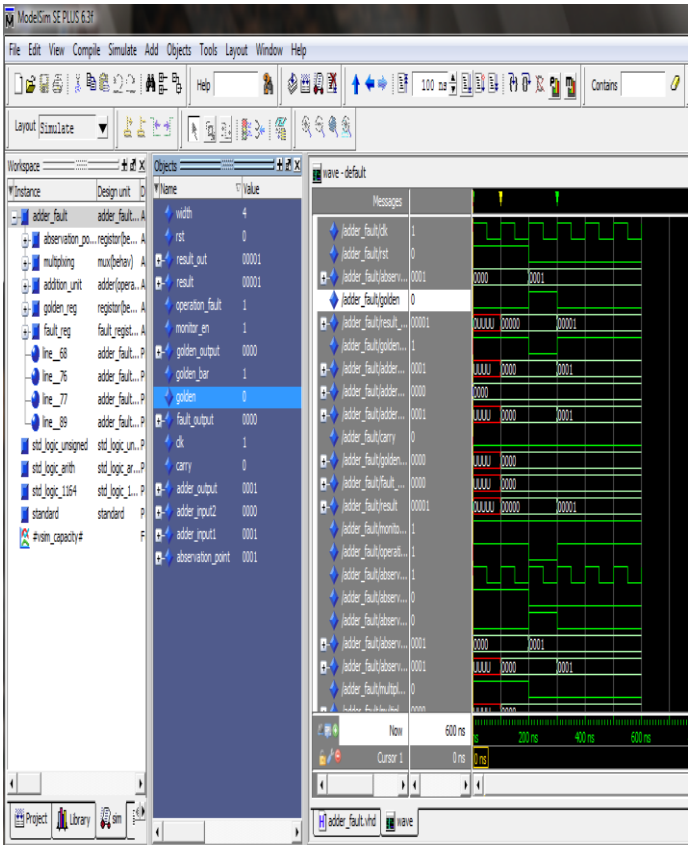

Fig -2: Simulation result

3. EXPERIMENTAL RESULT

In this experiment, we used SPARTAN3E FPGA for implementing memory and fault injection environment. All elements are designed by VHDL language. After implementing fault injection tool text data is input to the memory [6] through MAT LAB. The fault is injected to this text data and the errors in the memory will find out. if error is present correct the error and display the result. Simulation result for the fault injection is shown in fig 2.

4. FUTURE WORK

Using this the error in the memory unit can be detected. As a future work we can locate the error and correct it. For that the corresponding check bit is saved along with the data bit. The block diagram is shown in the fig 3.

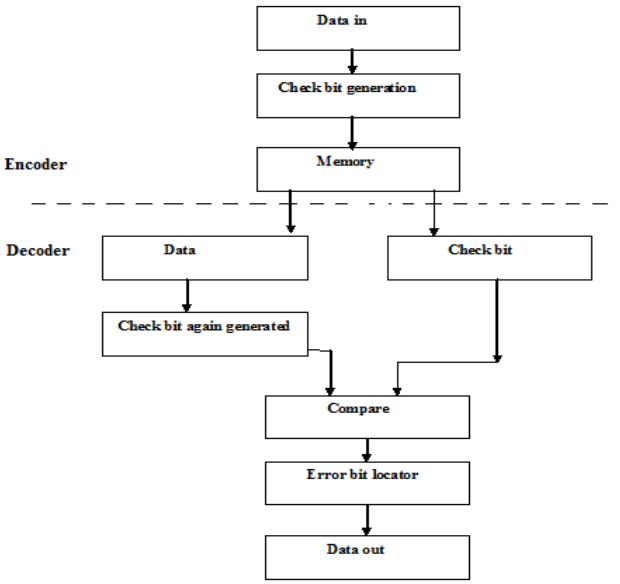

Fig -3: Memory error correction

5. CONCLUSION

Fast fault injection tool which is based on FPGA is implemented. This tool reduces the communication latency by implementing all fault injection parts inside FPGA. Using this fault injection, fault is injected to the memory unit and the corresponding architecture errors and tolerance are determined. Similarly this method can be used to find out the tolerance and errors of all parts of embedded processor. But the problem is related with observation time. But if we make it longer, probably more accurate results will get.

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