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A HIGH PERFORMANCE CLOCK DISTRIBUTIOIN NETWORK FOR SYSTEM ON CHIP

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Abstract—*Clocks distribution networks are important part of synchronous circuits to ensure the availability of the clock signal at each flip flops across the integrated circuit. There are several design methodologies proposed to design effective clock distribution networks.*

However, the exponential reduction in feature size of the transistors that necessitates high speed clock signals only create more difficulties in practically designing an efficient clock distribution network. This report discusses the various clock distribution used in conventional sequential circuits and some of the emerging designs.

In this paper, design of a clock distribution networks by first verifying its operation then building and testing your circuit stage by stage using Cadence Tools.In realization, first discuss the architecture and the implementation issues. Then, the coding process is simulated and verified by Cadence Tools.

Tools used: Cadence Tools(Virtuoso,ADEL,SpectreSimulator,Assura

Index Terms—Clock distribution networks, clock skew, De-skew buffers, H-trees, wireless clock distribution.

I. INTRODUCTION

Clock signals are important in synchronous circuits to synchronize different data signals arriving from different parts of the integrated circuit, such that the correct data is available for computation. Due to impedances present in interconnects there are mismatches in the clock arrival time due to spatial distances between two clocks. These mismatches in time are known as clock skews.Due noises caused by other interconnect lines running in parallel with the clock signals, clock signals arriving at two different registers with the same clock input experience a phase noise, commonly known as clock jitter [1].

Clock distribution networks ensure that these constraints regarding clock skew and jitters are minimized. Design of clock distribution network is however a cumbersome task and a designer must decide the clock distribution before the circuit is designed because the difficulty in designing an efficient clock distribution network increases in the latter stages of design [1]. Different techniques such as H-tree, buffered clock trees and meshed clock network are used in the design of the clock networks. Since the interconnects do not scale proportionally to the rapidly scaling transistor feature sizes that operate at high clock frequencies, sets a difficulty in designing an efficient
clock distribution networks.

The operation of most digital circuit systems, such as computer systems, is synchronized by a periodic signal known as a "clock" that dictates the sequence and pacing of the devices on the circuit. This clock is distributed from a single source to all the memory elements of the circuit, which are also called registers or flip-flops.

In a circuit using edge-triggered registers, when the clock edge or tick arrives at a register, the register transfers the register input to the register output, and these new output values flow through combinational logic to provide the values at register inputs for the next clock tick. Ideally, the input to each memory element reaches its final value in time for the next clock tick so that the behavior of the whole circuit can be predicted exactly.

The maximum speed at which a system can run must account for the variance that occurs between the various elements of a circuit due to differences in physical composition, temperature, and path length.In addition to clock skew due to static differences in the clock latency from the clock source to each clocked register, no clock signal is perfectly periodic, so that the clock period or clock cycle time varies even at a single component, and this variation is known as clock Jitter. At a particular point in a clock distribution network, jitter is the only contributor to the clock timing uncertainty.

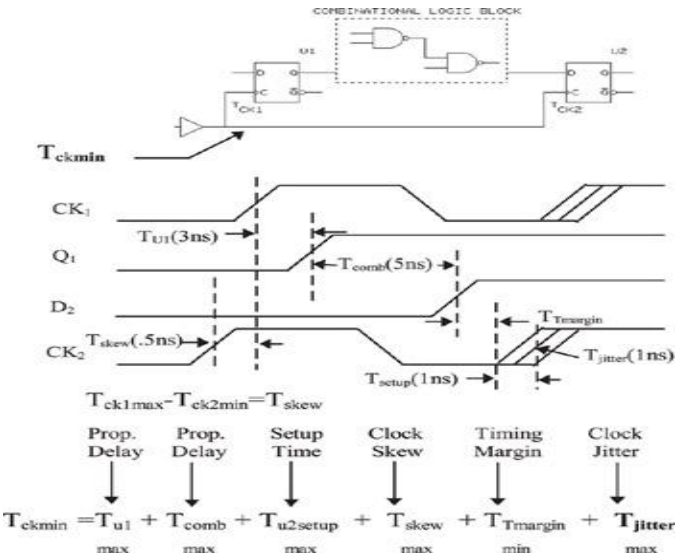

Fig-1: Clock Timing(Skew & Jitter)

In a synchronous circuit, two registers, or flip-flops, are said to be "sequentially adjacent" if a logic path connects them. Given two sequentially-adjacent registers R_i and R_j with clock arrival times at destination and source register clock pins equal to T_{Ci} and T_{Cj} respectively, clock skew can be defined as: $T_{skew\ i,\ j} = T_{Ci} - T_{Cj}$.

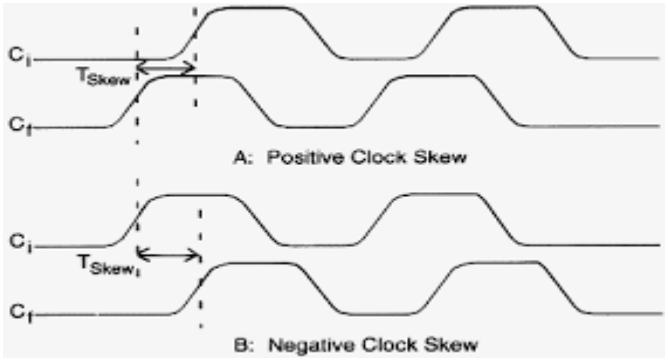

Fig-2: Positive & Negative Skew

II. CLOCK DISTRIBUTION NETWORKS

The Design methodology and structural topology of the clock distribution network should be considered in the development of a system for distributing the clock signals.The system speed,Physical die area,and power dissipation are greatly affected by the clock distribution network.

Requirements:-

1. clock waveforms must be particularly clean and sharp
2. No Skew.

Difficulty:-

1.The requirement of distributing a tightly controlled clock signal to each synchronous register on a large hierarchically structured integrated circuit within specific temporal bounds is difficult.

2. Technology Scaling in long global interconnect lines become much more resistive as line dimensions are decreased. This increased line resistance is one of the primary reasons for the growing importance of clcok distribution on synchronous performance.

Methodologies:-

Clock distribution strategies:- The relative phase between two clcoking element is important

Achieve zero skew routing:- Route clock to destinations such that cloc k edges appear at the same time.

The different Clock distribution networks are:

1.CLOCK TREE:-

a. Single Driver-If the interconnect resistance of the buffer at the clock source is small as compared to the buffer output resistance.

b.Maintaining high quality waveforms shapes (short transition times)

c.useelmore formula to compute delay

d.Balance delay paths.

Drawback:

Large delay,drive capability should be high.

The most general approach is to equipotential clock distribution by use of buffered trees and all patha are balanced.

Insert Buffers either at the clock source or along a path forming a tree structure.

Buffers:-

The Distributed buffers serve the double function of amplifying the clock signals degraded by the distributed interconnect impedance and isolating the local clock nets from upstream load impedances.

Design Methods:-

1. All node have capacitance
2. All Branches have resistance
3. Fix the load of each buffer
4. Compute no. of levels required
5. Position the buffers optimally.

Minimize delay,buffer delay =segment delay

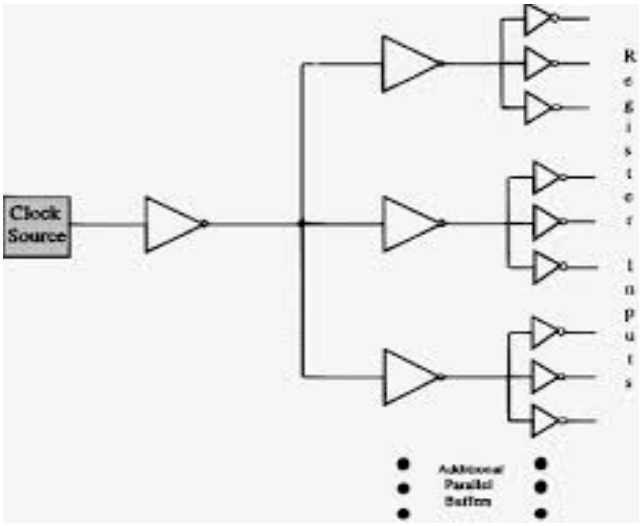

Fig-3:Buffered C lock Distribution Network

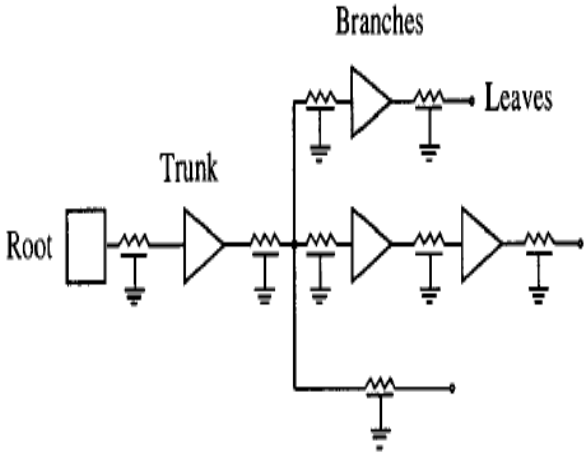

Fig-4:Tree Structure of a Clcok distribution Network

2.MESH VERSION OF CLOCK TREE:-

1.Shunt paths further down the clock distribution network are placed to minimize the interconnect resistance within the clock tree.

2. This mesh structure effectively places the branch reistances in parallel minimizing the clock skews

3 .GRID:-

1. Low Skew Achievable
2. Lots of Excess Interconnect
3.Large Power dissipation.

4. H-TREE:-

The primary goal in clock distribution design has traditionally been to transmit the clock signal to every register in the system at precisely the same time. Many routing algorithms exist for attaining zero clock skew, some more effective than others.

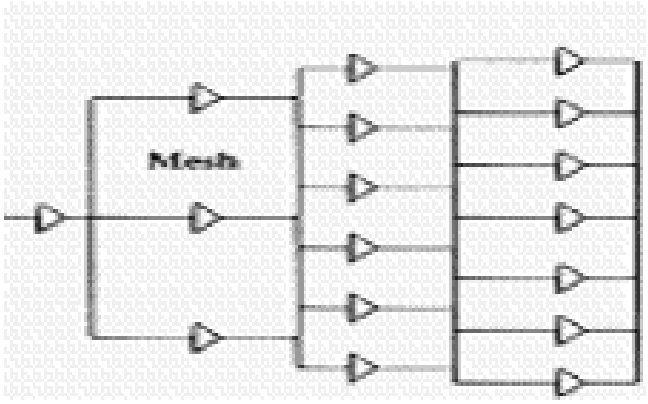

Fig-5:Mesh Version of C lock Distribution Network

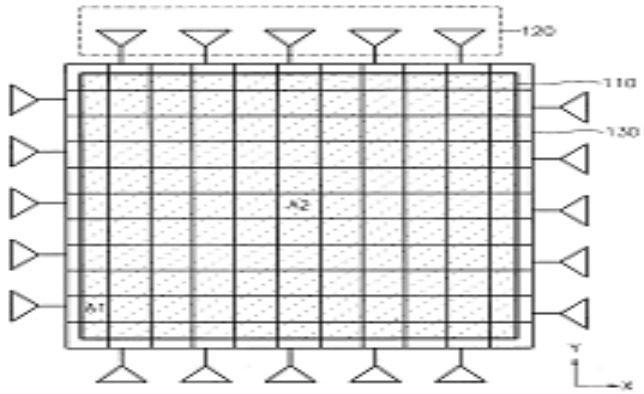

Fig-6 :Grid Version of C lock Distribution Network

In all cases, routing for zero clock skew results in a larger clock distribution network. The necessity to match delays forces increased route lengths, and often increases complexity.

A common zero skew routing strategy is the symmetric H-tree clock distribution network. This method aims to produce zero skew clock routing by matching the length of every path from clock source to register load. This is accomplished by creating a series of H-shaped routes from the center of the chip as illustrated by Fig4. At the corners of each "H" the nearly identical clock signals provide the inputs to the next level of smaller "H" routes. At each junction the impedance of the interconnect is scaled to minimize reflections.

For an H-tree network, each conductor leaving a junction must have twice the impedance of the source conductor. This is accomplished by decreasing the interconnect width of each successive level. This continues until the final

points of the H-tree structure are used to drive either the register loads, or local buffers which drive the register loads. Thus, the path length from the clock source to each register is practically identical in an H-tree distribution. A variant of H-tree is X-tree clock distribution network illustrated in Fig.

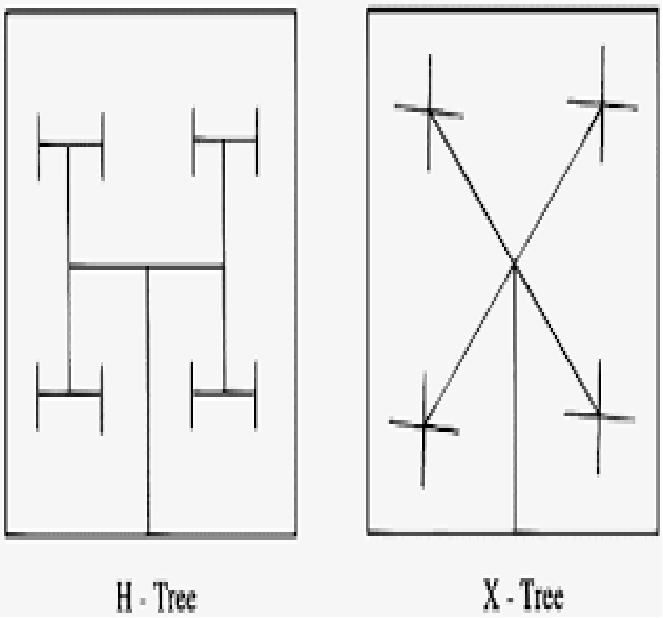

Fig-7:H-tree and X-Tree CDN

Obviously, this method does not truly produce zero clock skew. At some point the clock signal must be routed to the registers. Within this local block, clock skew will exist, but the block size is chosen such that the skew is insignificant. Other sources of skew include the variation in interconnect parameters, and the variation in active parameters for any buffers distributed through the H-tree network. Since the magnitude of the clock skew is only significant for sequentially adjacent registers, the symmetry provided by an H-tree distribution is largely unnecessary.

Considering the additional interconnect capacitance (which leads to increased power dissipation), the benefits of zero clock skew may not be worthy of the price. Even if sequentially adjacent registers are located on opposite sides of a chip, the concept of tolerable skew routing seems more effective. Allowing a measure of clock skew between registers significantly relaxes wiring constraints. This relaxation reduces overall interconnect capacitance and power dissipation.

This method inserts buffers with tuned delays to achieve an optimal clock skew schedule. This not only reduces the overall clock interconnect length, but increases system performance by allowing a higher frequency. Routing and distributing the clock signal are only part of the design process.

The method of clock signaling must also be determined. Typically, the clock signal is not treated any differently than any other signal in this respect. However, the uses of alternative clock signaling methods achieve significant power savings, often at minimal cost to performance and area.

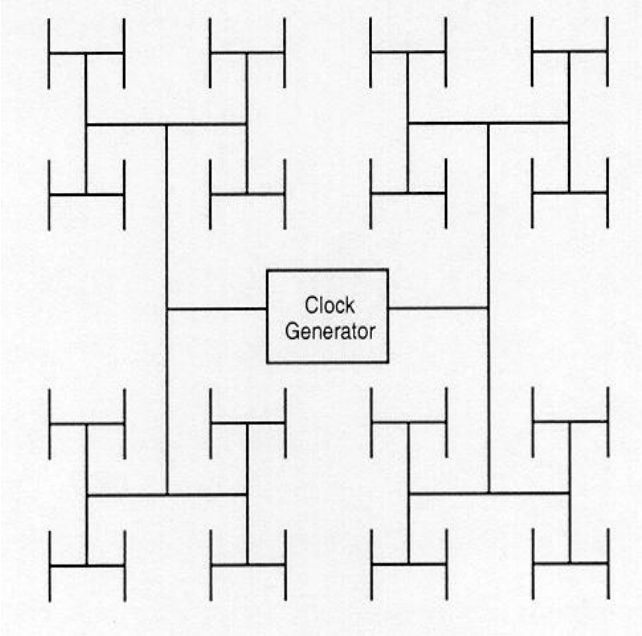

Fig.8: H-tree Clock distribution network

Difficulty:-

1.Clock routed in both vertical and horizontal directions.

For a standard two level CMOS process, this structure created added difficulty in routing clock lines without using either resistive interconnect or multiple high resistance between the two metal lines.

2.Interconnect Capacitance and the power dissipationis much greater for the H-tree as compared with the standard clock tree since the total wire length tends to be much greater.

6.TAPERED H-TREE:-

1. The Conductor widths in H-tree structures are designed to progressively decrease as the signal propagates to lower levels of the hierarchy.
2. This strategy minimizes reflections of the high speed clock signals at the branching points

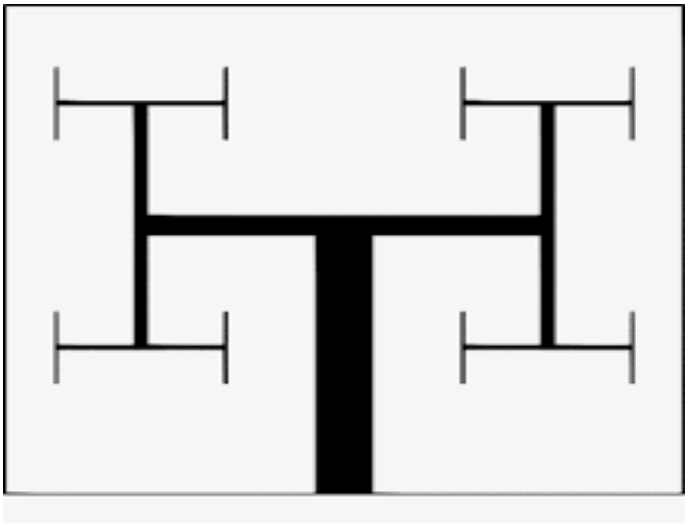

Fig.-9:Tapered H-Tree

For a System on chip, the clock distribution network can be a mixed method where depending of line resistance(interconnect) and load capacitance the design can be modeled as in the figure.

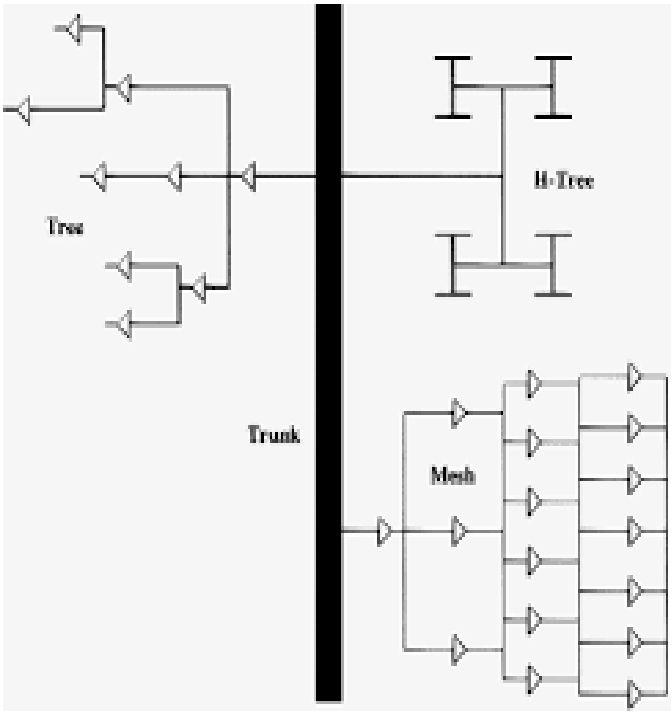

Fig-10:Common Structures of clock distribution networks including a trunk, tree, mesh and H-tree

III. SIMULATION RESULTS

1. Buffered Tree Clock Distribution Network:-

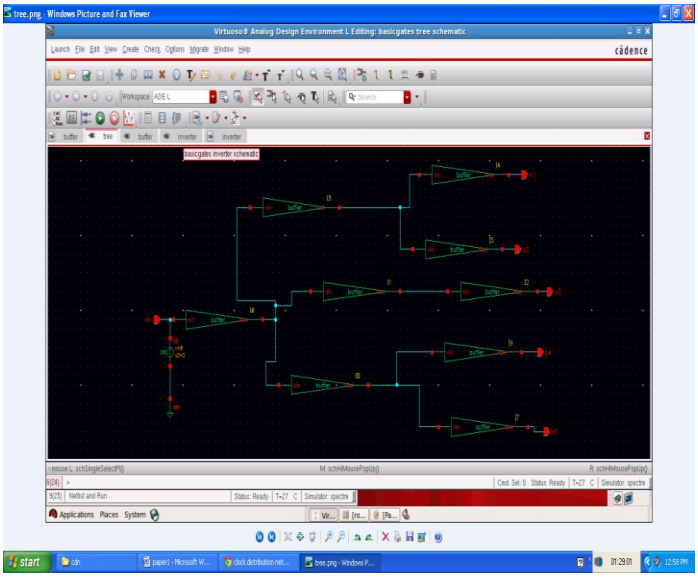

Fig-11:Buffered Tree CDN

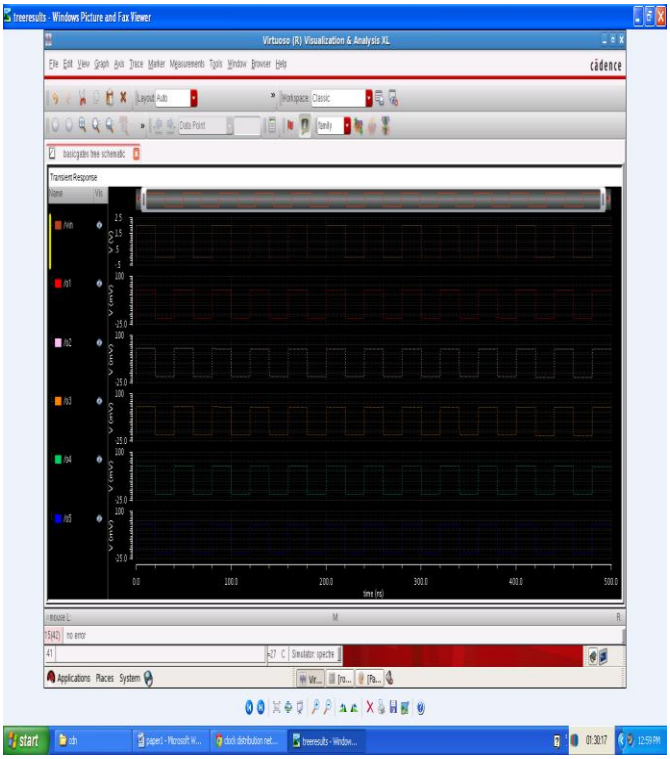

Fig-12:Simulation Results of Buffered Tree CDN

2. Mesh Version of Clock Distribution Network:-

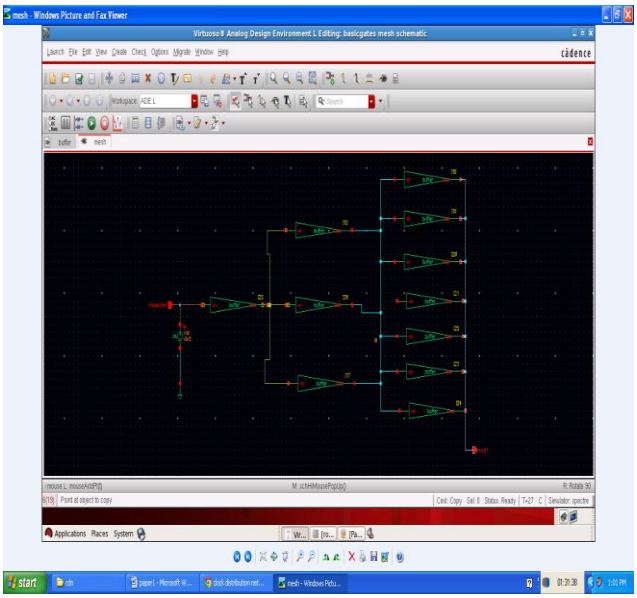

Fig-13: Mesh Version of CDN

3. Grid Version of Clock Distribution Network:-

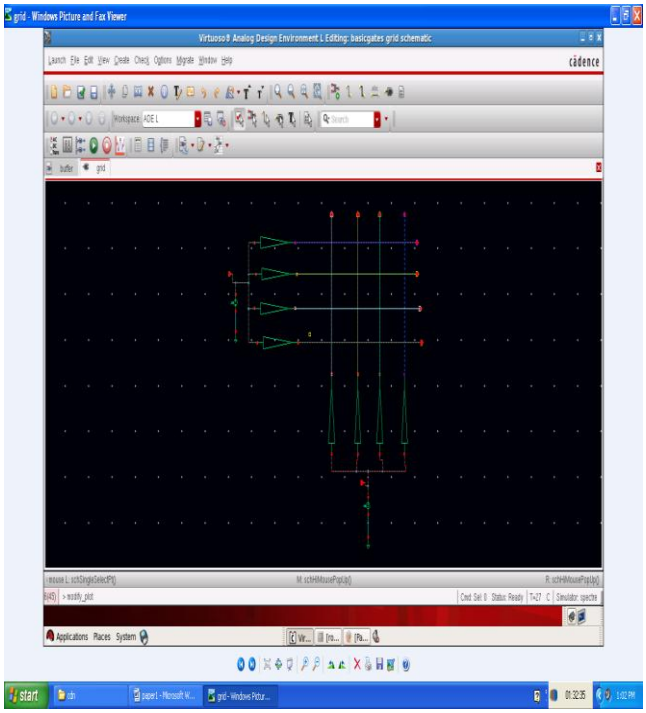

Fig-14: Grid Version of CDN

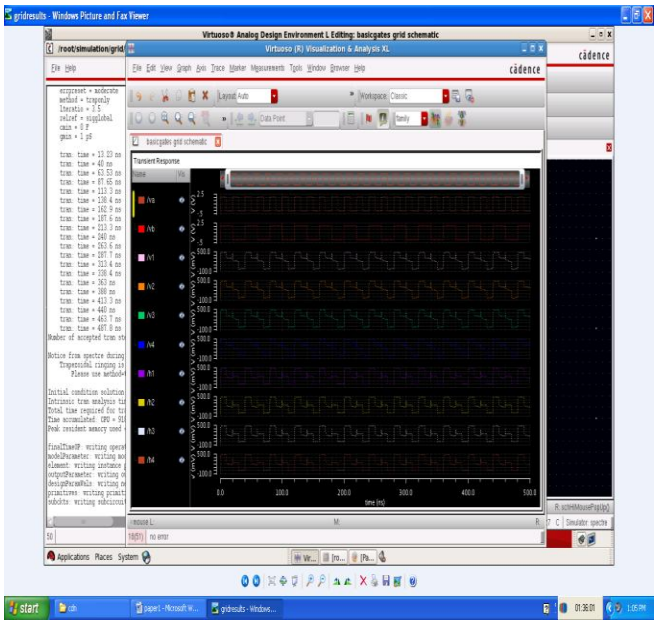

Fig-15:Simulation Results of Grid Version of CDN

4.H-tree Version of Clock Distribution Network:-

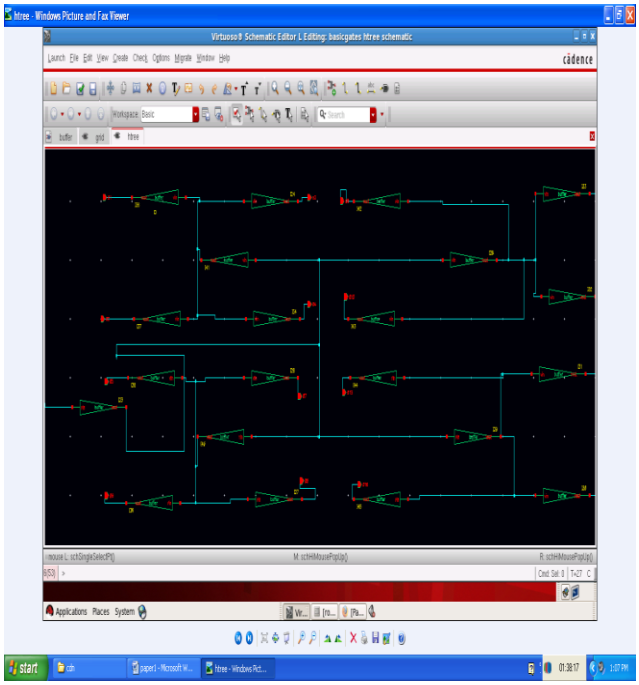

Fig-16: H-tree Version of CDN

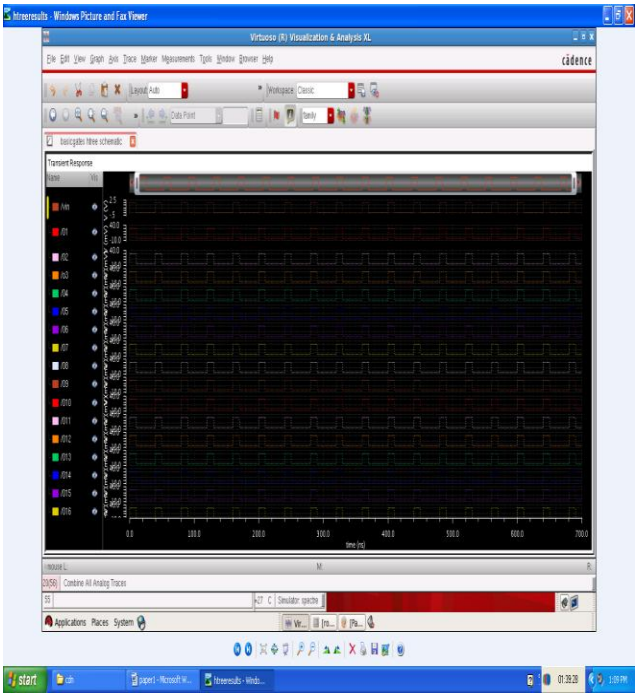

Fig-17: Simulation Results of H-tree Version of CDN

IV. RESULTS & CONCLUSION

In this paper, I investigated the performances and com-plexities of the Various ClockDistribution networks regarding effect of interconnect resistance and load capacitance when driving long signal lines. The Clock skew and clock jitter can be minimized by selection of proper clock distribution network and the parameters affecting it.

Various circuit-based design methodologies and techniques for distributing the clock signals have been suggested and practical circuit applications have been reviewed. It is the intention of this paper to integratethese various topics and to provide some sense of cohesivenessto the field of clocking and specifically, clock distribution networks.

It is often noted that the design of the clock distribution network represents the fundamental circuit-based performance limitation in high-speed synchronous digital systems. The local data path-dependent nature of clock skew, rather than any global characteristics, requires extreme care inthe design, analysis, and evaluation of high-speed clockdistribution networks.

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BIOGRAPHIES

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