

# Design of High Speed 64x64 Bit Fault Tolerant Reversible Vedic Multiplier

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Abstract - Multiplier is the most widely used arithmetic unit, having great importance in the digital world. For example- Digital Signal Processing, Processor and Quantum Computing etc. The Multiplier is the slowest and having a complex structure. In this paper a 64x64 bit high speed and fault tolerant multiplier architecture is proposed .The speed of the multiplier is enhanced with the help “Urdhva Tiryakbhayam” aphorisms from the ancient Vedic Indian Mathematics. Further the architecture of the multiplier is implemented using the Fault Tolerant Reversible Gates which exhibits a fault tolerant property by preserving the parity. Hence the parity checking method is used to find out the error and correction. Finally the Partial Product of the multiplier is added with the help of fault tolerant Carry look ahead adder. The coding is written in Verilog .While synthesis and simulation is performed using Xilinx 14.7i.

Key Words: Delay, Fault Tolerant Reversible gate, Vedic Method , Carry look ahead Adder.

## 1. INTRODUCTION

As the technology is scaling down from micro scale to nano scale . At such scale a new field is evolved is called quantum computing. Quantum computation based on the principle of reversible operation, means the information is conserved and performs certain task in nanosecond. [1]These are the main motivation to develop a high speed multiplier using reversible logic gates. In order to implement a high speed multiplier an Vedic algorithm is applied .Because it perform simple operation and yield result quickly. The multiplication process involves two step generation of partial product and addition of partial product , these two steps are concurrently perform by the Urdhva Tiryakbhayam algorithm of Vedic Mathematics .[5]

This paper proposes the implementation of fault tolerant reversible Vedic multiplier , with the aim to develop a high speed multiplier with Vedic method and the architecture

of multiplier is implemented with fault tolerant reversible gate in order to improves the reliability, reduces area.

The paper is describe under the following sections : Section 2 explain Reversible logic Gates, Section 3 Urdhva Tiryakbhayam aphorism, Section 4 Fault Tolerant Carry Look Ahead Adder Section 5 Proposed 64x64 bit Fault Tolerant Reversible Vedic Multiplier Architecture Section 6 shows the Result and Comparison and Section 7 shows the Conclusion.

## 2. REVERSIBLE LOGIC GATES

Reversible logic perform reversible computation means that the input can be recovered back from the output and the output can also be obtained from the input . Hence the reversible logic circuit are also called as the Information loss-less logic. Reversible logic is classified into types they are Basic Reversible gate and Fault Tolerant Reversible Gates. Reversible gate are those gates having the same number of the input lines and the output line. While Fault tolerant Reversible gate are also known as the parity preserving reversible gate which performs reversible computation as well as the preserve the parity at the input side as well as at the output side.[12] Some of the Fault Tolerant Reversible Gate are shown in the below:

### 2.1 Double Feynman Gate

The double Feynman gate is a 3\*3 gate are shown in the fig1. The input vector is I(A,B,C) and output vector is O(P,Q,R). The input parity is same as the output parity .Quantum Cost of F2G is equal to 2.

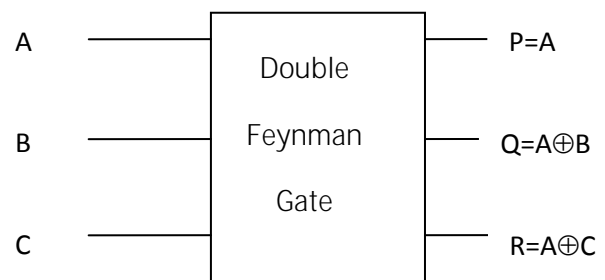


Fig- 1: Feynman Gate

### 2.2 Islam Gate(IG)

The Islam gate is a 4\*4 gate are shown in the fig 2. The input vector is I(A,B,C,D) and output vector is O( P,Q,R,S). The input parity is same as the output parity and Quantum Cost of F2G is equal to 7. It can perform AND,EX-OR function.

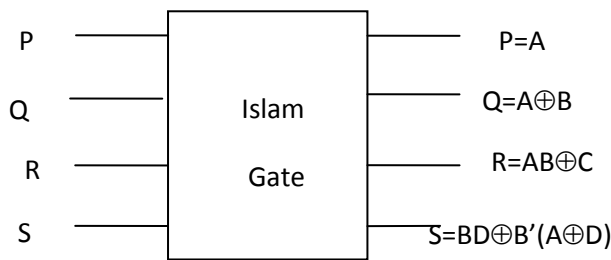


Fig- 2: Islam Gate

### 2.3 NFT Gate

The NFT gate is a 3\*3 gate are shown in the fig 3. The input vector is I(A,B,C,D) and output vector is O( P,Q,R,S). The input parity is same as the output parity. Quantum Cost of NFT is equal to 5. It can perform NOT, OR, XOR,NAND,AND,EX-OR function.

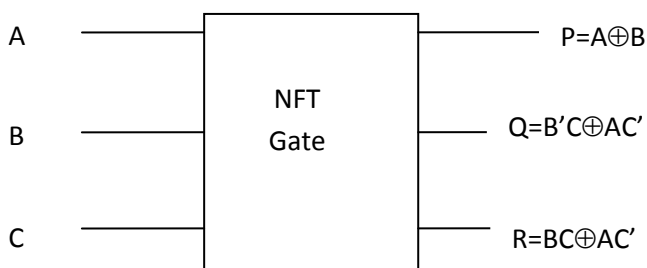


Fig- 3: NFT Gate

### 3. URDHVA TIRYAKBHYAM APHORISMS

Urdhva Tiryakbhyam(UT) sutra is the multiplication formula from the ancient Vedic mathematic which suits for the multiplication of decimal number, hex as well as for the binary number. This features of UT algorithm compatible with the digital systems. The UT provides the fast computation because the partial product and their sums are calculated parallel. The Sanskrit words Urdhva means vertical and Tiryakbhyam" means "crosswise" in English..These algorithm performs crosswise and vertical operations

between the two numbers which shown in the fig 4 .The procedure is adapted for the multiplication is based on the concept in which generation of the partial products and additions are done concurrently which increases the speed of multiplication operation.[7]

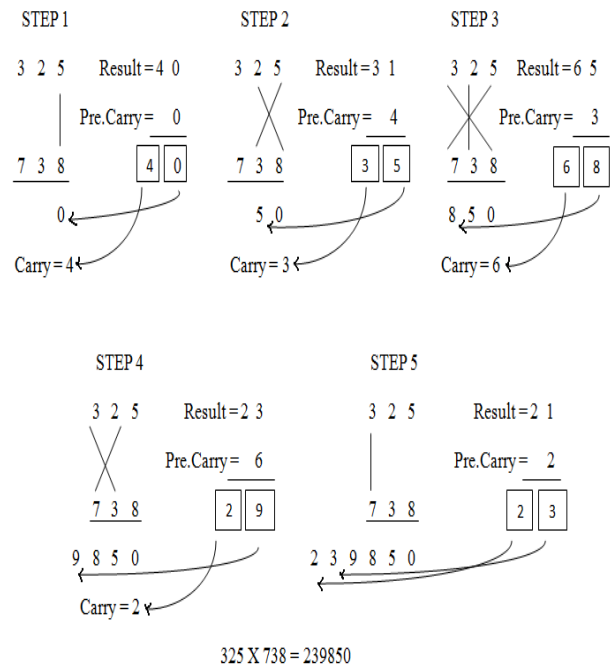


Fig- 4: Urdhva Tiryakbhyam multiplication of the two decimal number

4. FAULT TOLERANT CARRY LOOK AHEAD ADDER  
Carry-look ahead adder is the fastest adder among the all adders. It generates carry bit in advance before it generates the sum, which reduce computation time to obtain final results.[10] Here the Carry look ahead adder is implemented using the New Fault Tolerant gate (NFT) gate and Double Feynman gate. Fault tolerant carry look ahead adder is used to add the partial product of the multiplier blocks .The 2-bit fault tolerant carry look ahead adder is shown in the fig 5.

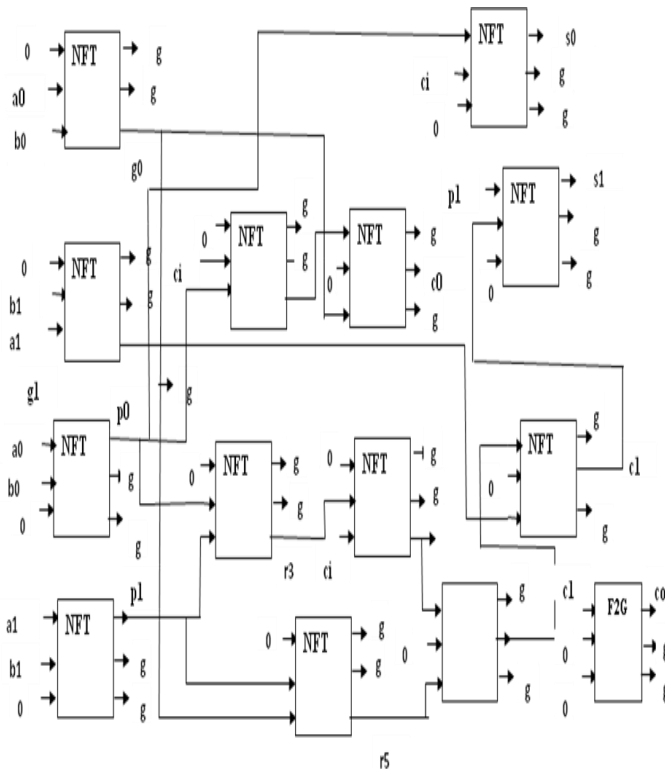


Fig 5 : 2-Bit Fault Tolerant Carry Look Ahead Adder.

### 5.IMPLEMENTATION OF PROPOSED MULTIPLIER ARCHITECTURE

The 64x64-bit high speed fault tolerant reversible Vedic multiplier architecture is constructed by using 2x2 bit,4x4 bit,8x8 bit ,16x16bit ,32x32bit fault tolerant reversible Vedic multiplier. In the first step 2x2 multiplier architecture is implemented with fault tolerant reversible gate, and Urdhva Triyagbhayam algorithm is applied, which is the major building block for the construction of 64x64 bit multiplier. Further 4x4bit, 8x8 bit, 16x16 bit,32x32 bit Fault tolerant reversible Vedic multiplier are shown in the below section.

#### 5.1 2x2 Bit Fault tolerant Reversible Vedic Multiplier

The basic building block of the 2x2 fault tolerant reversible vedic multiplier is constructed using the fault tolerant reversible gate they are 2 Islam gate, 3 NFT gate and 3 Double Feynman gate. And the Urdhva Tiryagkbhyam algorithm is applied for multiplication. Let us consider 2-bit of input say A0A1 and B0B1 as per vedic algorithm . The output is obtained in 4-bit P0,P1,P2,P3. where P0 is obtained by performing vertical

multiplication of A0 and B0. The P1 is obtained by the cross wise multiplication and their addition that is A1B0 and A0B1. The P2 is obtained by the addition of the product vertical data A1 and B1. Finally the P3 is the carry generated from the calculation of P2.

#### 5.2 4x4 Bit Fault Tolerant Reversible Vedic Multiplier

The 4x4 bit Fault tolerant Reversible Vedic multiplier is designed using four 2x2 bit fault tolerant Reversible Vedic multiplier. While the output of the four 2x2 multiplier is added with the help of carry look ahead adder and the carry look ahead is also implemented using fault tolerant reversible gate. The block diagram of the proposed 4x4 Fault Tolerant Reversible Vedic multiplier is shown in the fig 6.

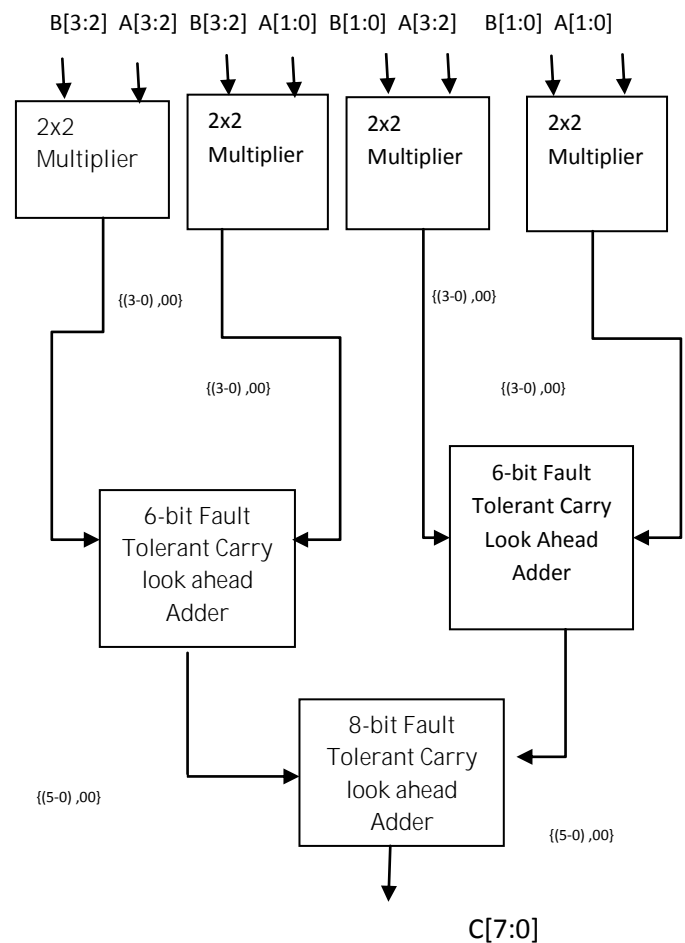


Fig-6 :4x4 Bit Fault Tolerant Reversible Vedic Multiplier

### 5.3 8x8 Bit Fault Tolerant Reversible Vedic Multiplier

The 8x 8 bit multiplier is implemented using four 4x4 bit multiplier .The outputs of these multipliers are added with fault tolerant carry look ahead adder to obtain the final product. Thus, in the final stage three adders are also required. Now the basic building block of 8x8 bits multiplier is shown in the fig 7.

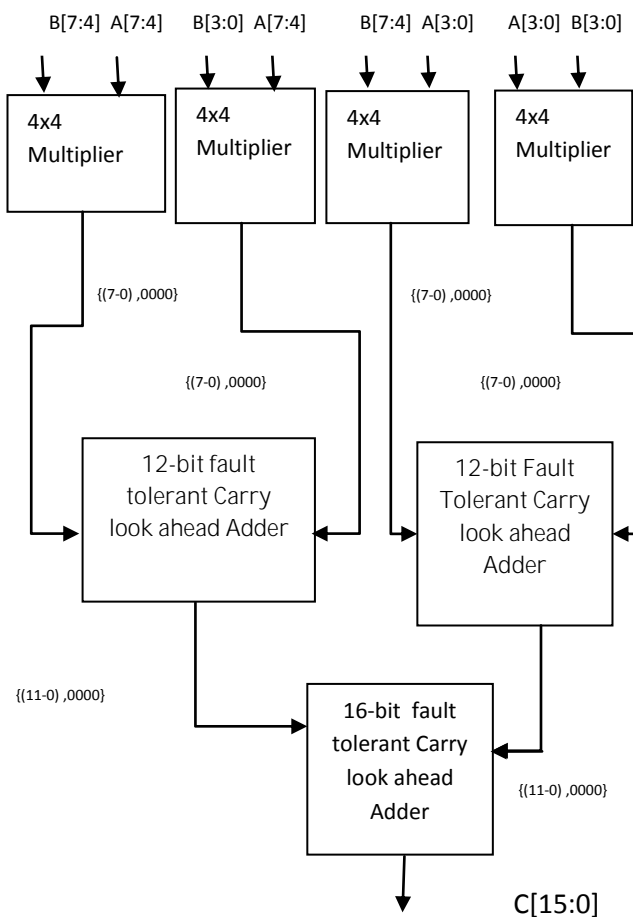


Fig -7 :8x8 Bit Fault tolerant Reversible Vedic Multiplier

### 5.4 16x16 Bit Fault Tolerant Reversible Vedic Multiplier.

The 16x16 bit multiplier is implemented using four 8x8 bit multiplier. The outputs of these four 8x8 bit multipliers are added with fault tolerant carry look ahead adder to obtain the final product. Thus, in the final stage three adders are also required. Now the basic building block of 16x16 bits multiplier is shown in the fig 8.

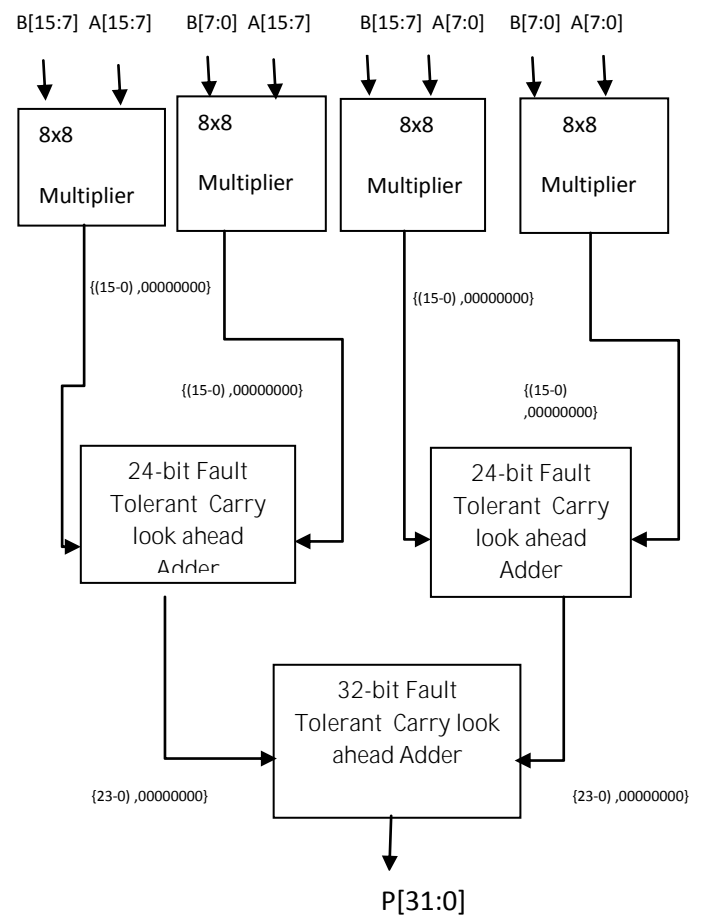


Fig -8 :16x16 Bit Fault Tolerant Reversible Vedic Multiplier

### 5.5 32x32 Bit Fault Tolerant Reversible Vedic Multiplier.

The 32x32 bit is implemented using four 16x16 fault tolerant reversible Vedic multiplier. The outputs of four 16X16 bit multipliers are added with fault tolerant carry look ahead adder to obtain the final product to produce 64-bit output which is shown in fig 9.

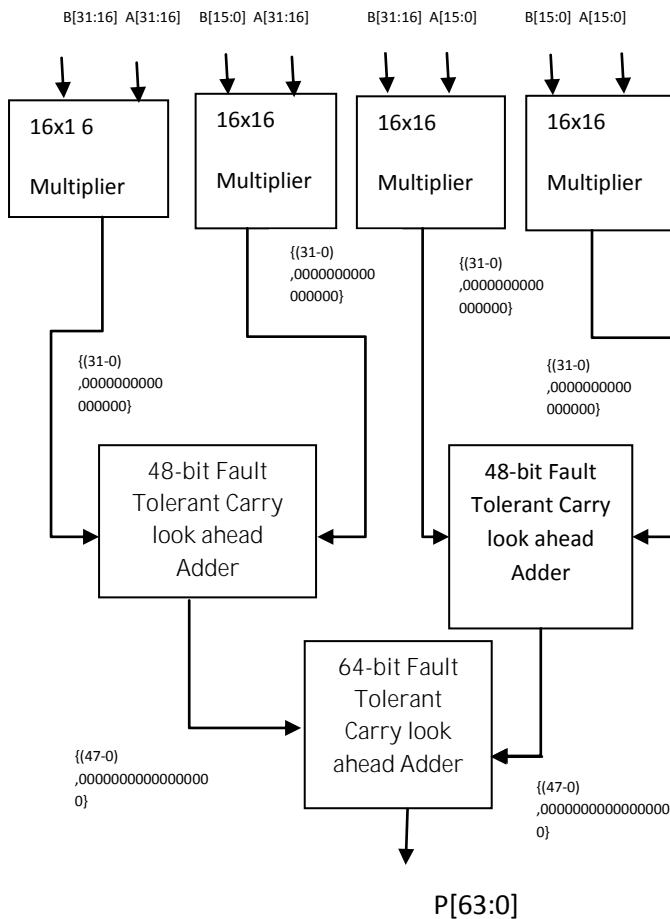


Fig -9 :32x32 Bit Fault Tolerant Reversible Vedic Multiplier

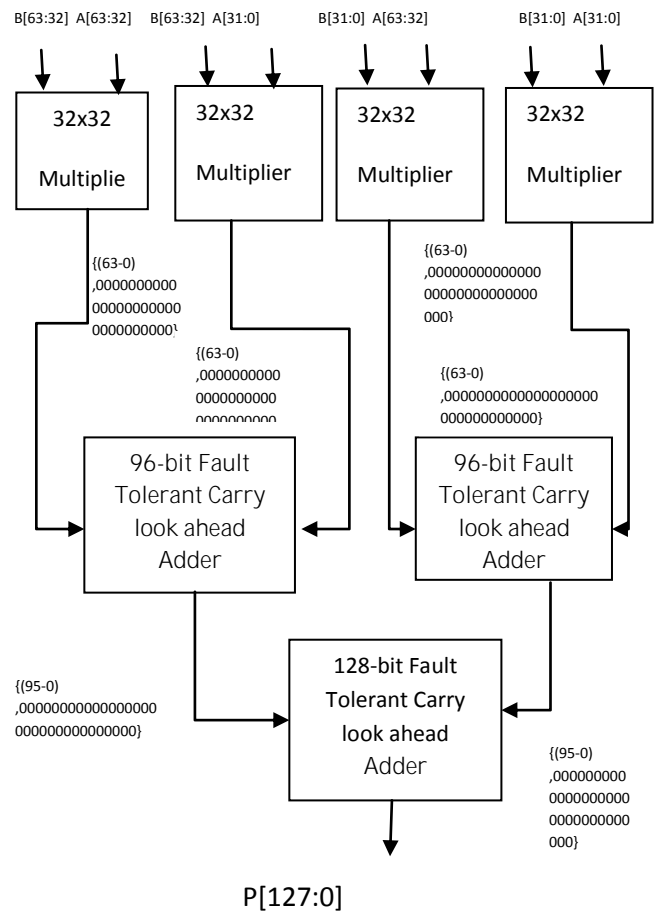


Fig-10 :64x64 Bit Fault Tolerant Reversible Vedic Multiplier

### 5.6 64x64 Bit Fault Tolerant Reversible Vedic Multiplier.

The 64x64 bit is implemented using four 32x32 fault tolerant reversible Vedic multiplier. The outputs of four 32X32 bit multipliers are added with fault tolerant carry look ahead adder to obtain the final product. Now the basic building block of 64x64 bit fault tolerant reversible Vedic multiplier shown in the fig 10.

### 6. RESULT AND COMPARISON

In this paper 64x64 bit Urdhva Tiryakbhyam multiplier using fault tolerant reversible gates are designed in Verilog and the synthesis and simulation was done using Xilinx14.7i. The synthesis result obtained for the Proposed Fault tolerant Reversible Vedic multiplier and simulation results and RTL synthesis are shown in Figures 11 and 12 respectively. The device utilization summary of 64x64 fault tolerant reversible Vedic multiplier for Xilinx, Virtex 6-family is shown below:

Device Utilization Summary: Selected Device : 3s500efg320-5.

Number of LUT Flip Flop pairs used: 9783

Number with an unused Flip Flop: 9783 out of 9783  
100%

Number with an unused LUT: 0 out of 9783 0%

Number of fully used LUT-FF pairs: 0 out of 9783 0%

The simulation result is obtained for the Proposed fault tolerant Reversible Vedic multiplier for verification is shown in fig 11. In behavioral simulation test is performed for the given input bits-

a) For 64x64 bit fault tolerant reversible Vedic multiplier input ,multiplier a="12 and multiplicand b= "12" and we get 128-bit output c= "144" . Similarly another input is applied where multiplier a= "18" and multiplicand b= "18" also we get the output in 128 bit , c= 324.

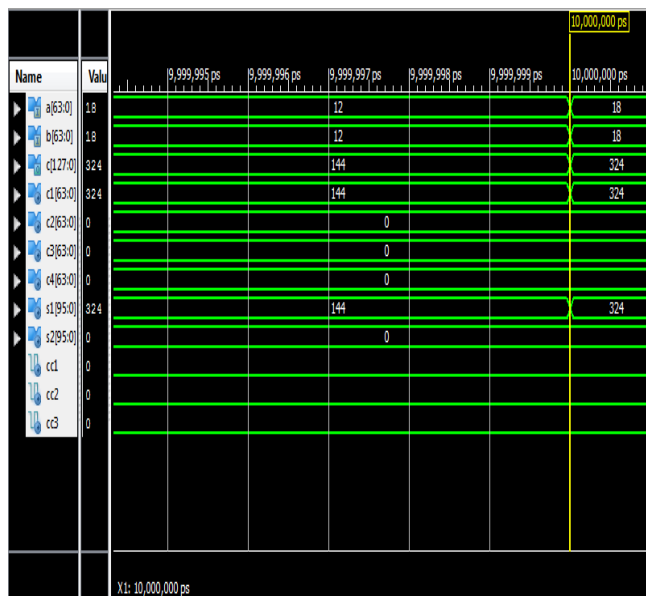


Fig-11:Simulation result of Proposed 64x64 Bit Fault Tolerant Reversible Vedic Multiplier with carry look ahead adder (12x12=144) &(18x18=324)

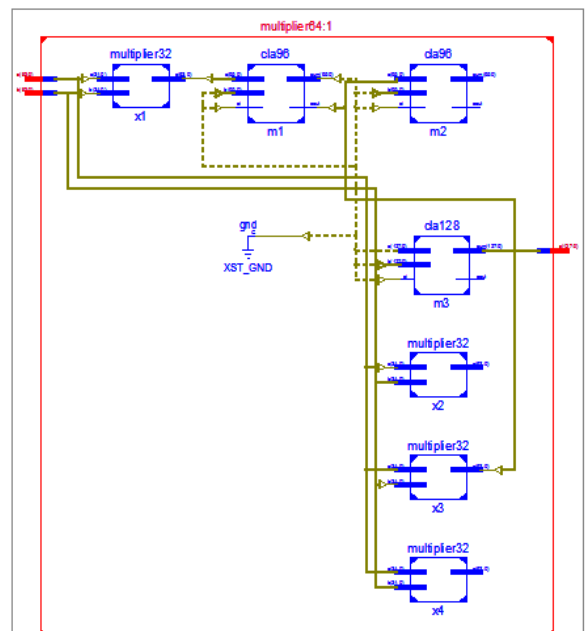


Fig-12:RTL Schematic of Proposed 64x64 Bit Fault Tolerant Reversible Vedic multiplier

Table I shows the comparisons of Proposed 64x64 bit Fault tolerant Reversible Vedic Multiplier using carry look ahead adder in terms of computational path delays (ns) and fault tolerant property.

Parameter	64-bit Array Multiplier	64-bit Vedic multiplier	64-bit Booth Multiplier	64-bit Proposed Fault Tolerant Reversible Vedic multiplier
	[19]	[19]	[19]	
Delay(ns)	47.855	45.601	46.340	40.942
Fault Tolerant Property	No	No	No	Yes

Table I:Comparisons of Proposed 64x64 bit Fault Tolerant Reversible Vedic Multiplier using carry look ahead adder and Array Multiplier, Vedic Multiplier Booth Multiplier.

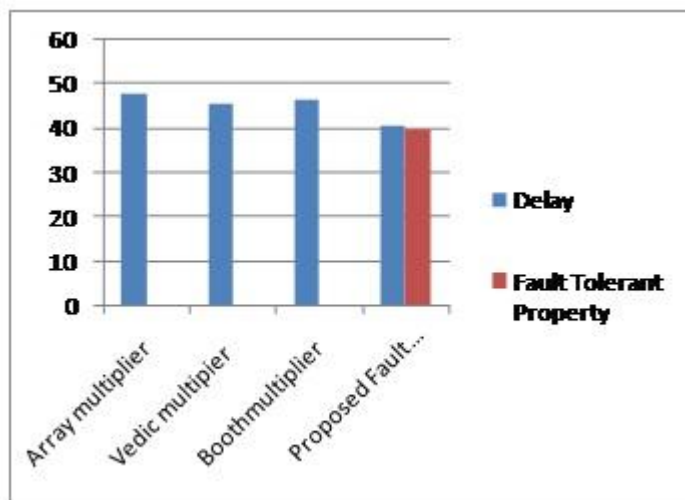


Chart-13: Comparison Between the Existing Array Multiplier, Vedic Multiplier Booth Multiplier and Proposed Fault Tolerant Reversible Vedic Multiplier

## 7. CONCLUSION

This paper presented a high speed multiplier using Urthva Tiryakbhayam algorithm for multiplication based on Vedic mathematics and the partial product addition is done by the fault tolerant carry look ahead adder which offered fast computational speed. While architecture of multiplier is implemented using fault tolerant reversible gate. The Proposed 64x64 Fault tolerant Reversible Vedic Multiplier have minimum path delay and fault tolerant capability when compared to other multipliers.

In future, high performance adaptive LMS filter can be designed using fault tolerant reversible Vedic multiplier which provide faster computational speed, These multiplier used in quantum computer, as quantum computing perform computation in reversible manner.

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