Study of Tree Multiplier Using Reversible Logic Gate

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Abstract— The objective of this project is to design high performance arithmetic circuits which are faster and have low power consumption using a new adiabatic logic family of CMOS and to analyze its performance for sequential circuits and effects upon cascading. Reversible logic is widely used in low power VLSI. This adiabatic logic family is best suited to arithmetic circuits because the critical path is made of a long chain of cascaded reversing gates. The more advantage of this logic which is higher speed and low power consumption is observed upon cascading which ***is more precise, it's bett****er suitable for arithmetic circuits. The proposed multiplier is better and provides better result in terms of the number of gates, constant inputs, garbage outputs, hardware complexity, and number of transistors required as comparison with the existing circuit. The data relating to the primitive reversible gates which are available in literature and helps researches in designing higher complex computing circuits using reversible gates are represented by this paper.*

Keywords— Reversible logic gate, Wallace multiplier, Reversible circuit, low power.

1. INTRODUCTION

The reversible logic operations do not erase (lose) information and dissipate very less heat. Demand of reversible logic is high in high speed power aware circuits. Interest of reversible circuit is high in, , nanotechnology, quantum computing optical computing and low power CMOS design . Application of reversible logic is very high in quantum computers. Quantum network (or a family of quantum networks) can be viewed as a quantum computer. Quantum network can be consists of quantum logic gates; each. An elementary unitary operation on one, two or more two–state quantum systems called qubits is performed by each gate.

An elementary unit of information corresponding to the classical bit values 0 and 1 is represented by each qubit is reversible, Quantum networks effecting elementary arithmetic operations such as addition, multiplication and exponentiation cannot be directly deduced from their classical Boolean counter parts (classical logic gates such as AND or OR are clearly irreversible) because any unitary operation is reversible. Thus, reversible logic components can be made from quantum arithmetic. Serious problems for today's computer chips are heat generation and power dissipation.

The 30-year-long trend in microelectronics has been to increase both speed and density by scaling of device components. In the last decade the heat generation is reduced by higher level of integration and new fabrication processes during this trend. Quantum gates which are represented by unitary matrices have potentials to implement reversible logic circuits. A valid quantum operation is represented by each quantum gate. Each quantum gate must be unitary and hence must be reversible. Many classical logic gates are irreversible but quantum gates are reversible.

II. Reversible Logic Gate:

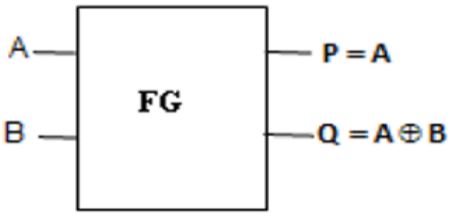
1) If n is input and m output is logic gate and there is a one-to-one correspondence between its inputs and outputs, and then this type of logic gate is called to be reversible.

2) If and only if the (Boolean) function is objective then the gate is said to be reversible. In other words, a gate is reversible if each of its input vector maps into a unique output vector and vice versa.

Following are basic reversible gates:

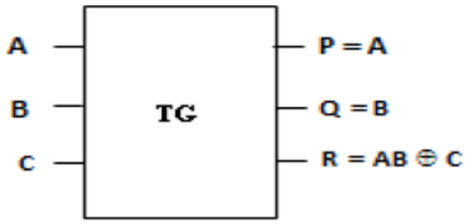
Feynman gate:

The Feynman gate which is a 2*2 gate and is also called as Controlled NOT and it is widely used for fan-out purposes. The inputs (A, B) and outputs P=A, Q=A XOR



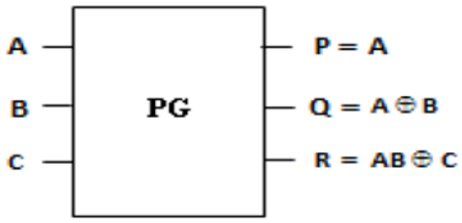
Toffoli gate :

Toffoli gate which is a 3*3 gate with inputs (A, B, C) and outputs P=A,Q=B, R=AB XOR C.



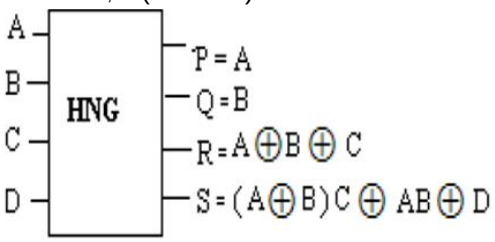
Peres gate :

Peres gate which is a 3*3 gate having inputs (A, B, C) and outputs
P = A; Q = A XOR B; R = AB XOR C.



Haghparast Navi gate:

Each output is annotated with the corresponding logic expression. It is 4*4 gate having inputs(A,B,C,D) and output P=A,Q=B,
R=AB XORC,S=(A XOR B)C XOR AB XOR D.



This document proved that the proposed multiplier is better and optimized, compared to its existing counterparts with respect to the number of gates, constant inputs, garbage outputs, hardware complexity, and number of transistors required.

By using full adders and half adders in their reduction phase. This paper presented that Wallace high-speed multipliers half adders do not reduce the number of partial product bits. Hence, reduction in the hardware complexity can be achieved by the number of half adders used in a multiplier reduction. This document proposed a novel reversible multiplier and the aim of this paper is to decrease the depth of the circuit. In this paper the depth of novel reversible multiplier is less without increasing the quantum cost or the number of garbage outputs with respect to previous counterparts. In proposed design, using Peres gates partial products are generated.

This study provided the initial threshold for building more complex system which can execute more complicated operations using reversible logic. It is proved that the proposed multiplier architecture using the proposed TSG gate is better than the existing counterpart in literature in terms of reversible gates and garbage output.

III. Wallace Tree Multiplier:

Reduction in number of partial products to be added can be achieved by using Wallace tree multiplier. Reduction in number of addition in critical path can be aimed using tree structure. Figure Below shows the architecture of 5 bit Wallace tree multiplier .

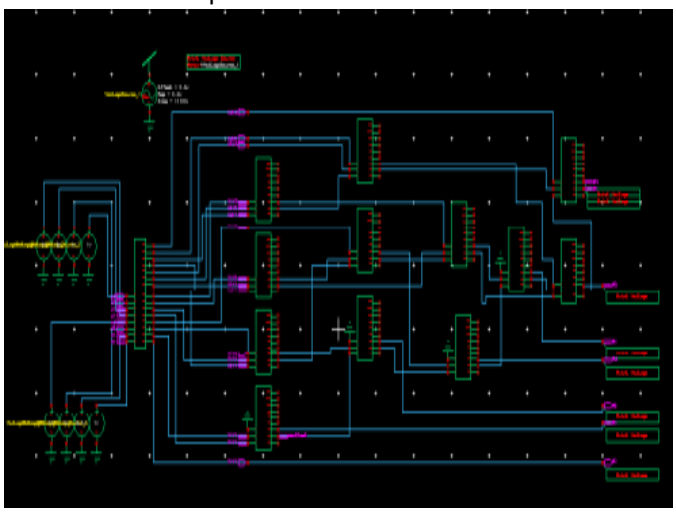


Figure: Proposed Architecture of 4 bit Wallace Tree Multiplier

IV. CONCLUSION

Wallace tree multiplier method reduces partial product array and it can be used for implementation of reversible multiplier with the use of reversible logic gate using pass transistor logic. By using reversible logic gate the number of transistor is reduced and hence hardware complexity is less. Due to these reasons, Reversible multiplier is better and most favorable method than other methods.

There are many uses of reversible logics such as low power CMOS, nanotechnology, quantum computing and optical computing.

REFERENCES

[1] Hatkar A. P.,Hatkar A. A., Narkhede N. P."ASIC design of reversible multiplier circuit" 2014 IEEE Conference.

[2] Ron S. Waters, Member, IEEE, and Earl E. 2008 IEEE Conference Jr., Fellow "A Reduced Complexity Wallace Multiplier Reduction" 2010 IEEE transaction

[3] Fateme Naderpour, Abbas Vafaei "Reversible Multipliers: Decreasing the Depth of circuit"2008 IEEE Conference.

[4] Himanshu Thapliyal and M.B Srinivas "Novel Reversible Multiplier Architecture Using Reversible TSG Gate" 2006 IEEE

[5] Prashant .R. Yelekar Prof. Sujata S. Chiwande" Introduction to Reversible Logic Gates & its Application".

[6] Md. Belayet Ali1 , Hosna Ara Rahman2 and Md. Mizanur Rahman3"Design of a High Performance Reversible Multiplier"International JournalVol. 8, Issue 6, No 1, November 2011

[7] M. Haghparast, Somayyeh Jafarali Jassbi, K. Navi and Omid Hashemipour, " Design of Novell Reversible Multiplier Circuit Using HNG gate in Nanotechnology", world applied science journal 3[6], 2008, pp.974-978

[8] Y van Van Rentergem and Alexis De Vos, "Optimal Design of a reversible full adder", Internaltion Journal of Unconvection Computing, Vol.-1, 2005, pp339-355.

[9] Md. Belayet Ali, Hosna Ara Rahman and Md. Mizanur Rahman, "Design of high performance reversible multiplier", IJCSI International Journals of Computer Science Issues, Vol.-8, Issue-6, No.-1, 2011, pp.134-141

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