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Power Reduction Techniques for Digital Systems

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Abstract - *Power reduction is the most important aspect considered while designing the digital systems. Various approaches have been used in the past to reduce the power consumption of the digital systems. The paper presents the review of various techniques that have been used in the past for the reduction in the power consumption of the digital systems.*

Keywords: Power reduction, Low power, Digital systems design.

I. INTRODUCTION

Designing a low power system is very important because high power consuming systems often have large battery pack, short battery life and are generally costly. Various techniques that have been used in the past for power reduction have been discussed in section II and the conclusion of the review has been given in section III summarizing the whole discussion.

II. LITERATURE REVIEW

Micheli et al. designed a Computer Aided Algorithm for the state coding. They implemented the design using Programmable Logic Array (PLA) considering D Flip-Flops as the memory elements [1]. PLA had been used because any logic circuit can be implemented using PLA. The authors advised to modify the proposed algorithm for components other than PLA and D Flip-Flops.

D. Liu and C. Svensson estimated the Power Consumption of the CMOS Chips based on Gate Count, Memory Size, Logic Implemented and Layout Styles. They concluded that the power consumption can be reduced by reducing the operating clock frequency and by designing the chip using *Full Custom Design* style [2]. The operating clock frequency can be reduced by making the sequential components double edge triggered.

Surti et al. used two different code lengths for the state assignment. Highly probable states were coded using the less number of bits and less probable states were coded using the more number of bits. An additional Set Detection Logic was used to switch between the set of less number of bits and the set of more number of bits depending on whether the next state is highly probable or less probable respectively [3]. The number of states in highly probable state set was more than the number of states in less probable state set so that the power reduction due to highly probable state set could be more than the extra power required due to the less probable state set.

Benini et al. divided the state machine into several sub machines. Power consumption was reduced by activating only one sub machine at a time. Two sub machines were active together only at a time when the control is being passed from one sub machine to the other. The proposed approach increased the area due to the additional signals required for the communication between the sub machines [4].

E. T. Lee introduced a method for the state minimization. The author used the approach similar to the K-map (Used for the Boolean Expression minimization) [5]. The author named the proposed approach as L-map method. The K-map method is used for the Boolean expression minimization while the L-map method had been used for state minimization.

S. Chattopadhyay and P. N. Reddy presented an algorithm for the state assignment. Power consumption was reduced by the reduction of Hamming Distance between the codes of the states. The authors designed a Computer Aided Algorithm to independently assign the codes to the states of each partition [6].

N. Chabini and W. Wolf reduced the power consumption by supplying the original supply voltage to the critical components while supplying a low voltage to the non critical components of the circuit. The authors changed the operating frequency of the critical and non critical components to a lower and higher value respectively so that the overall operating frequency remains unchanged [7].

Sagahyroon et al. presented an Integer Linear Programming technique to assign the codes to the states in the state diagram. Integer Linear Programming is a mathematical programming technique in which all the variables are restricted to be the integers. The algorithm includes designing the equations based on the required constraints and then solving the equations using the ILP solver [8].

Zhao et al. designed the structure of the D Flip-Flop using the transistors. The proposed structure used lesser number of clocked transistors as compared to the conventional structure. Power consumption was reduced due to the lesser number of clocked transistors in the proposed structure [9].

Jassani et al. Proposed Multi Objective Genetic Algorithm (MOGA) for the area and power reduction. The authors implemented the algorithm using C++ programming language. The proposed algorithm gives more than one result [10].

Yang et al. presented an algorithm for the state machine design for the area and power reduction. The algorithm was based on the concept of Relay race in which the present runner uses the experience of the past runner. Therefore, in the proposed algorithm, the present configurations were taken from the past configurations [11].

Liu et al. used the transistor architecture with the channel made of Silicon Nanowire to design the digital chips. The author designed the Ring Oscillator using the proposed architecture. The proposed architecture resulted in the reduced circuit delay and the power consumption [12].

R. S. Shelar divided all the sequential elements into different clusters. Each cluster was driven by a separate clock buffer. The algorithm was implemented using C++ programming language. The proposed algorithm reduced the power consumption of the clock distribution network [13].

Ravishankar et al. proposed an approach to reduce the switching activity of the digital systems. Switching activity was reduced by disabling the inputs which are not observable at a certain point of time [14].

Pozo et al. analyzed various low power design techniques used in the spacecraft *Rosetta*. They implemented the test bench using anti fuse Field Programmable Gate Array (FPGA). The authors concluded that the Clock Gating was the most important part in terms of power reduction. Another important technique was to completely shut down the redundant bus interface as long as the normal bus interface is working properly [15].

Shyu et al. reduced the power consumption by replacing individual single bit Flip-Flops with some multi bit Flip-Flops. The algorithm was implemented using C++ programming language [16].

Tang et al. proposed an architecture of Successive Approximation Analog to Digital Converter for the less power consumption. The proposed ADC was intended to be used in retinal replacement. The authors reduced the power consumption by reducing the voltage supply to the internal Digital to Analog Converter [17].

Leuders et al. discussed some techniques for the low power design which includes implementing Enable/Disable function to the Low Drop Out (LDO) regulator, using different LDO regulators for different load conditions and implementing the efficient switching techniques for the state transitions [18].

A. Sanyal and N. Sun reduced the switching energy in the Successive Approximation Analog to Digital converter. Switching energy was reduced by the reduction in the number of capacitors in the design. The switching activity has less dependence on the frequency in the proposed design [19].

D. Kidd used Deeply Depleted Channel transistor for the power reduction. An adaptive body bias method was proposed using DDC transistor to correct the manufacturing variation in terms of power consumption [20].

Jana et al. conserved the energy used while clocking or switching in the digital system. Inductor was used to store the switching energy. This stored energy can easily be transferred to an external resonant circuit [21].

III. CONCLUSION

Different techniques presented by the authors to reduce the Power Consumption include changing the hardware architecture to get the power efficient components, reducing the switching activity between the codes of the states, activating only the critical parts of the system while making the other parts idle and conserving the power used while switching the states.

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BIOGRAPHIES

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