

## DESIGN OF HIGHER ORDER PHASE LOCKED LOOP

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**Abstract** - A phase-locked loop (PLL) is a closed-loop feedback control system, which synchronizes its output signal in frequency as well as in phase with an input signal. The phase detector, the loop filter, and the voltage controlled oscillator are the key parts of almost all PLLs. The phase-locked loops (PLLs) are probably the most widely used synchronization technique in grid-connected applications. A basic approach to improve the performance of phase-locked loop (PLL) under adverse grid condition is to incorporate a first-order low-pass filter (LPF) into its control loop. The first-order LPF, however, has a limited ability to suppress grid disturbances. Normally the loop filter is designed to match the characteristics required by the application of the PLL. If the PLL is to acquire and track a signal the bandwidth of the loop filter will be greater than if it expects a fixed input frequency. The pure digital phase locked loop is attractive because it is less sensitive to noise and operating conditions than its analog counterpart. A PLL is a nonlinear feedback control system that tracks the phase and frequency of the input signal fundamental component and is able to re track the phase, with no steady-state error, following a transient event such as phase and frequency jumps.

**Key Words:** Phase-locked loop, Low pass filter, Synchronization.

### 1. Phase Locked Loop

Phase-locked loops (PLLs) are a widely needed and used circuitry in today's semiconductor chips. They are mainly used for three different tasks: Generation of high frequency on-chip clocks by frequency multiplication, Reduction of clock skew and Jitter attenuation. A PLL is characterized by the frequency range, jitter, jitter attenuation and lock time. PLLs are only used for generation of high frequency stable clocks and are normally feed by quartz controlled oscillators so that there is no need for a jitter attenuation. The phase-locked Loops (PLLs) are probably the most widely used synchronization technique in grid-connected applications. The key feature of open-loop synchronization techniques

is that they are un- conditionally stable. They typically yield a satisfactory performance in terms of the phase or frequency detection accuracy when the grid frequency is at, or close to, its nominal value; however, their performance tends to worsen when the input frequency deviates from its nominal value. To overcome this problem, incorporating frequency estimation or control algorithms into the open-loop schemes have been proposed. The main challenge that is associated with the PLLs is how to precisely and fast estimate the phase and frequency, when the grid voltage is unbalanced and/or distorted. To overcome this challenge, incorporating moving average filter(s) (MAF) into the PLL structure has been proposed in some recent literature. An MAF is a linear-phase finite-impulse-response filter, which can act as an ideal low-pass filter, if certain conditions hold. The main aim of this paper is to present the control design guidelines for a typical MAF-based PLL.

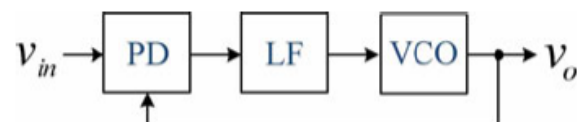


Fig -1: Basic PLL Structure

Fig- 1 shows the basic structure of PLL. Among the various synchronization techniques, PLLs have found much attention, mainly due to their simplicity, robustness, and effectiveness. A PLL is a closed-loop feedback control system, which synchronizes its output signal in frequency, as well as in phase, with an input signal. With the advanced technology of microcontrollers and digital signal processors (DSPs), all of the functions of the classical PLL have been implemented by software. The components are:

#### 1.1 Phase and Frequency Detector

The first component in PLL is the phase and frequency detector. The output of the PFD depends on both the phase and frequency of the inputs. This type of phase detector is also termed a sequential phase detector. It compares the leading edges of data and data1 (data is the input signal to PFD, data1 is considered as the feedback signal from the output of VCO to PFD). A data1 rising edge cannot be present without a data rising edge. If the rising edge of the data leads the data1 rising edge, the up output of the phase detector goes high while the down output remains

low. This causes the data1 frequency to increase and makes the edges move closer. If the data1 signal leads the Data up remains low while the down goes high. And we can find the phase difference between data1 and data.

### 1.2 Loop Filter

The second component in PLL is the loop filter. The loop filter consists of two parts, the charge pump and the RC-filter. The output of the PFD should be combined into a single output to drive the loop filter. In charge pump, two NMOS and two PMOS are connected serially. The uppermost PMOS and lowermost NMOS are considered as the current source and the other PMOS and NMOS in the middle are connected to the up and down of the output of PFD. When the PFD up signal goes high, the PMOS will turn on. This will connect the current source to the loop filter. It is in the similar way when the PFD down signal goes high. The loop filter is a simple RC filter. However, it plays a very important role in the PLL. Unless the loop filter values are correctly chosen, it would take the loop too long to lock or once locked it is still unstable small variations in the input data may cause the loop unlock again. If the rising edge of data leads that of data11, the PFD up goes high. And it will cause the voltage of the output signal of the loop filter become higher. If the rising edge of data lags that of data1, the PFD down goes high. It would cause output signal of the loop filter become lower.

### 1.3 Voltage Controlled Oscillator

In the voltage controlled oscillator (VCO), the main part is the multiple stage oscillator which is similar to the ring oscillator. In each stage, there are two PMOS and two NMOS. The upper most PMOS and lower most NMOS operate as current source and the PMOS and NMOS in the middle operate as inverter. The current sources limit the current available to the inverter. Compared with the resistance and capacitance present in the loop filter, the resistance of the VCO should be designed infinite and the capacitance of the VCO should be designed smaller. Fig- 2 shows the standard structure of PLL.

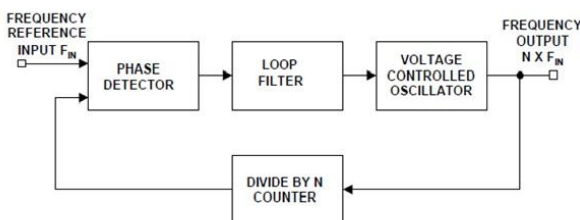


Fig -2: Standard PLL Structure

The input to the VCO is the output signal of loop filter. When the voltage of the input signal to VCO is high, the frequency of output signal in VCO becomes larger and larger. The output of loop filter is given to the input of VCO. On the contrary, when the voltage of the input signal

to VCO is low, the frequency of output signal in VCO becomes smaller and smaller. This is reasonable. For example, if the voltage of the input signal to VCO becomes high, that means the rising edge of data leads that of data1. That is the reason why we need to make the frequency of the output signal of VCO larger to catch up with the reference (input) signal.

### 2. Model Order Reduction

According to the small signal model in fig- 3. The PLL under study is of order  $n + 2$  ( $n$  is the LPF order). In what follows it is shown that regardless of the LPF order, the PLL Department of model can be approximated by a third-order model. This model order reduction simplifies the analysis and design of PLL. The key to determine the reduced-order model lies in the fact that the in-loop LPF causes phase delay in the PLL control loop, so to ensure the PLL stability its crossover frequency must be sufficiently lower than the LPF cutoff frequency.

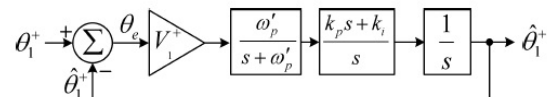


Fig -3: Reduced Order Small Signal Model

The higher the LPF order, the greater the low frequency phase delay is, and therefore the smaller the PLL crossover frequency (compared to the LPF cutoff frequency) should be. According to this fact, the reduced-order model can be obtained by neglecting the high frequency dynamics of LPF and approximating its transfer function with a first-order transfer function in Fig- 3. This model is accurate at low frequency range. Therefore, it can only be used to study the stability and dynamic behavior of PLL.

### 3. PLL Structure and Small Signal Modeling

Fig- 4 shows the schematic diagram of PLL under study, which is a standard three phase PLL with an in-loop LPF. In this structure, the PI controller acts as the main filter of Control loop as it is responsible to provide a zero steady-state average phase-error for the PLL. The LPF, on the other hand, supports the PI controller as it is responsible to improve the disturbance rejection capability of control loop under adverse grid condition. The performance of PLL under distorted grid condition is to include a simple first order low pass filter (LPF) inside its control loop.

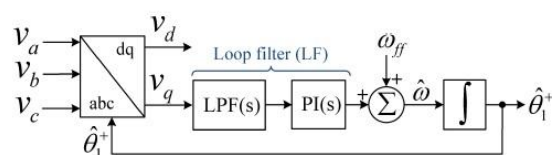


Fig -4: Structure of PLL under Study

A first-order LPF, however, has a limited ability to suppress the grid disturbances. To further improve the disturbance rejection capability of PLL, using higher order LPFs are sometimes recommended. For example, using a fourth order LPF in the PLL control loop is suggested in. Application of these high order LPFs, however, results in high order PLLs.

#### 4. All Digital Phase Locked Loop

An all digital phase locked loop was implemented, in 0.25 micron CMOS technology, by understanding the analog phase locked loop concepts and the digital conversion required to maintain the same functionality. The all digital phase locked loop achieves locking within about 100 reference clock cycles. The pure digital phase locked loop is attractive because it is less sensitive to noise and operating conditions than its analog counterpart. Many circuits currently face the problem of clock skew, and registers and flip-flops are not receiving the clock at the exact same time. The clocks are generated by oscillators, but the clocks that reach the registers and flip-flops are distorted and require a phase locked loop to address this problem.

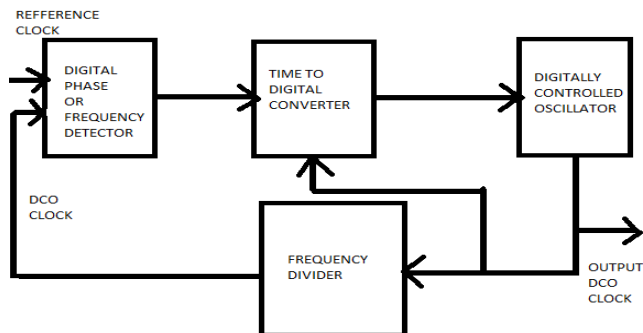


Fig -5: ADPLL Block Diagram

A phase locked loop ensures that the clock frequencies seen at the clock inputs of various registers and flip-flops match the frequency generated by the oscillator. The phase locked loop (PLL) is a very important and common part of high performance microprocessors. Traditionally, a PLL is made to function as an analog building block, but integrating an analog PLL on a digital chip is difficult. Analog PLLs are also more susceptible to noise and process variations. Digital PLLs allow a faster lock time to be achieved and are attractive for clock generation on high performance microprocessors. The all digital phase locked loop was designed such that it is composed of four main components. The components are analogous to the analog PLL, but the implementation consists of digital components. A digitally controlled oscillator (DCO) was utilized instead of a voltage controlled oscillator. A high level block diagram of the implementation is shown in Fig-5. The phase frequency detector (PFD) detects the phase

and frequency mismatch of the reference clock and divided DCO clock. The PLL is locked when the PFD detects that the phase and frequency of the two clock inputs match. The output of the PFD drives the time to digital converter. The PFD produces up and down enable signals that are interfaced to the digital converter. The digital converter takes these inputs and increases or decreases the control word which is fed to the thermometric decoder. This decoder is essential for controlling the DCO. The DCO clock is divided by a specific multiplication factor, in our case it is four, and sent back to the PFD for phase and frequency comparison.

#### 5. Linear Phase Locked Loop

Linear PLL is also in s domain. The phase error is small in linear PLL. A PLL can be accurately described by a linear model. So it is known as linear PLL. Fig- 6 shows the linear PLL model.

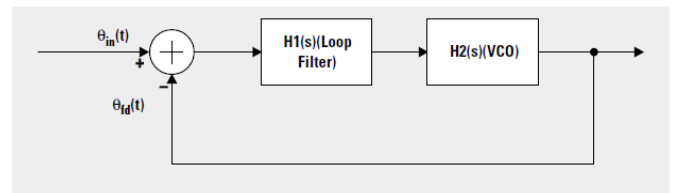


Fig -6: Linear PLL Model

The phase of the input signal, the phase of the feedback signal is shown in fig- 6. Since the system is described in the continuous-time domain. So far, all the modeling shown is in the continuous-time domain. This model can be applied directly to an analog PLL. One mandatory requirement for designing linear PLLs is that the linear PLL system must be stable. Basically, the stable condition of a discrete-time system occurs when the roots of the characteristic equation are inside the unit circle in the Z-plane. Normally, after a system is implemented, numerical Coefficient can be substituted into the characteristic equation. By solving the characteristic equation numerically, the positions of the poles can be found to determine if the system is stable; however, this method is technically difficult to use when implementing a linear PLL since numerical coefficients will not be available at the beginning of the process.

#### 6. CONCLUSIONS

PLL is a closed-loop feedback control system that synchronizes its output signal in frequency as well as in phase with an input signal. Phase Locked Loops (PLL) circuits are used for frequency control. They can be configured as frequency multipliers, demodulators, tracking generators or clock recovery circuits. Each of these applications demands different characteristics but they all use the same basic circuit concept. The phase locked loop (PLL) is a very important and common part of

high performance microprocessors. Traditionally a PLL is made to function as an analog building block, but integrating an analog PLL on a digital chip is difficult. Analog PLLs are also more susceptible to noise and process variations. Digital PLLs allow a faster lock time to be achieved and are attractive for clock generation on high Performance microprocessor. On concerning the future work the phase locked loop (PLL) has been widely used in Wireless communication systems due to the high frequency resolution and the short locking time. The usage of Direct Digital Synthesis (DDS) avoids some of the typical tradeoffs in PLL like the achievement of a very high-frequency resolution together with fast settling and spectral purity. As a part of the future work, the present work can be extended with a DDS-based PLL architecture.

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## BIOGRAPHIES



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