DESIGN OF HIGH SPEED MODIFIED-GDI BASED CARRY SELECT ADDER

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Abstract - *Addition is an inevitable operation for any high speed digital system, digital signal processing system. The primary issues in the design of adder cell are area, delay and power dissipation. Optimization of several devices for speed and power is a significant issue in low-voltage and low-power applications. In the proposed adder, the carry select (CS) operation is scheduled before the calculation of final-sum, which is different from the existing approach. An efficient CSLA design is obtained using optimized logic units. The proposed CSLA design involves significantly less area and delay than the recently proposed BEC-based CSLA. Due to the small carry-output delay, the proposed CSLA design is a good approach for square-root (SQRT) CSLA. These issues can be overcome by incorporating Gated Diffusion Input (GDI) technique. Modified GDI is a novel technique which is extension of GDI (gate diffusion input) technique for low power digital circuits design further to reduce the swing degradation problem. This paper presents logic style comparisons based on different logic functions and claimed modified Gate Diffusion Input logic (Mod-GDI) to be much more power-efficient than Gate Diffusion Input logic (GDI) and complementary CMOS logic design. This techniques allows reduction in power consumption, carry propagation delay and transistor count of the carry select adder. This technique can be used to reduce the number of transistors compared to existing SQRT CSLA, which gives that the usage of carry strength signals allows high-speed adders to be realized at lower cost as well as consuming less power than previous designs. Hence, the proposed architecture mainly concentrating on the area delay product (ADP) using modified GDI logic.*

Key Words: High-speed adders, Modified GDI, ADP Product, and Low-Power design etc…

1. INTRODUCTION

Most of the VLSI applications, such as digital signal processing, image and video processing, and microprocessors, extensively use arithmetic operations. Addition, subtraction, multiplication, and multiply and accumulate (MAC) are examples of the most commonly used operations. All complex and simple digital multiplication is based on addition. An area efficient, fast and accurate operation of a digital system is largely depends on the performance of the basic adders cells. Adders are very important component in digital system design because of their wide usage in these systems. Hence, to design a better architecture the basic adder blocks must have reduced delay, power consumption and area efficient architectures. The demand is of DSP style systems for both less delay time and less area requirement for designing the systems.

The CSLA is used in many computational systems to relieve the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) configuration to generate partial sum and carry by considering carry input Cin=0 and Cin=1, then the final sum and carry are generated by the multiplexers (mux) based on selection lines. To overcome this problem BEC based CSLA was proposed. This architecture uses Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption. The main advantage of this BEC logic is it uses less number of logic resources than the regular CSLA structure. Since it uses one RCA propagation delay is more.

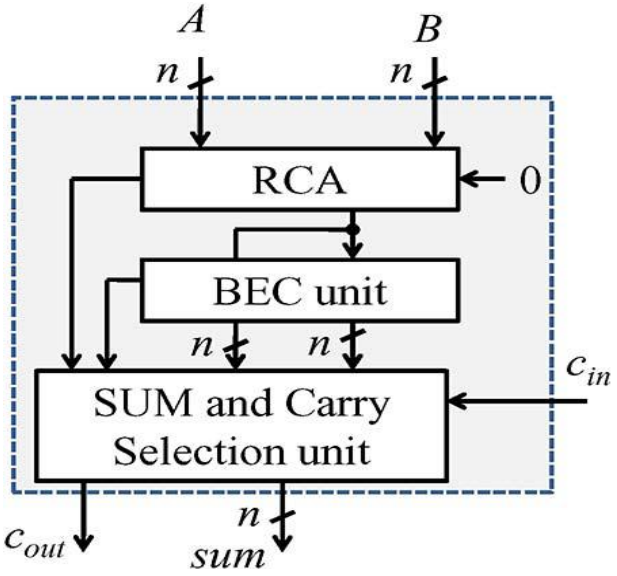


Fig -1: BEC based CSLA

Even though Adders using different implementations to achieve required performance, due to presence of RCA logic propagation delay is the major concern while designing more number of transistors fabricated on a single chip. Modified gate diffusion input (Mod-GDI) technique which is used to achieve area delay power (ADP) product significantly. Diffusion Input (GDI) is an advanced technique for low power digital design .This technique can be used to reduce power consumption, delay and number of transistors compared to Conventional CMOS design with better output logic swing. The standard CMOS and several different techniques for circuit design are compared with Modified GDI technique.

2. PROPOSED GDI BASED CSLA

The BEC-based CSLA involves less logic resources than the conventional CSLA due to eliminating redundant logic operations, but it has marginally higher delay. A CSLA based on common Boolean logic (CBL) is also proposed. The CBL-based CSLA of involves significantly less logic resource than the conventional CSLA but it has longer Carry Propagation Delay, which is almost equal to that of the RCA. To overcome this problem, a SQRT-CSLA based on Common Boolean Logic. However, the CBL-based SQRT- CSLA architecture requires more logic resource and delay than the BEC-based SQRT-CSLA. We observe that optimization of logic largely depends on availability of redundant operations in the formulation, whereas adders delay mainly depends on data dependence. In the existing designs, logic is optimized without giving any importance to the data dependence. In this brief, we made an analysis on logic operations involved in BEC-based CSLA to study the data dependence and to identify redundant logic operations. Based on this analysis, we have proposed a logic formulation for the CSLA. The main involvements in this brief are logic formulation based on data dependence and optimized carry generator (CG) and CS design. Based on the proposed logic formulation based CSLA, we have derived an efficient logic design for CSLA. Due to optimized logic units of CS and CG units, the proposed CSLA involves significantly less ADP product than the existing CSLAs.

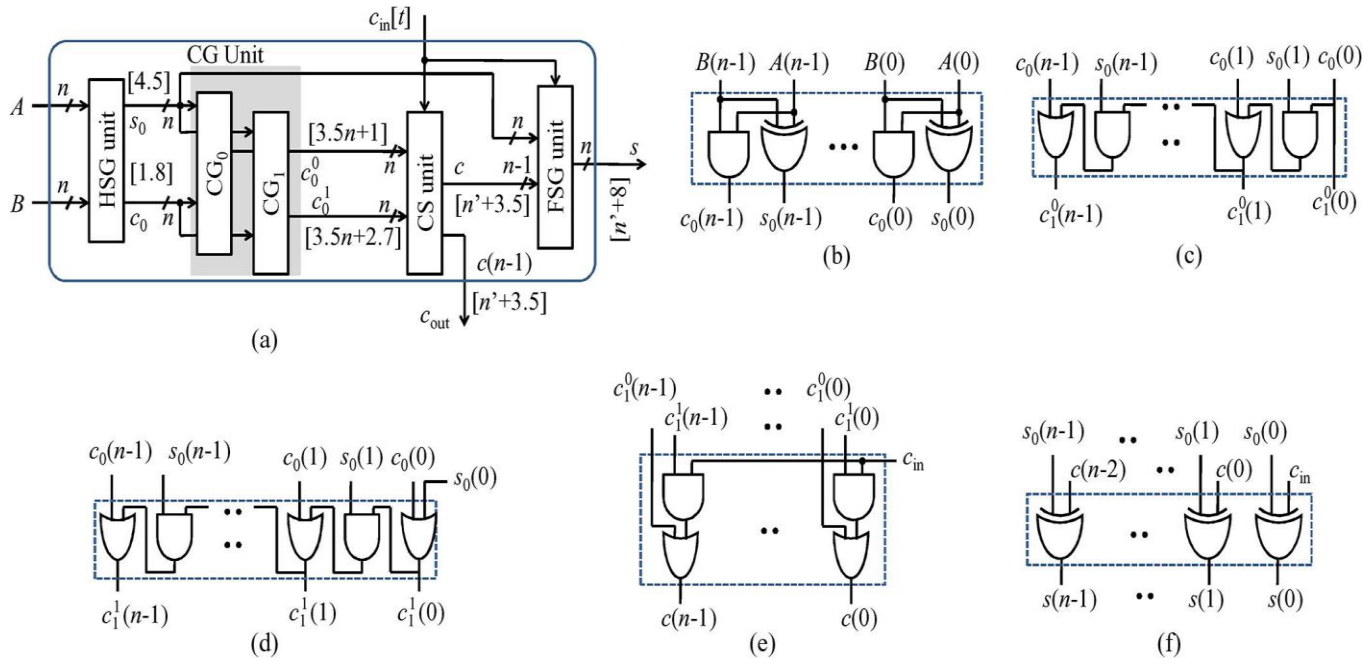


Fig -2: (a) existing CS adder design, where *n* is the input operand bit-width. (b) Gate-level design of the HSG. (c) Gate-level optimized design of (CG0) for input-carry = 0. (d) Gate-level optimized design of (CG1) for input-carry = 1. (e) Gate-level design of the CS unit. (f) Gate-level design of the final-sum generation (FSG) unit.

2.1 Basic GDI Cell

The basic GDI cell reminds one of the standard CMOS inverter, but there are some important differences. 1) The GDI cell contains three inputs: G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS). 2) Bulks of both nMOS and pMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter. The GDI cell structure is different from the existing PTL techniques. It must be remarked that not all of the functions are possible in standard p-well CMOS process but can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies.

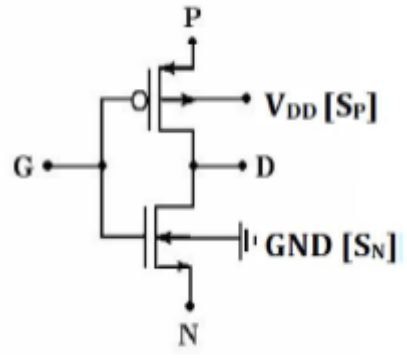


Fig -3: Basic GDI cell

Power dissipation becomes most important consideration in high performance applications. Optimizations for basic logic gates are fundamental constraint in order to get better the performance of a variety of low power and high performance devices. A high-speed and multipurpose logic style for low power electronics design are known as Gate Diffusion Input (GDI), with reduced area and power requirements, and ease of implementing a wide variety of logic functions. But this basic Gate Diffusion Input (GDI) logic style suffers from some practical limitations like swing degradation, fabrication complexity in standard CMOS process and bulk connections. These limitations can be overcome by modified gate diffusion input (Mod-GDI) logic.

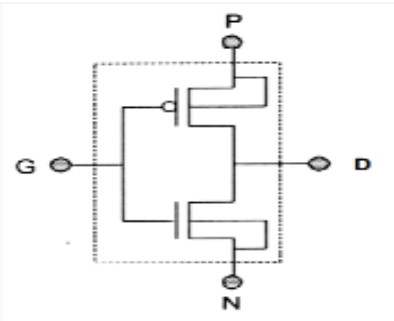


Fig-4: Modified GDI Cell

Comparison made with basic GDI cell, Modified GDI cell consist,

i. A low voltage terminal (SP) configured to be connected to high constant voltage
ii. A high voltage terminal (SN) configured to be connected to ground.

Including terminals, we can ensure that the Mod-GDI cell can be implemented with all current CMOS technologies. In Mod-GDI cell, the bulk node of all PMOS transistors are connected to VDD and bulk node of all NMOS transistors are connected to GND. Mod-GDI cell uses standard 4 terminal NMOS and PMOS transistors and it provides ease of implementation in all type of standard CMOS technology. Table-1 represents the various logic functions which can be implemented with help of MOD-GDI cell for different input configuration. This arrangement of modified GDI cell provides reduction in both sub-threshold and leakage power compared to static CMOS gate. Mod-GDI is more suitable while designing of high speed, low power circuits by using reduced number of transistors as well as improved swing degradation and static power characteristics. The mod-GDI cell uses standard four-terminal NMOS and PMOS transistors and can be effortlessly implemented in all types of standard CMOS technology. The Mod-GDI cell be capable of as well implemented in all kinds of non-standard technologies twin-well CMOS technology, Silicon on Insulator (SOI) technology and Silicon on Sapphire (SOS) technology.

In Fig.-2, Logic gates can be replaced by Mod-GDI cell to achieve high speed efficient carry select adder with low power consumption and less layout area. Each logic gates in SQRT CSLA is replaced by modified GDI logic cells. Performance comparison also done with SQRT CSLA and Mod-GDI based CSLA.

3. OBSERVATIONS

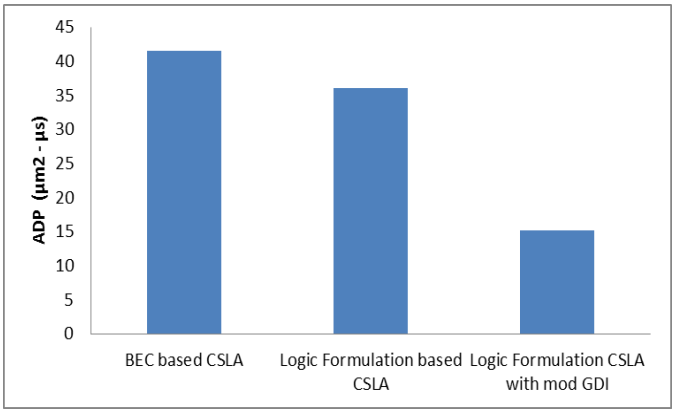
Table-1: Various logic Functions implemented with mod GDI cell

N	S_N	P	S_P	G	D	F UNCTIONS
0	0	1	1	A	A’	INVERTER
A	A	0	A	B	AB	A ND
1	0	A	D	B	A+B	OR
A’	0	A	1	B	A’B+AB’	X OR
A	0	A’	1	B	AB+A’B’	X NOR
0	0	B	B	A	A’B	F UNCTION 1
B	0	1	1	A	A’+B	F UNCTION 2
C	0	B	1	A	A’B+AC	MUX

Table-2: Performance Analysis Table for various 16bit-Carry Select Adder

S.NO	TYPE	DELAY (ns)	AREA (μm^2)	ADP (μm^2 - μs)
1	BEC based CSLA	16.204	2562.46	41.52
2	Logic Formulation CSLA	18.735	1923.82	36.04
3	Logic Formulation CSLA with mod GDI	10.426	1456.63	15.18

Chart-1: Performance Analysis Chart for various 16bit-Carry Select Adder



4. CONCLUSION

The new implementation of mod GDI is based on the logic formulation architecture, Mod-GDI gates lower the transistor count and in turn the silicon area required when compared to standard static CMOS and dynamic CMOS based designs. The sub threshold leakage power and tunneling leakage current of Mod-GDI gates is lower than the traditional CMOS logic styles. The problem of fabrication of GDI gates in standard nano-scale CMOS technology is overcome by connecting the sources of pMOS and nMOS to VDD and GND respectively, in Mod-GDI logic style. The mod GDI cell also improves swing degradation problem, which is the major problem in basic GDI cell. VDD and GND interconnect wires are not required because the Mod-GDI cell requires VDD and GND only to supply the body or bulks. This is in contrast to the majority previous implementations, which would still need VDD and GND to perform the operation. The comparison between our analysis and prior works shows that the mod GDI is one of this logic styles for low power digital design does provide many advantages. In short, the proposed Mod-GDI logic style based designs can be taken a better alternative in future.

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6. BIOGRAPHIES

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