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Power and Area Efficient ADC with Suitable Encoders and Comparators: A Review

M Jamal Azmi[1], S Akhtar Imam[2]

[1]*Sr. Assistant Professor, ECE Department, Indira Gandhi Delhi Technical University for Woman, India*
[2]*Associate Professor, ECE Department, Jamia Millia Islamia, India*

Abstract:- *Even though many electronic gadgets are operating with digital signals, but the signals in a real world are in the analog form. Thus, there is demand for a device which can convert the analog information into the digital form. Such a conversion is provided by an Analog to Digital converter (ADC). Thus, it can be inferred that an ADC acts as a conduit among a actual world and digital world. There are different kinds of ADC and they can be executed depending upon the size, speed and power requirement. So, while designing an ADC, the focus is on accuracy, area, power, and speed. Aforementioned prompted the examination of different ADC outline systems. In this paper, we introduced ADC with power and area efficient by using different types of encoders and different types of comparators.*

Key Words: *ADC, Flash ADC, Sigma-Delta ADC, SAR ADC, Dual Slop ADC*

1. INTRODUCTION

One of the important and fundamental blocks among all the electronic devices present in today's scenario for processing real world data is an Analog to Digital converter (ADC). For analysing and processing any analog signal using digital logic or the vice versa, we have to utilize a converter as the block through which we are going to begin any of the systems mainly concern with digital electronics. These converters are the essential blocks providing an interface between the real world and the electronic digital space[1]. Since converters are the essential block in mixed signal applications, sometimes the performance and speed in data processing becomes a bottleneck for the overall system. After the processing of converted data, we have to convert it again into its original form in order to make it compatible with the real world signals. Hence we can conclude that, data conversion devices shows dynamic role in modern systems [2].

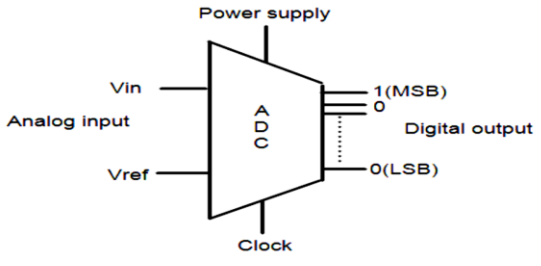


Fig -1: Block diagram of A/D converter

The basic operation of an ADC is depicted in figure-1, wherein an input analog voltage is getting converted into digital bits[3]. It works on the principle of conversion, i.e. whenever $V_{in}>V_{ref}$, it corresponds to a particular level of digital output and vice versa when $V_{in}<V_{ref}$. Where V_{in} is the input Analog signal and V_{ref} is the reference Analog signal used for the comparison [4].

2. ADC ARCHITECTURES

The different ADC architectures which are commonly used in various applications are as follows:

2.1. Flash ADC

It is also called as parallel ADC as the structure utilizes parallel combination of comparators. It is the speediest A/D converter among the various sorts and is apt for high transfer speed execution. We realize that power consumption and device size increases exponentially with resolution; hence it finds its application in low resolution circuits. It consists of 2^N resistor ladder due to which huge amount of power is consumed by the device. It also possesses lower resolution and accounts for higher cost for high resolution circuits [5]. It finds its application primarily in wide-band frequency devices and in alternate sorts of A/D converter models, i.e. making as sub-part of other ADC's. Multi bit ADC's like sigma-delta and pipelined use flash ADC's as their component [6]. Basically in high frequency applications flash ADC's are used such as radar discovery, optical communication, wideband radio receivers and satellite links. More frequently the flash converters are embedded in large integrated circuits containing numerous digital functions.

A flash ADCs' basic building blocks consist of reference generating circuits (typically it was resistors), comparator cluster block and an encoder converting thermometer codes to binary codes. The quantities of comparators required to change an analog voltage to N bits of digital signals are 2^N-1 comparators. We feed an analog signal as an input to all the comparators. This input signal in contrast with reference signal produces an output signal. As we increase the resolution, the quantity of resistors and the comparators required likewise increments exponentially [7]. The diagram of Flash ADC is demonstrated in figure- 2.1

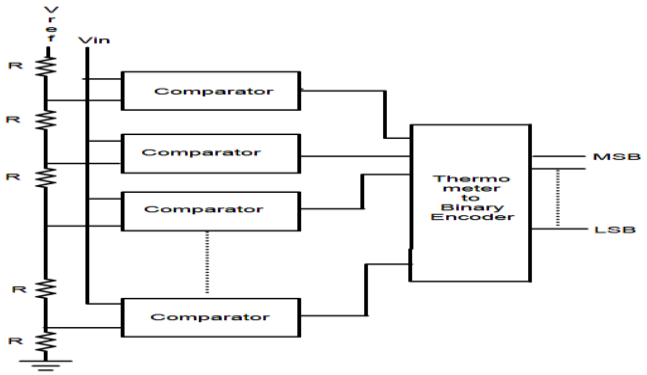


Fig- 2.1: Architecture of Flash ADC

2.2. Successive Approximation (SAR) ADC

When high resolution, high accuracy and low to medium speed applications are needed then SAR ADC's comes into action. Biomedical instruments, portable battery-powered instruments and sensors use such kind of ADC's. Due to its low power consumption property it is widely used in low power applications like digitizer pens, signal/data acquisition and industrial controls. The diagram of SAR ADC is demonstrated in figure 2.2

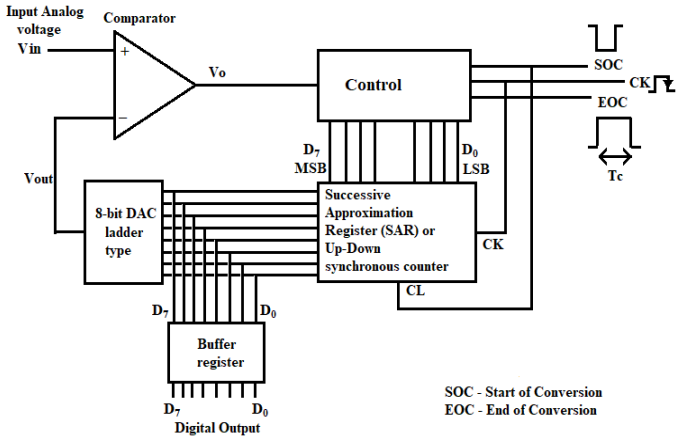


Fig-2.2: SAR ADC

The operation of SAR ADC is as follows:

1. The starting of conversion (SOC) goes low, counter is cleared and the digital output is 0000 0000.
2. At the same time the input Analog voltage is applied such that Vo goes high and the end of conversion (EOC) signal goes high and the conversion starts.
3. During the first clock pulse, the first control circuit loads a high MSB into the SAR whose output is then 1000 0000.
4. If $V_{out}>V_{in}$, the negative output of the comparator signals the control circuit to reset the MSB
5. If $V_{out}<V_{in}$, the positive output of the comparator indicates that the MSB is to remain set.
6. If $V_{out}=V_{in}$, the conversion is complete.
7. The next lower bits are then handled in the same way. This process is continued until the SAR tries all the bits.
8. When the conversion is complete, the control circuit sends a low signal i.e. $\overline{EOC}$.
9. At the falling edge of the EOC signal, the digital equivalent is loaded into the buffer register. Thus, the buffer register contains the digital output.

2.3. Sigma-Delta ADC

The basic architecture of ΣΔ A/C is illustrated in figure-2.3. The structure includes 1-bit Digital to Analog converter, a comparator, integrator and digital filter. Here, 1-bit DAC works as a switch and at high frequency, it will quantize the input signal whereas the digital decimator reduces the rate of sampling and increases the resolution of ADC. In this structure, difference of analog input signal and DAC's output is applied as an input to the integrator. The integrator will add the new value to the previous value it have. Then the output of integrator is passed to comparator. The comparator output will either be '1' or '0' which is then passed to the digital filter. The digital filter results in reduction of sampling rate and components of noise[8]. The sigma-delta ADC has an advantage over other ADC's in terms of accuracy and cost. But, they are complex in design and it is the slowest ADC among all other ADC's. They are widely used in high precision, high resolution applications.

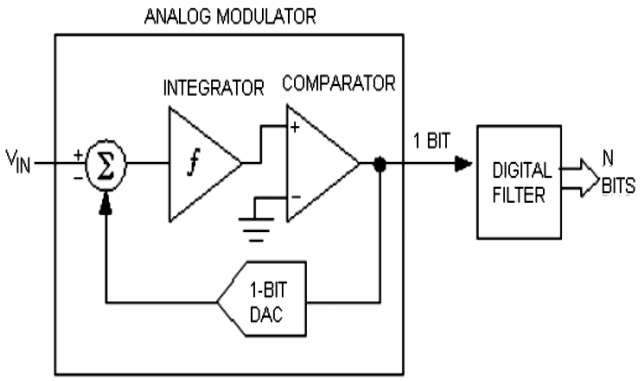


Fig -2.3: Sigma-delta ADC

2.4 Dual Slope ADC

The dual slope ADC has the slowest conversion time but has the advantage of low cost as it does not require precision components, i.e. DAC or VCO. The basic operation of dual slope ADC involves the charging and discharging of capacitor C linearly using constant currents. Firstly, the analog input signal is fed to the integrator and capacitor starts charging. As the input is applied to the inverted terminal of the integrator, the output voltage is negative in magnitude. Now, the integrator's output is passed to the comparator, resulting in high V_c. Thus the enabling logic gate and clock pulses reach the CLK terminal of the counter. The counter was initially cleared and it starts counting when 2^N-1 clock

pulses are applied. When the next clock pulse arrives i.e. 2^N, the counter is reset, and the flip flop output is set to one.

As the result, value of the switch is controlled by the output of flip flop. Now switch moves to reference voltage, V_r. Consequently, the output of integrator starts to move in a positive direction. The counting process continued until $V_0<0$. When V_0 goes positive, V_c goes low which disables the AND gate and thereby, the counter stops counting. It is the slowest but most accurate ADC. It is often used in digital voltmeters because of its conversion accuracy and low cost. The diagram of dual slop ADC is demonstrated in figure-2.4

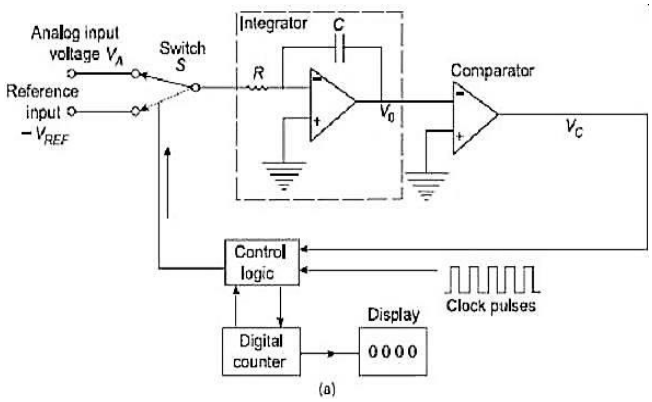


Fig-2.4: Circuit diagram of dual slope ADC

3. ADC CHARACTERISTICS

An A/D converter is used to convert the wide range of input values into discrete form. Generally the analog signals have wide range of values and selecting a specific number of input values from this wide range is quite challenging. Consequently, there will be some data loss while picking a specific input values and an error will be introduced. In ADC, the quantisation and encoding processes are done simultaneously. The process of converting the infinite input values into digital form is called quantisation. 2^N is the number of quantization level for an N-bit A/D converter. Figure-3 demonstrates the transfer function of a perfect ADC. The digital outputs are marked on y-axis whereas the input analog signals are marked on x-axis. The transfer function of A/D converter is commonly called as staircase curve.

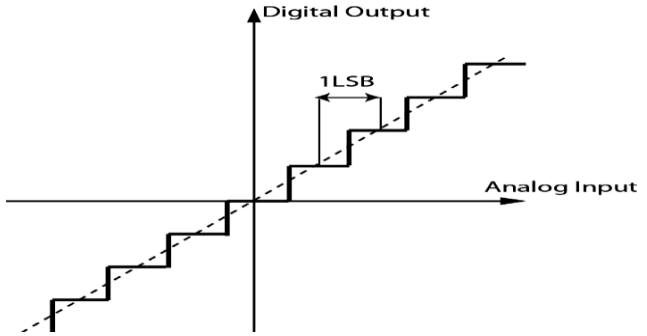


Fig -3: Transfer function of an ideal ADC

Here, least significant bit (LSB) is the smallest level of quantization that an A/D converter can resolve and it is given by:

$$LSB = \frac{V_r}{2^N} \quad (1)$$

Where V_r is the reference voltage and 2^N is the number of different levels.

4. ANALOG TO DIGITAL CONVERSION ERRORS

In ADC conversion the following main types of errors occur.

4.1. Quantization error

It happens because of the change of analog signal into digital signal. It can be defined as the variation between the ideal values and the measured value.

$Q_{error} = V_i - V_{staircase}$

Figure-4.1, depicts the quantization error of ideal N-bit A/D converter. The error signal i.e. The difference between analog voltage and quantized output voltage is represented by a sawtooth waveform. The conversion has a maximum error of $\pm\frac{1}{2}\ LSB$.

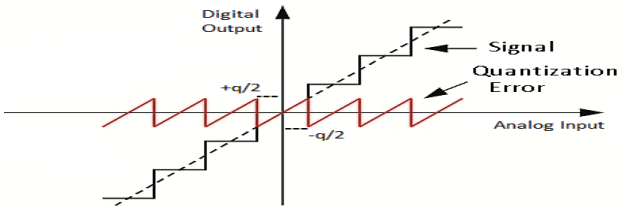


Fig-4.1: Representation of Quantisation error

4.2. Offset and Gain error

A fixed difference between the transfer function of ideal ADC and a shifted ADC is called offset error. A shift in the transfer function of ADC is due to mismatching of device or other non-idealities of the components of ADC. Using some appropriate design methodologies, offset error can be overcome and in such case, quantisation error becomes ideal. ADC offset error is shown in figure-4.2(a).

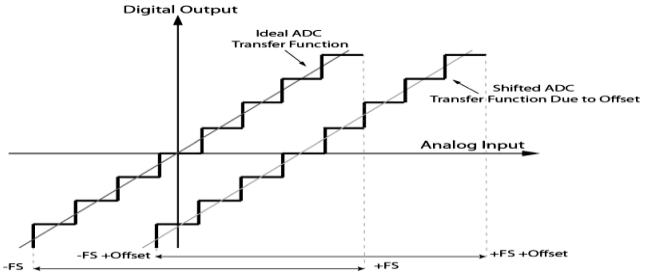


Fig -4.2(a): ADC Offset error

Gain error occurs if there is variation in the slope of actual ADC transfer function and ideal ADC transfer function. This generally happens when an on-chip reference is used. In ideal ADC, conversion output results in all '1' on the application of full-scale input. In an ADC with gain error, the conversion output will be '1' when applied voltage is higher than full-scale (negative gain error) or less than full-scale (positive gain error). Fig 4.2(b) illustrates the transfer function of ADC with gain error.

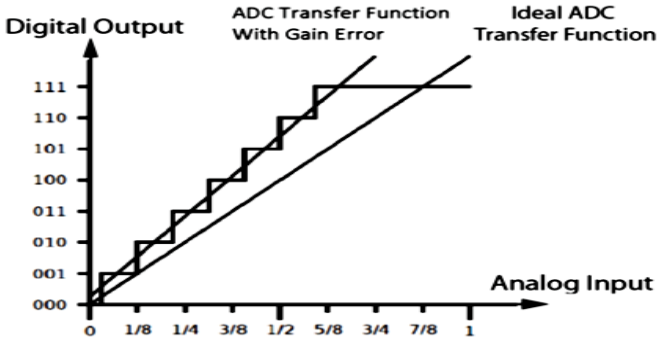


Fig-4.2(b): Transfer function of ADC with Gain Error

4.3 Non-linearity error

Differential non-linearity (DNL) and integral non-linearity (INL) are the two important parameters for testing the performance of ADC.

Differential non-linearity (DNL) depicts the variation in the step width of real ADC transfer curve from the ideal ADC transfer curve where 1LSB is the step width of ideal ADC transfer curve. Figure-4.3 illustrates the differential non linearity. In other words, the output of ideal ADC transfer function is divided into 2^N uniform voltage levels with a step size equal to 1LSB. Any difference from ideal step size leads to an error called differential non-linearity (DNL). For an ideal ADC, DNL is 0LSB. Practically, DNL comes from the ADC used. For instance, in a successive approximation A/D converter, differential non-linearity error might occur close to the middle range because of mismatching of its Digital to Analog converter.

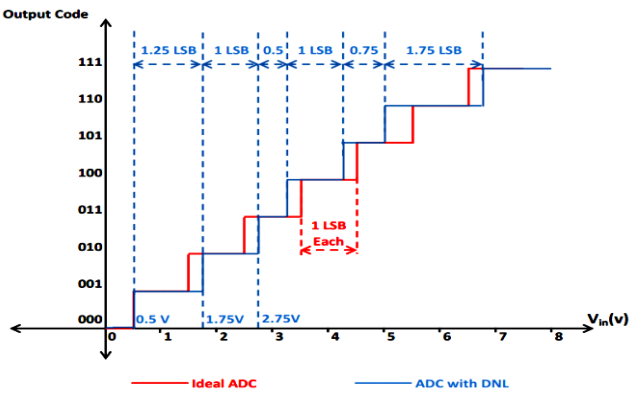


Fig -4.3: DNL representation in an ADC transfer curve

The maximum deviation between transfer function of actual ADC and ideal ADC is referred as Integral non linearity (INL). In the other words INL tell us how exactly the output of ADC matches with characteristics of ideal ADC. Integral non-linearity can be described as the difference of LSB between the ideal and actual ADC's transfer function. In actuality, integral non linearity is estimated by mapping the transfer curve of ADC as described under.

There are two strategies to discover the integral non-linearity error,

1. Best straight line technique

2. End point technique

4.3.1 Best straight line Technique:

In this scheme of INL measurement, gain and offset error are considered. One can look in figure-4.3.1, that for calculating best straight line, the transfer curve for an ideal ADC does not start from an origin. Here, the transfer curve of an ideal ADC is drawn such that it describes the nearest first-order approximation to the real transfer curve of the ADC. The slope plus intercept of this perfect bend can give us the estimation of the gain and offset error of the A/D converter. Instinctively, the best fit line technique produces better outcomes for integral non-linearity.

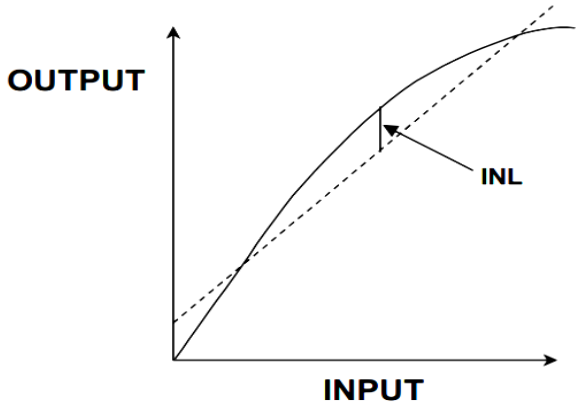


Fig-4.3.1: Best straight line method

4.3.2. End-point INL:

The End-Point technique gives the most pessimistic scenario of integral non-linearity. This estimation passes the straight line through the starting point and maximum output code of the A/D converters. For DC applications, it is more valuable to utilize this strategy when contrasted with the one evaluated utilizing best fit method. This method must be used for applications concerning precise measurements and control. The End-point INL is demonstrated in figure-4.3.2.

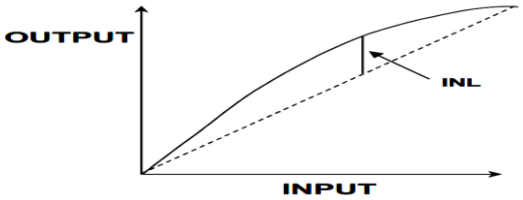


Fig-4.3.2: End Point INL

4.4.Noise error

The electronic circuitry mainly generates noise error. The electronic hardware is regularly the primary cause of noise signals. The performances of Analog to Digital converters are profoundly influenced by the noise signals. Jitter and thermal noise are typical in electronic devices. The blemishes in the clock signal cause the jitter to occur. In other words, the clock edges will constantly shows some variety from the required esteem. At the time of sampling, this blemish in the clock signal leads to a problematic situation. So jitter is as yet a huge issue in Analog to Digital converters. Thermal noise is because of the irregular movement of electrons in conductors. Hence this noise will be available in wide range of electronic gadgets. On account of ADCs, it will influence the effective resolution.

5. TIQ BASED FLASH ADC

A conventional N-bit flash A/D converter uses the resistive ladder network for generating the reference voltage but it results in large die area and high power consumption. In order to overcome these problems, threshold inverting quantization (TIQ) comparators are used which can produce the reference voltages internally. Figure-5 illustrates the TIQ based flash ADC block diagram. It comprises Threshold inverter quantization (TIQ) comparators and an encoder[9]. The TIQ comparator compares input signals with the internally generated reference voltage which depend upon the transistor sizes of the inverters and produces a thermometer code[10]. Through an appropriated encoder, the conversion of these thermometer codes into binary codes takes place. The elimination of a resistive ladder leads to faster conversion speed of flash ADC with the additional advantage of power consumption reduction. Thus can be inferred that TIQ based flash ADC is beneficial for the low power and high speed applications.

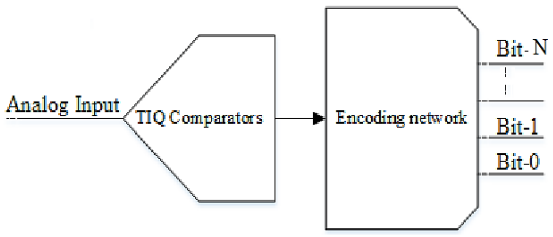


Fig-5: TIQ Flash ADC block diagram

6. THERMOMETER TO BINARY CODE ENCODER

The transformation of thermometer code to binary code is measured as a bottleneck in the design of fast and low resolution flash A/D converter. Since, digital back end of the flash A/D converter can affect the overall power consumption of the device so it must be designed appropriately. Many researchers came up with new and better ideas for encoder designing. Among numerous strategies, direct transformation into binary code using 2:1 multiplexer and conversion of thermometer to binary code via gray-code circuit are the most recent ones[11].

Apart from these two, some other encoder architecture available in the literature are ROM based encoder, Wallace tree encoder and fat tree encoder. In this paper, a new structure is proposed which helps in reducing the overall power consumption of device. For the designing of the encoder's components, the GDI technique gives a better outcome on the basis of the area and the power consumption among every architectures available.

The Multiplexer is designed using full swing GDI technique which is in contrast with the other 3 methods utilizing CADENCE VIRTUOSO. The circuit has been designed in 90nm CMOS technology operating at 1 V power supply. Firstly, GDI technique is used in each existing encoder and compared with the other conventional techniques used to design an encoder. Then, a new architecture is proposed using this technique.

6.1 Types of Thermometer to Binary code Encoders

The various types of encoder to convert thermometer to binary code are explained below:

6.1.1 ROM (Read only memory) based encoder

Earlier, Read only memory based encoding scheme is considered to be most adopted structure used for flash ADC. The different kinds of ROM based encoder are the Gray-ROM encoder and Binary-ROM encoder.

Figure- 6.1.1, demonstrates the architecture of flash A/D converter using Binary-ROM encoder. The encoder comprises of two fragments, the 1-of-N circuit and the read only memory structure.

Firstly, the one out of N circuit takes the input as thermometer code and then its output is delivered to the ROM structure which selects the appropriate row in the ROM on the basis of the input. The 1-of-N circuit consist of array having one input inverted showing AND gate and its function in thermometer code is to identify the one to zero change happened.

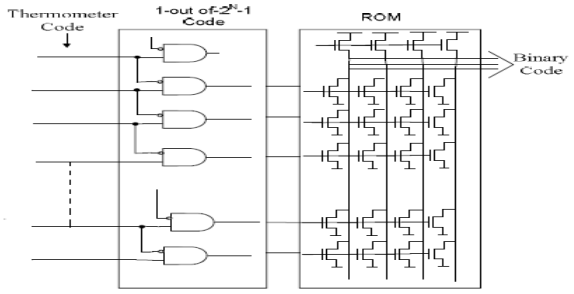


Fig-6.1.1: Encoder which is based on ROM

The Encoder which is based on ROM has an advantage of its design simplicity. However, power consumption is high and the conversion speed is comparatively slow. Another issue with Binary-ROM encoder is the bubble error.

The problem of bubble error might be resolved through Gray-ROM encoder [12]. More than one number of '1's will appear in the output waveform of 1-of-N encoder, if any kind of bubble error is present in the circuit. Resulting in which more than one number of lines of the given encoder gets enabled; this leads to the binary code output having any kind of error. One probable key to this issue is to implement a 3-input AND gate to suppress the bubble, but again it is capable of dealing with only separated one bubble. If one wishes to obtain an advanced bubble (e.g.10001110), they need to add more number of input pins at AND gate to suppress the bubbles present and hence putting pressure on increased power consumption and dice area. Another possible way is to use NAND gate in place of AND gate with one of the input as inverted and use a clock signal in ROM encoder for controlling the leakage etc.

6.1.2 Wallace tree encoder

The Wallace tree encoder is a best way to deal with thermometer to binary code conversion. It has an inbuilt bubble error suppression property where as other encoders requires a bubble correction circuit. The architecture of Wallace tree encoder is demonstrated in figure-6.1.2. The primary function of Wallace tree encoder is to count the number of ones and this function performs via full adder. It is also known as 'Ones counter'. But this encoder has a disadvantage as the structure is designed using full adder which itself contains numerous transistors. So the structure consumes large power and the delay also increases.

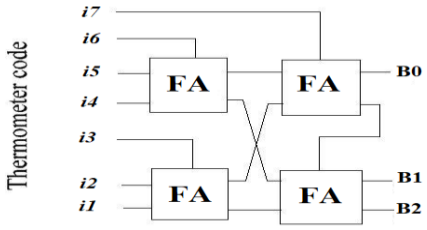


Fig-6.1.2: Circuit diagram of Wallace tree encoder

6.1.3 Fat-tree encoder

The architecture of fat tree encoder is shown in fig 6.1.3. It's working is similar to the ROM based encoder where stage-1 converts the thermometer code into 1 out of N code and then the stage-2 converts the 1 out of N code into binary code. The fat tree encoder occupies small chip area and has less delay as compared to wallace tree and ROM based encoder [13].

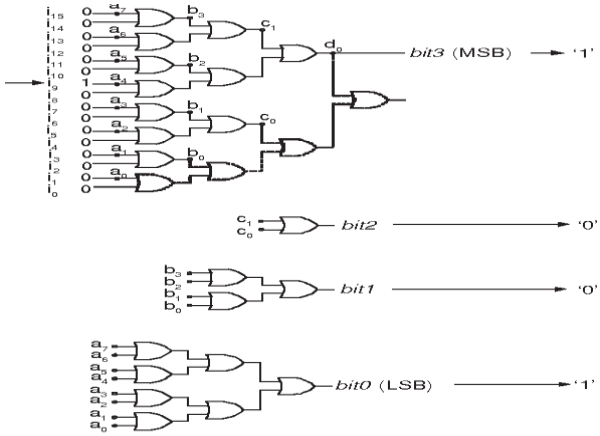


Fig-6.1.3: Circuit diagram of 4-bit fat tree encoder

6.1.4 MUX based encoder

For the designing of flash ADCs, this architecture is commonly used as it operates at high speed and occupies small chip area in comparison to above discussed architecture. The block diagram of conventional MUX based encoder is illustrated in figure-6.1.4. This structure has a disadvantage of large fan-out which increases the overall power consumption. So proposed a modified MUX based encoder which gives a better results in terms of area, power and propagation delay[14]. Figure-6.1.5(a) shows the architecture of modified MUX based encoder and truth table for the same is shown in figure-6.1.5(b).

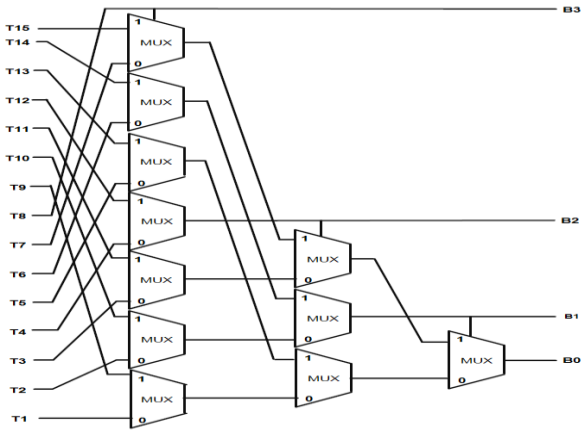
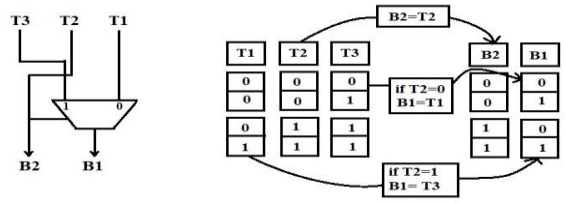


Fig-6.1.4: 4-bit Existing **MUX** based encoder

Here, thermometer codes are represented by T[1]-T[3] and binary codes are represented by B[0]-B[2].



(a) (b)

Fig-6.1.5: circuit diagram and truth table for 3- bit thermometer to binary encoder

Now, a 7-bit thermometer to binary encoder can be implemented by utilizing a 3-bit encoder. Figure-6.1.6 demonstrates the circuit diagram of 7-bit thermometer to binary encoder and its truth table is illustrated in figure-6.1.7

It can be concluded from the table that B[2]=T[4] whenever T[4] equals zero ,then bits B[2]-B[0] are found to be equal to that of the outputs obtained from the 3-bit thermometer to binary encoder keeping T[3]-T[1] as inputs[21]. and When the T[4] bit equals 1 then bits B[2]-B[0] are found to be equal to that of the outputs obtained from the 3-bit thermometer to binary encoder keeping T[7]-T[5] as inputs.

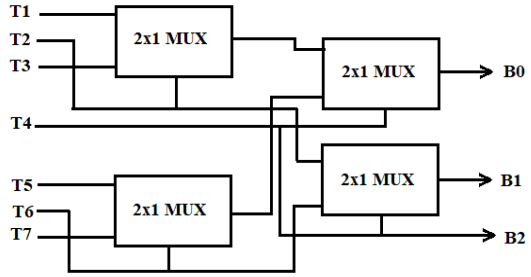


Fig-6.1.6: Block diagram of 7-bit thermometer to binary code encoder

T[7]	T[6]	T[5]	T[4]	T[3]	T[2]	T[1]	B[2]	B[1]	B[0]
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	0
0	0	0	0	1	1	1	0	1	1
0	0	0	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

Fig-6.1.7: Truth table of 7-bit thermometer to binary code encoder

7. GDI TECHNIQUE

Low power consumption and area reduction are the major focus of attention in the designing of digital circuits. High power consumption affects the performance of the portable devices whereas chip area affects the size and cost of the devices. A new methodology is introduced called Gate Diffusion Input (GDI) [15] , which consumes less power and also occupy small area. This technique came up as a promising alternative to existing logic design such as CMOS logic, pass transistor logic and transmission gate logic. Figure-7.1 shows the basic GDI cell. At first glance it looks like a standard CMOS inverter but there are some differences between the GDI cell and CMOS inverters which is[16]:

1. It has three input terminals (P, G and N) and one output terminal. Here, P is the input to source/drain of pMOS, G is the common gate input of pMOS and nMOS and N is the input to source/drain of nMOS.
2. The body of pMOS is connected to the input terminal P whereas body of nMOS is connected to input terminal N.

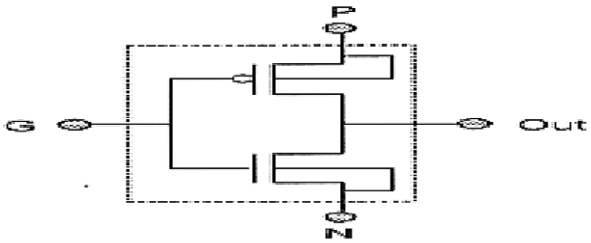


Fig-7.1: A basic GDI cell

A simple modification to the input configuration of the simple GDI cell corresponds to very different Boolean functions which is described in table-1

Table 1: output functions corresponding to different input combination

N	P	G	OUT	FUNCTION
'0'	B	A	$\bar{A}B$	F1
B	'1'	A	$\bar{A}+B$	F2
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
'0'	'1'	A	$\bar{A}$	NOT

Designing of these functions are very simple in GDI cell. For each function aforementioned only two transistors are required. However for executing the same function in CMOS, design becomes complex. Many logic functions can be implemented using GDI method as illustrated in Table -1. For example, consider a circuit diagram shown in figure- 7.2. XOR gate plays an significant role in realization of numerous digital circuits such as adder, multiplier, compressor etc.[17].

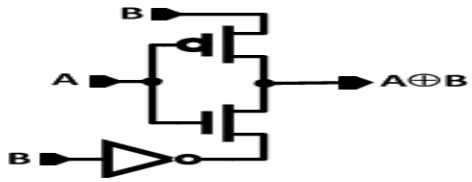


Fig- 7.2: GDI based XOR gate

A total of four transistors are used in designing of XOR gate. The output is given by:

$$A \oplus B = \bar{A}\,B + A\bar{B} \quad (1)$$

The operation of GDI based XOR gate is as follows:

1. When A and B are equal to '0' then NMOS transistor is in cut off and PMOS is in linear region. At Vi–Vtp < out < Vdd, XOR gate yield a value equal to threshold voltage of PMOS transistor (Vtp). At this duration NMOS is in cut off region as Vi<Vtn.
2. Output of XOR gate is high i.e. Vdd passes to the output through pMOS at A=0, B=1..
3. The output of the XOR gate is equal to Vdd-Vtn where Vtn is the threshold voltage of nMOS transistor when The pMOS transistor is turned off and nMOS transistor is turned on at A=1, B=0, where pMOS is cut off Vi<Vtp and nMOS in the linear region Vi–Vtn<Vout< Vdd.
4. A low output is produced when pMOS is in cut off region and nMOS is turned on at A=1 and B=1.

Table -2: Truth table of GDI based XOR gate

A	B	OUT
0	0	Vtp
0	1	Vdd
1	0	Vdd-Vtn
1	1	gnd

However, the problem occurs with GDI cell is that they suffer from threshold drop problem. To get over this problem, proposed a FS-GDI methodology. This methodology employs a transistor which restores the swing and recovers the output swing of gate diffusion input based functions. The SR transistor will be activated only when V^{th} (threshold voltage) drop occurs in the output. Now, taking into considerations the two gates, i.e. F1 and F2, the threshold voltage drop V^{th} will appear at only one of the logical level. It will be supply voltage minus the threshold voltage rather than supply voltage in F2 whereas in case of F1, it will be threshold voltage rather than 0V.

To assure the full swing operation we need a single SR transistor[18]. However swing restoring transistor is controlled whenever there is an inverted representation of the gate input signal of the GDI cell in the circuit. The diffusion input of this transistor will be same as that of a GDI but of opposite nature (that is the n-type MOSFET for F1 and p-type MOSFET for F2). Hence providing a path to the input signal through both types of transistors (Original GDI cell transistor and its complementary transistor). So when it comes to a promising alternative for restoring swing buffers, FS-GDI stands in designs where inverted signals are a part of logic function implementations. Architecture of XOR gate which is constructed with the help of full swing GDI methodology is shown in figure-7.3

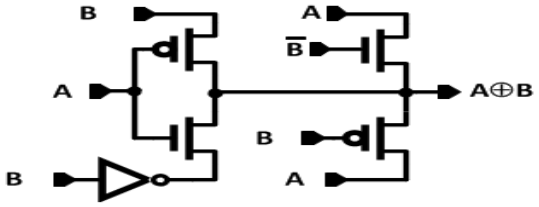


Fig-7.3: Circuit diagram of XOR gate using FS-GDI technique

Full adder can be realised using XOR gate and multiplexer. It acts as a building block for many arithmetic circuits. As the transistor sizes are decreasing day by day, the demand of circuits consuming low power have been increased. Hence gate diffusion technique emerges out to be beneficial for designing low power digital circuits. Figure-7.4 shows the structure of adder based on FS-GDI method. The structure is designed using two XOR gate and one multiplexer. Full adder performs addition of three inputs and yields two outputs which are carry and sum.

The expression for full adder which describes its operation is:

$$\text{Sum} = A \oplus B \oplus C \quad (2)$$

$$\textit{Carry} = AB + BC + CA$$

$$= A\overline{(A \oplus B)} + Cin(A \oplus B) \quad (3)$$

FS-GDI cell based full adder consists of 16 transistors and Table-3 shows the truth table for the designed full adder.

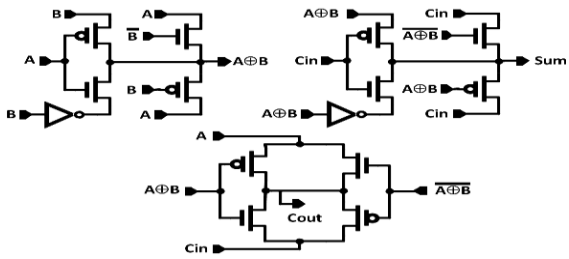


Fig-7.4: circuit diagram of FS-GDI based full adder.

Table-3: Full adder truth table

A	B	Cin	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

8. PROPOSED POWER AND AREA EFFICIENT ADC

For power and area efficient ADC we are proposing 3 bit flash ADC using MUX encoder based on GDI technique whose results we will discuss in our next paper

9. CONCLUSIONS

Low power consumption and area reduction is today's requirement for portable systems. The integration of analog and digital world causes the necessity of data converters. For high speed applications, flash ADC is considered to be the best choice over other ADCs. The performance of a flash ADC depends upon the comparator and an encoder thereby choosing an appropriate architecture for designing individual components of flash ADC can enhance its performance related to area, speed and power which makes them suitable for low power and high speed applications. In this paper, my works is focused on designing of low power thermometer to binary encoder.

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AUTHORS

M JAMAL AZMI[1]

Maria Jamal Azmi received the M.Tech.(Control and Instrumentation) in 1998 from Delhi College Of Engineering, Delhi and did her Ph.D. in Electronics and Communication from Jamia Millia Islamia, New Delhi, in 2012. Since 1999, she has been the part of Indira Gandhi Institute Of Technology (Now IGDTUW), Kashmere Gate ,where she is Assistant Professor in the Department of Electronics & Communication Engineering.

S A IMAM[2]

Syed A Imam has received the M. Sc. Engg. degree from AMU, Aligarh and PhD. degree in Electronics & Comm. Engg. from Jamia Millia Islamia, Central University, New Delhi, in 1998, and 2008, respectively. Since 1990, he has been part of Jamia Millia Islamia University, where he is Associate Professor in the Department of Electronics and Communication Engineering. He has more than 50 publications in journals and conf. of repute.

