Performance Characterization Of n-Channel Hetero-Dielectric Gate Tunnel Field effect Transistor (TFET) In Sub-Micron Region

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Abstract - *To fulfill the performance demands of low-power mobile devices, a high ION/IOFF ratio at low-VDD necessitates a specific device design. TFETs are increasingly favored due to their superior characteristics like low subthreshold slope and high transconductance compared to MOSFETs. However, silicon-based TFETs exhibit a drawback of low on-state current, limiting their applicability in high-performance scenarios. To address this issue, employing a narrower band gap material such as Ge can enhance tunneling efficiency at the source side. Furthermore, mitigating the larger ambipolar current associated with Si-TFETs can be achieved through a n-channel hetero-gate-dielectric (HGD) TFET. This research aims to propose and characterize a novel TFET structure leveraging hetero structure and hetero-gate-dielectric advantages, thereby enhancing ION while suppressing ambipolar current. The structure incorporates a hetero-dielectric Buried Oxide (BOX) on the doped substrate to reduce ambipolar current. The source-to-gate overlap technique is employed to attain the desired subthreshold slope (SS). All simulations are conducted using a 2-D TCAD simulator, specifically Atlas Silvaco. The structure is optimized based on metrics such as ION/IOFF ratio, and simulation results are compared with existing structures in literature for performance evaluation.*

*Key Words***:**   TFET, Heterro Gate Dielectric, Ambipolar current, ON current, simulation.

1.INTRODUCTION

Previously, MOSFET miniaturization was effective for circuit performance enhancement, but in the post-scaling era, its effectiveness is hindered by increased leakage current and short channel effects (SCEs) [1-3]. To address these challenges, researchers have proposed various alternative structures beyond planar ones [4-6], including multi-gate devices and those employing different materials to replace standard CMOS technology [7-9]. Leakage current emerges as a significant issue in the nanoscale regime, disrupting device stability. Thus, controlling leakage current without compromising ON current becomes a critical challenge. Nanowire transistors, particularly tunnel field-effect transistors (TFETs), have been suggested as potential replacements for planar MOSFETs [10-14]. Formerly, downsizing MOSFETs effectively boosted circuit

performance, but in the post-scaling era, short channel effects (SCEs) and increased leakage current have undermined its efficacy [2-3]. Various non-planar structures, including multi-gate devices and alternatives to conventional CMOS technology, have been proposed in literature [4-9]. Suppression of leakage current without compromising ON current is a primary challenge in the nanoscale era, where leakage current significantly impacts device stability. Nanowire transistors, particularly tunnel field-effect transistors (TFETs), have been suggested to manage leakage current [7,10,15].

TFETs are poised to replace planar MOSFETs in the future [13,16,17]. Despite TFETs exhibiting a reduced subthreshold slope (SS) at room temperature (60 mV/decade), they suffer from two main drawbacks: lower ON current and higher ambipolar current [14-18]. TFETs with gate-drain overlap structure have been proposed to reduce ambipolar current [9], albeit at the expense of reduced chip density. The ON current of TFET devices can be enhanced by employing high-k dielectric materials as gate insulators [18], albeit with increased ambipolar current. In addressing these drawbacks, hetero-dielectric gate (HDG) TFETs have been proposed in literature. HDG TFETs utilize SiO2 at the drain to decrease ambipolar current and a high-k material partially near the source to boost ON current.

In this paper, we have studied the electrical behaviour of the n-channel HGD TFET devices in terms of surface potential, tunneling width, drain current and ambipolar current. We have ignored the source/drain depletion width due to heavy doping and quantum confinement effect due to silicon film thickness (> 3 nm). The structure of this paper is given as follows: Section 2 describes device structure of the model. Section 3 discusses the electrical behaviour of the proposed structure and at the end, we conclude the paper in section 4.

2. DEVICE STRUCTURE

2.1 Structure of n-channel HGD TFET

The 2-D structure and coordinate system of the proposed n-channel hetero-gate-dielectric TFET (HGD TFET) is shown in Figure 1 below.
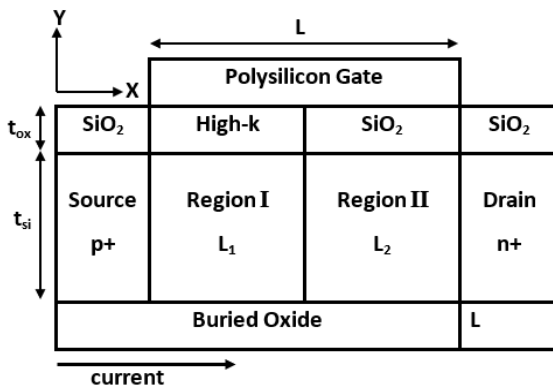
Fig -1: Structure of n-channel HGD TFET

The proposed structure has a hetero-dielectric gate, which means that the gate dielectric is composed of two different materials with different dielectric constants. The hetero-dielectric gate consists of a buried oxide layer (BOX) and a top dielectric layer, which are located between the metal gate and the low-k dielectric layer. The hetero-dielectric gate is designed to reduce the ambipolar current and enhance the on-state current of the device.

2.2 Analytical Model

The pseudo-2D method was employed to solve the Poisson equation due to its computational efficiency, simplifying the solution process.

Referring to Figure 1, after disregarding fixed carrier oxide charges, the 2-D Poisson's equation for the potential distribution ψj(x,y) in the corresponding region is expressed as [19-20];

$$\frac{d^2 \psi_j(x,y)}{d^2 x} + \frac{d^2 \psi_j(x,y)}{d^2 y} = -\frac{q N_a}{\varepsilon_{si}} \qquad (1)$$

Where, N_a is the channel doping concentration, j=1, 2 represents the region I and region II respectively, ε_{si} is the silicon permittivity, $\psi_j(x,y)$ is the 2-D electrostatic potential in the region I and II measured with respect to Fermi potential respectively.

The 2-D electrostatic potential in the channel can be represented as follows by assuming a parabolic potential profile along the film thickness (i.e. along the y-direction),

$$\varphi_{j(x,y)} = a_0 + a_{j1}y + a_{j2}y^2 \qquad (2)$$

Where, a_{0j} , a_{j1} and a_{j2} are constants and function of *x*-only. The following Boundary Conditions(BCs) can be used to obtain these constants:

$$\frac{d^2 \varphi_{j(x,y)}}{dy^2}\bigg|_{y=0} = 0, \qquad (3)$$

$$\varphi_{j(x,y)}\bigg|_{y=\frac{t_{si}}{2}} = \phi_{sj(x)}, \qquad (4)$$

$$\frac{d^2 \varphi_{j(x,y)}}{dy^2}\bigg|_{y=\frac{t_{si}}{2}} = -\frac{C_{ox1}}{\varepsilon_{si}}\left[V'_{GSf_j} + \phi_{Sj(x)}\right] \qquad (5)$$

Where $\phi_{Sj(x)}$ is surface potential, $V'_{GSf_j} = V_{GS} - V_{fb}$.

V_{fb} is flat-band voltage which is given as

$$V_{fb} = \phi_m - \left[x + \frac{E_g}{2} + \frac{kT}{q}\ln\left(\frac{N_c}{n_i}\right)\right]$$

3. RESULTS AND DISCUSSION

The proposed analytical models are simulated for following values of the parameters; L=50 nm, t_{ox1}=t_{ox2}=3 nm, t_{si}=10 nm, V_{ds}=0.7 V, N_s=1020 /cm^3, N_d=10^{18}/cm^3, N_c=10^{16}/cm^3 unless and until specified.
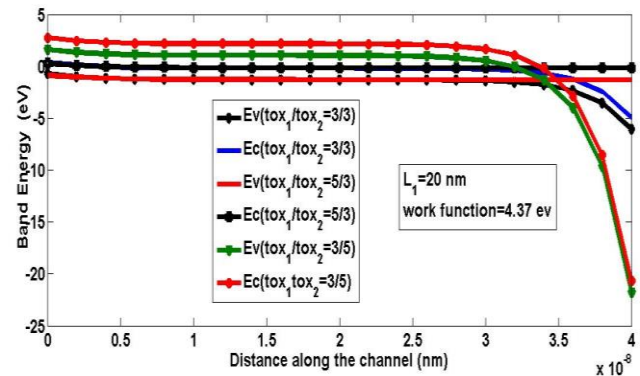

Fig -2: Band diagram for various combination of oxide thicknesses in two regions

From Figure 2 above, the result shows that sharp band bending occurs for t_{ox1}=3 nm and t_{ox2}=5 nm due to reduction of equivalent oxide thickness which enhances the coupling between the gate and the channel junction. The surface potential change was observed to occur mainly within about 10 nm from the source-channel interface. This is entirely in the high-k region. The surface potential outside the tunneling space (mainly in the low-k region) changes little. This indicates that the tunneling is controlled only by the high-k dielectric and the drain has no effect on the tunneling current. This behavior allows for better control and optimization of the tunneling current, leading to improved transistor performance. By focusing on optimizing the properties of the high-k dielectric, such as its thickness and dielectric constant, the TFET can be designed to achieve specific performance targets such as low power consumption, high speed, or high gain.

Figure 3 shows the variation of surface potential along the channel of the proposed structure. The surface potential first reduces along the channel for x ≤ 25 nm and then increases sharply. The sharp rise in surface potential near drain

restricts the tunnel of carriers from drain to channel and hence suppresses the ambipolar current. The change in surface potential due to increased gate-source voltage greatly narrows the tunneling width for charge carriers near source and hence results in larger tunneling probability. The MAPE (mean absolute percentage error) reported in between model and 2-D simulator results are given in Table 1. The error between two results is less than 5% which confirms the validity of the developed analytical model.
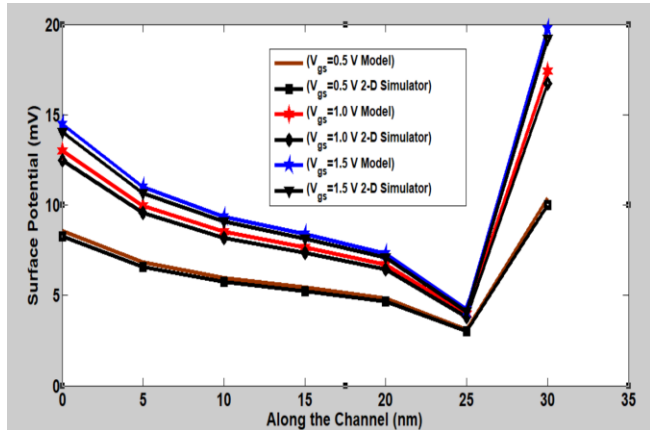

Fig -3: Surface potential variation along channel length: comparison with 2-D ATLAS simulator

Table -1: Mean Absolute Percentage Error (MAPE)

V_{gs} (V)	MAPE %
0.5	4.2
1.0	4.2
1.5	3.13

The effect of length L1 on the surface potential of the proposed structure has been analyzed. As L1 decreases, conduction band becomes shallower which results in lower tunneling currents whereas the increase in L1 results in wider conduction band as seen from Figure 4. The larger conduction band increases the ambipolar current. Therefore, to restrict the ambipolar current and to achieve larger ON current we have chosen L1=15 nm which is the best choice. This choice offers a good balance between the two important characteristics of TFETs namely, tunneling and ambipolar currents.
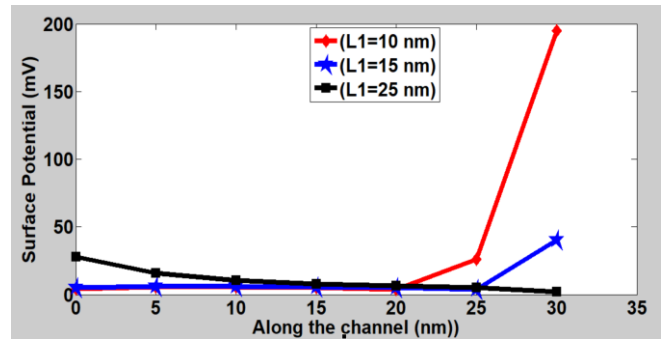

Fig -4: Surface potential variation along channel length for different length of High-κ Oxide
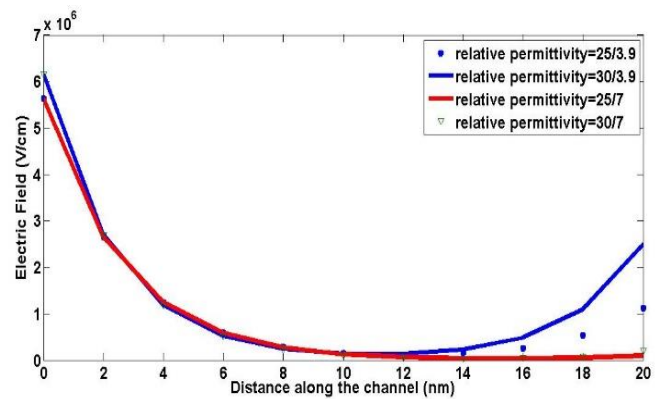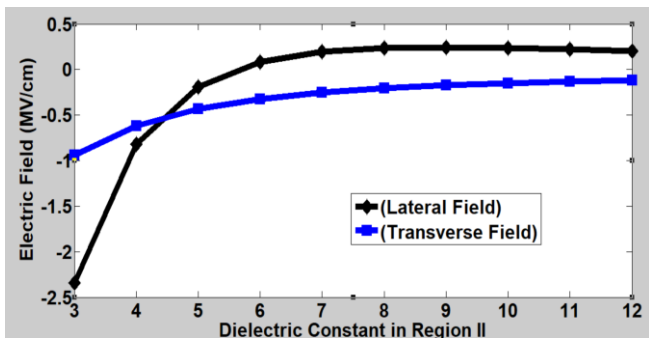

Fig -5: Variation of the electric field along the channel for different dielectric constant (relative permittivity) combinations

The lateral electric field decreases along the channel and reaches a minimum value in mid-range of the channel. Figure 5 shows the variation of the electric filed along the channel for different combinations of dielectric constants. We observed that electric field takes on a larger value when region I is occupied by high-k dielectric material.

The lateral as well as transverse electric field of region II have been analyzed in detail as shown in Figure 6. Both the fields increase as the dielectric constant κ-increases. From analytical results, it is observed that for κ≤ 4, fields take negative value. The negative field in drain-channel region decelerates the carriers and hence suppresses the ambipolar current. From this result, it is clear that SiO_2 dielectric material near drain-channel region, is the natural choice to control the ambipolar current.

Fig -6: Electric Field Variation with dielectric constant in region II

Figure 7 shows the variation of lateral electric field in region I along the channel for single dielectric gate TFET and hetero dielectric gate TFET when κ=25 and κ=50. It is observed that field takes larger value near source-channel junction for κ=50 due to better control of gate over the channel. The peak of the lateral electric field near the source-channel interface is responsible for the larger tunneling probability.
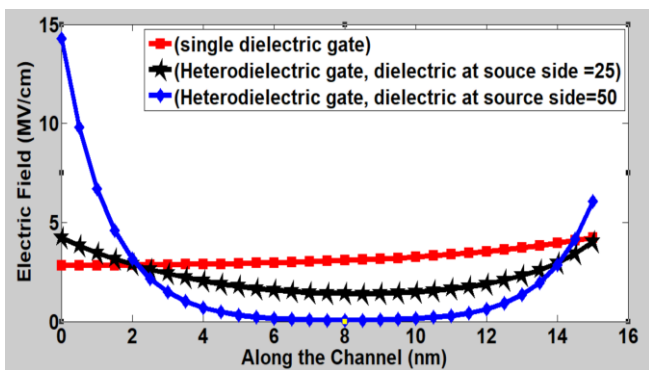

Fig -7: Total Electric Field variation along region I for single dielectric gate and Hetero-dielectric gate

Increasing the doping concentration ratio between the source and drain regions leads to a more abrupt surface potential near the source end, resulting in improved electrical characteristics characterized by a narrower tunneling width. This effect consequently lowers the threshold voltage independent of the channel length, as depicted in Figure 8.
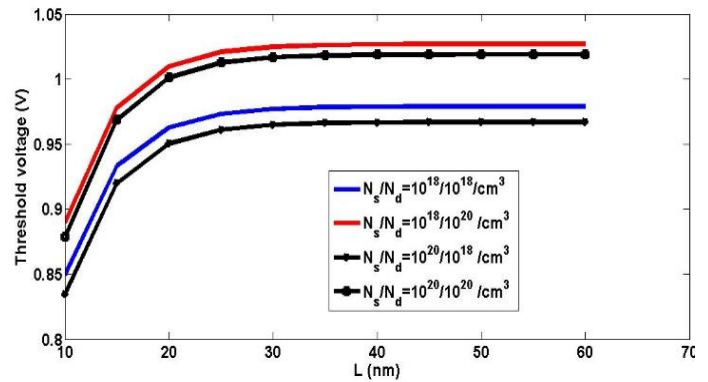
Fig -8: Threshold Voltage of HGD TFET Device Versus Channel Length for Different Concentrations Combination in the Source and Drain Regions

As the length of region 1 decreases, conduction band becomes flatten, which makes band-to-band tunneling difficult and hence increases the threshold voltage. This is due to the conduction band becomes more flat, which makes it harder for band-to-band tunneling to occur, as shown in Figure 9. It is observed that the larger tunneling length L_1 accumulates more charges, which resulting in a lower threshold voltage.
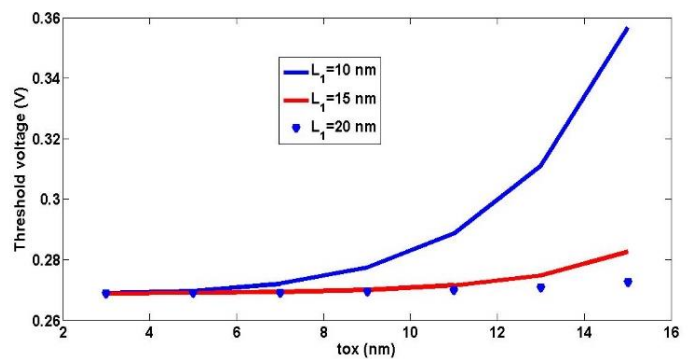
**Fig -9**: Threshold Voltage Variation with t_{ox} for Different Tunneling Length (L_1)

Figure 10 shows the variation of drain current per unit channel width with gate source voltage. For negative gate bias voltage, ambipolar current decreases and reaches its minimum value at Vgs= -0.4 V. The on-current starts only when gate-source voltage is equal or larger than threshold voltage which is more than 500 mV in this structure. The mean absolute percentage error (MAPE) is calculated in this case and found to be 3.1% which confirms the validity of the developed analytical model of current. The slight difference at lower gate source voltage is due to negligence of mobile carriers.
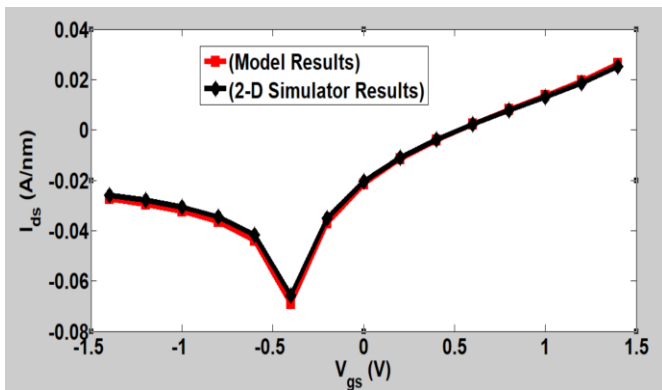
Fig -10: Comparison of drain current with 2-D ATLAS simulator results

To see the effect of work function on the drain current of the hetero dielectric gate TFET, we have studied the current for single metal TFET and dual metal TFET under two cases; cas1 1: tunnel gate having higher work function (4.5 eV) than auxiliary gate (4.25 eV) and case 2: auxiliary gate having higher work function (4.5 eV) than tunnel gate (4.25 eV). Figure 11 shows the simulation results. In case 2, the band width overlaps increase which results in narrow tunneling width and hence ultimately on-current increases on the cost of increased ambipolar current. This result also suggests that the work function difference results in change in surface potential which improves the gate control over tunneling process. A narrow tunneling width gives a larger tunneling probability of carriers. Therefore, we can conclude that gate dielectric engineering along with choice of metal can be employed in HDG TFEET design to enhance the tunnel current and reduce the ambipolar current.
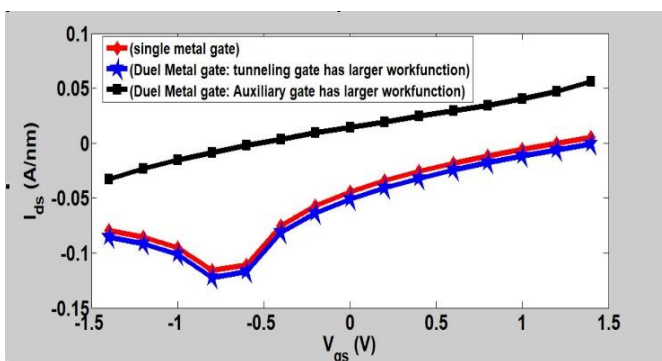
Fig -11: Transfer characteristics of single metal gate and dual metal gate with Hetero-Dielectric

4. CONCLUSIONS

This paper offers a comprehensive analysis of the HGD TFET device, a promising candidate for low-power and high-performance applications. The proposed tunnel width model is validated through 2-D TCAD simulation results, showing good agreement. The device structure effectively suppresses ambipolar current, enhances ON current, and mitigates short channel effects. Gate engineering proves effective in reducing ambipolar current, increasing transconductance, and lowering the threshold voltage. Moreover, the proposed structure exhibits a lower subthreshold slope and higher transconductance compared to conventional TFET devices. To further enhance device performance, a combination of material engineering and thinner source gate oxide can be employed. Overall, this paper provides valuable insights into the design and optimization of HGD TFETs for future low-power and high-performance electronic applications.

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