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Application of Vertical Transistors in Advanced Memory and Logic Development

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***Abstract*—**Vertical Tunnel Field Effect Transistors (VTFET) has a different working principle than traditional FET's and are said to be more beneficial than the traditional FinFETs that we have been using for decades. This paper presents a new device architecture, which can be shared by a wide range of sorts of semiconductor transistors. Here, the significance and prerequisites of the vertical transistor in the VLSI industry alongside its device processing have been illustrated. It moreover talked about the benefits and applications in memory, logic technology alongside analog development over past years. Vertical semiconductors have helped decrease expenses per bit for flash memory and it has assisted with diminishing the leakage current in most recent innovation hubs. Looking for better performing devices specialists are presently investigating 3D designs, for example, vertical semiconductors, whose benefits incorporate low power consumption, smaller current leakage towards the bulk, and better suitability for adaptable hardware.

Keywords: Vertical Tunnel Field Effect Transistor (VTFET), atomic layer affidavit (ALD), Silicon-On-Insulator (Sal), gate-all-around (GAA), 3D designs, Memory application.

I. INTRODUCTION

Modern electronics are mostly flat, with millions of planar silicon transistors lying on a chip's surface. These are getting faster and efficient every day because of the tiny chips that power these electronics evolving at an unprecedented rate. Our understanding at transistors or chips starts with a term called Moore's Law. This law states that the number of transistors on a chip double about every two years. The speed of the chip depends on the number of transistors on the chip. As the number of transistors keep on increasing year by year, we should now be worried about running out of space on the chip. One solution to overcome this problem is, to find a new technology where space is not the constraint, VerticalTransport Field Effect Transistors. This is a new technology to overcome the problem with the traditional MOSFET's. In Vertical-Transport Field Effect Transistors (VTFET), the transistors are arranged perpendicular to the plane of the chip. This eliminates the space constraint and allows the engineers to pack a lot more transistors vertically in a given space. The VTFET's are said to dominate the speeds of traditional FinFET's. The transistors that we currently use has three terminals on the same plane: gate, source & drain. When a small voltage is applied to the gate terminal, the transistor will turn on and the current flows from source to drain. When these transistors are placed on the chip, there is a very high chance that the adjacent transistors interfere each other. To prevent them from interfering, we place dummy gates between the transistors which occupies additional area on the chip. VTFET's does not need these dummy gates between them – they instead use something called as shallow trench isolation which doesn't require any additional space on the chip. The current in VTFET's also changes it direction from the traditional FinFET's, which is perpendicular to the surface of the chip. This gives us the flexibility to change the length of the gate to control the current. to as "16/14," but real "7nm" node circuit densities will necessitate the next generation of lithography, EUV at 13.5nm wavelength. The cost of the chip, which ischallenged by the requirement for unique cost-intensive patterning techniques, is the key to acceptance in the electronics device area. Given the higher wiring parasitic, the ability to gain more performance at constant chip power will be the key to adoption in the server area. To get to mature 7nm nodes, new materials will be required in all scenarios.[3]

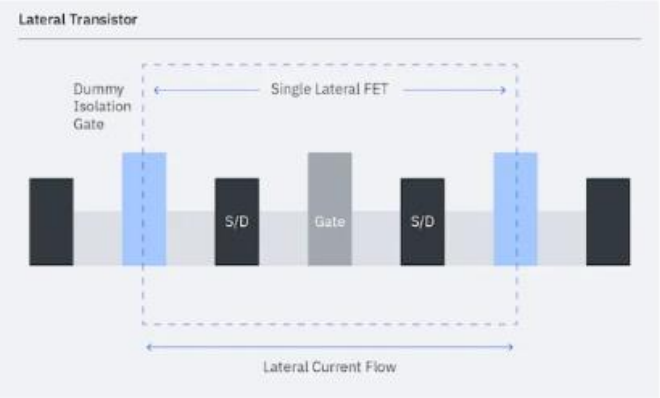

Fig. 1. FET Configuration

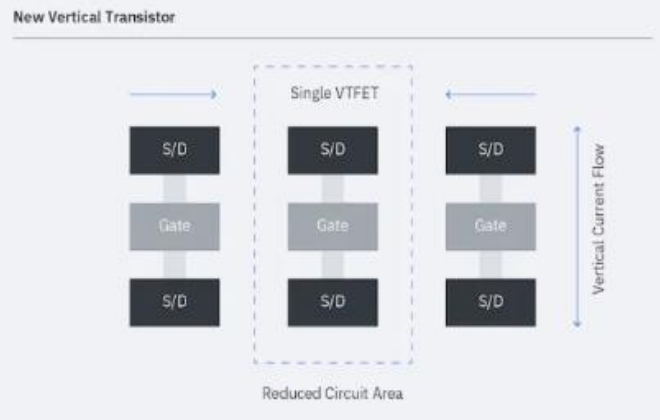

Fig. 2. VTFET Configuration

In a research performed by IBM, it is observed that the VTFET's can allow up to five times more transistors on the chip of the same size. They also observed that there is a reduction in the capacitance and resistance, which reduced the power in VTFET's.

II. FABRICATION METHOD FOR VERTICAL SURROUNDING GATE TRANSISTOR

Proceeding with endeavors in Complementary Metal Oxide Semiconductor (CMOS) research have led to the remarkable increment of device integration density during the last 40 years. In the recent past increasing fabrication costs and increasing overall variability have turned into a hindrance for the scaling pattern. To beat such limits, impressive examination is devoted for instance to the use of new materials (such as high-x dielectrics with metal gates), dual-gate devices, novel isolation techniques that make use of Silicon-On-Nothing (SON) or Silicon-On-Insulator (Sal) substrates [1]. The vertical FET of the figure. 3 was first delivered by gate and etch-back methodology. A n+ Si (111) (~0,002ωcm) substrate was utilized for vertical FET structure and a p+ Si(111) (ρ ~ 0.04 Ωcm) substrate was utilized for steep SS switch application. The gate oxide was produced using 1ML-Al2O3/4 ML-HfO2 by the atomic layer affidavit (ALD) and the thickness was 4-14 nm. Then, tungsten (W) was saved as a RF faltering metal gate. W is lithographically portrayed in NW-designed veils (50 × 50 μm2) and the NWs were then covered by benzocyclobutene (BCB) and covered by receptive particle drawing (RIE) with CF4/O2 mixed gas to draw BCB, W, and HfALO gate oxide constantly.[4][5] After the RIE, the NWs had been encased by the BCB and scaled back by the RIE to oblige the metal gate and pipe. By then, Ni/Ge/Au/Ni/Au vanished into a lithographically described locale as a channel link for the InGaAs nanowire-net. Over the long haul, the NW-SGT was tempered at 420ºC in N2 including the acquisition of Ohmic contacts in the source / channel region as a post metallization step to reinforce the gate oxide.

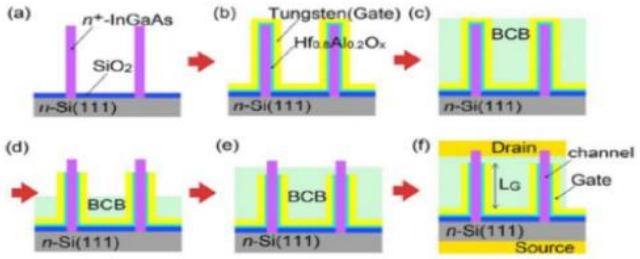

Fig. 3. Device fabrication processes: (a) InGaAs NW growth. (b) Atomic layer deposition of Hf0.8Al0.2Ox and sputtering of W-gate metal. (c) Spin-coating of BCB polymer. (d) RIE of BCB, gate oxide and W metal. (e) Spin-coating of BCB and RIE etch back for electrical separation layer formation. (f) Drain and source metal evaporation

III. CHALLENGES IN MEMORY VTFET

VTFET technology will impact memory technologies and could potentially replace DRAM's with SRAM's. We know that DRAM is a cheap memory technology which stores the data using a capacitor. But SRAM's are comparatively faster than DRAM's which does not require refresh cycles as the data is non destructive i.e does not require a writeback. But the capacitor which is used to store data in DRAM needs to be refreshed at regular intervals to hold the data in it unlike SRAM. If the dependency on this capacitor is eliminated, the memory can be made more scalable. Capacitor less 1T-DRAMs are receiving increasing attention for memory applications due to the integration limitations of conventional single capacitor DRAMs in nanoscale CMOS technologies.[7] [8] So the vertical transistors comes in to picture to improve this scalability that the traditional DRAM is seeing.The trench capacitance in the vertical transistors can replace the capacitor that is present in the DRAM which will also help improve the retention time of the memory. The trench structure reduces the electron-hole recombination. With the valence band offset between GaP and Si, holes can be confined in the storage region for improved retention times. As VTFETs uses trenches structures, eliminating holes is very tough as the voltages required to bias such devices is very large. This large biasing voltages will generate large currents in the device which directly relates to increase in power consumption. There are few papers which discussed how this power consumption can be reduced significantly by using alternate methods where the operating current in the device is reduced for low power applications.[2]

IV. OPERATING PRINCIPLE

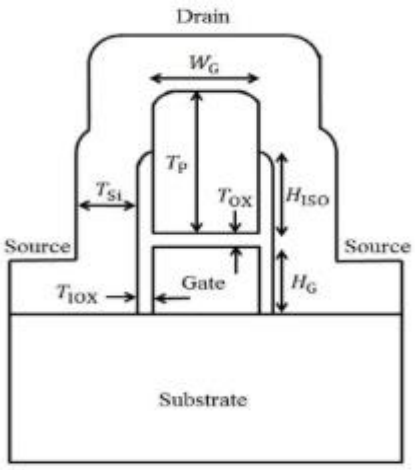

Fig. 4. DRAM Schematic

Fig. 4 shows the schematic of the DRAM that is implemented using a type of vertical transistor i.e body over gate vertical nanosheet transistor. This device has a 3-wide source contact and one contact for the drain terminal. A significant amount of drain current is generated when the drain is positively biased. The write operation in this DRAM is controlled by the ionization between n-type channel and the ptype body. This ionization effect can be seen in the Fig. 5. With the help of positive drain bias voltage, the holes were forced to the p-type body which reduces the threshold voltage by accumulating the excess carriers in the storage region. Because of this, the reading current will increase. [6]

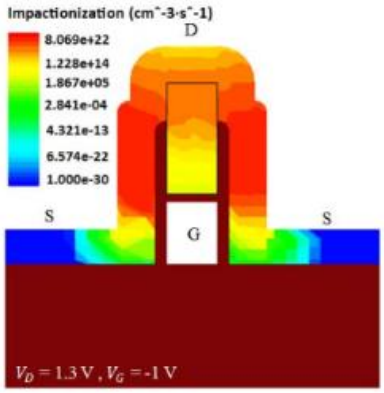

Fig. 5. Impact Ionizations

With the help of this positive drain bias voltage, the holes will be pushed into the storage region which can be retained in the p-type body with the help of negative gate bias voltage. SO holding the value 1 has a very high state density. In contrast, holding 0 will have a low hole density. This can done by forward biasing the device which will then expel the holes from the storage region. This is how the date is stored in the device.

V. I-V CHARACTERISTICS

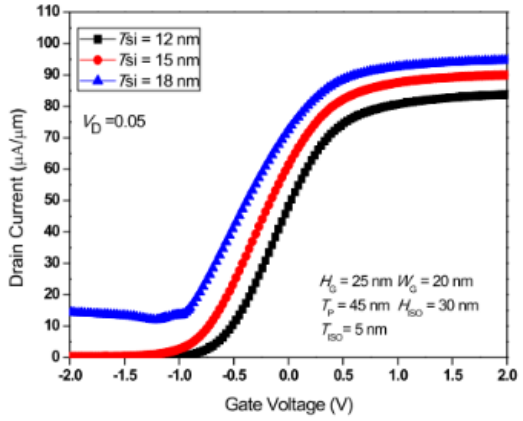

Fig. 6. IV Characteristics with different channel layer thickness

Fig. 6 shows the IV characteristics of the device when the layer thickness of the channel is varied. This figure illustrates how the channel layer thickness impacts the input characteristics. The channel layer thickness can be controlled by controlling the gate voltage. This impacts the programming window when the width of the channel is made too thick or too thin. So the thickness has to be optimized such that the programming window is not affected. From the figure we can also observe that the leakage current is increasing when the channel thickness is increased. So we should also make sure that the leakage current is not too large by selecting the optimal channel layer thickness.So from the above plot, we can see that the red curve is optimal with normal leakage current when compared to the other 2 curves. The programming window also depends on the isolation heights. This improves as isolation height is lowered since there are wider drain-end regions, which help to collect and store holes generated by the impact ionization simply by using negative gate bias.So it is better to maintain the drain-end regions as wide as possible so that it will allow the memory to write 1s and 0s efficiently.[9]

VI. MEMORY APPLICATION

Significance of the Flash memory can be featured in numerous ways. NAND/NOR flash is quite possibly the main use of vertical transistors. Flash memory is a non-volatile memory chip used for capacity and for moving data between a (PC) and computerized devices. It tends to be electronically programmed and erased. EEPROM is a sort of data memory device using an electronic charge to eradicate or compose advanced information. Drifting gate transistors are electrically separated and utilize a coasting node in direct current (DC). A remarkable charge trap mechanism is utilized to store the information and its value relies on limit voltage which can be changed. [11]

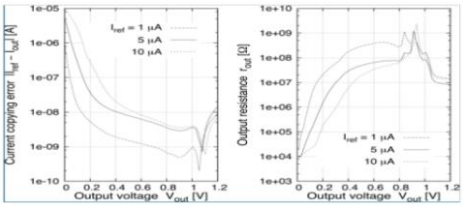

Fig. 7. Current mirror with the VeSFET-based OTA in the feedback loop: (a) current copying error and (b) output resistance .

3D NAND FLASH

3D NAND has ascended as a strong substitution to 2D NAND giving the continued scaling carried forward by extending the number of layers just as utilizing the prevalent cell attributes of the 3D NAND to build the quantity of bits/cell from 3 bits/cell to 4bits/cell. Many organizations, for example, Intel, WDC, Micron have been working on increasing the number of bits they want to store in the given area. A single cell can be used to save 2/4/8/16 bit value contingent on its order as TLC, QLC, MLC, and so on. This can be accomplished however the more number of bits to be stored, the more number of Vth state should be characterized and this comes at the expense of precision.

3D NOR FLASH

NOR flash is generally faster to read than NAND flash , yet it is logically expensive, and it takes more time to delete and compose updated information. NAND has a higher storage bits limit than NOR. Alternately, equivalent NOR Flash memory supports onebyte inconsistent access, which

engages machine rules to be recovered and run straightforwardly from the chip, correspondingly as a traditional PC recovers directions legitimately from the primary memory. Nevertheless, NOR must write in bigger lumps called pages (bits) of data at once than NAND. parallel NOR Flash consists of a static random access memory (SRAM) interface that incorporates sufficient location pins to delineate the whole chip, empowering access to each byte inside it.

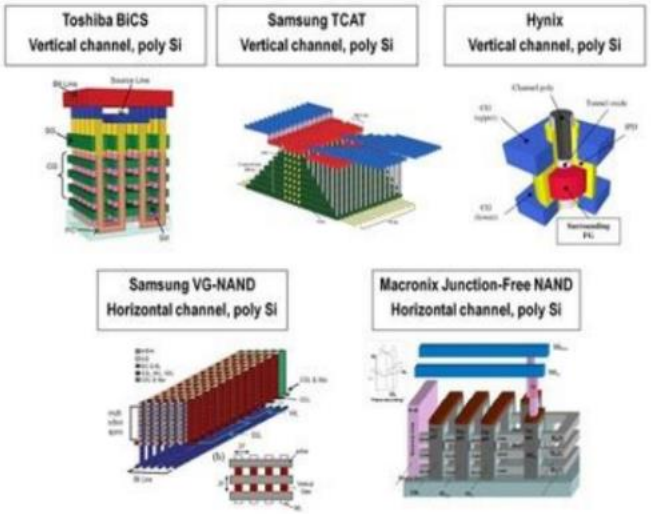

Fig. 8. 3D NAND Flash

VII. VeSFET APPLICATION

The Vertical Slit-based Field-Effect Transistor (VeSFET) is a clever junction-less device with two undefined, independently controlled doors. VeSTIC (Vertical-Slit Semiconductor Based Integrated Circuit) is a lately showed development for low-power VLSI circuits. The circuits are made with an insignificantly changed SOI CMOS process course of action. Lithography necessities are essentially relaxed by the all out departure from the normal rectangular elements in favor of circular ones and by incredible consistency of the design: all the devices, having the similar calculation, are separated on a square structure. Expected as an option in contrast to CMOS, the advancement permits a basic mix of various sorts of device (double door MOSFETs, JFETs, and bipolar semiconductors) on a similar SOI wafer. The key properties of this device incorporates 1) Activity subject to the movement of majority carriers. Thus, the overwhelming system is incomplete consumption of the dynamic area as opposed to reversal. 2) Two undefined, independently controlled gates on either side of the active region associating the source and drain. The central, most secure piece of the active region is insinuated as the slit The strong cross-fragment of the cut (and, subsequently, its conductance) is obliged by the development of drained areas obliged by the voltages of the gates.

Process Nodes	Ref.	Ref.	Ref.
0.13um	11.1	28	37
90nm	10.6	8	14
65nm	6.1	7	9
90nm PTM	10.0		
VeSFET OR	14.5		
VeSFET AND	21.6		

This table shows intrinsic voltage gain of the VeSFET compared to the MOSFET at different process nodes. The values of the above parameters propose that the VeSFET is superior to the MOSFET of the corresponding process node. A model use of the VeSFET based OTA is a high-precision current mirror. The best benefit of the VeSFET, be that as it may, is the presence of two independent gates controlling a common channel. The result voltage of this mirror is allowed to drop well beneath the immersion voltage of Mm2 in light of the fact that the current duplicating precision is ensured by identical operating conditions of both transistors. [9]

VIII. RELIABILITY OF VERTICAL MOSFETs

Strangely, the impact of the most striking vertical MOS unequivocal features like diverse source/drain designing, channel direction, and vertical gate oxide thickness on unwavering quality is examined. In spite of the way that LDD is missing, it is shown that cut back vertical semiconductors have a sufficient unwavering quality for possible use in gigascale recollections. [10][11]

IX. OPERATING STATES AND POWER CONSUMPTION OF DRAM

DRAM working consists of four operating states. These states are: Reading , Writing , Holding , Erasing. Each state consumes some power and this power is different for different states. In one of the IEEE papers, the power consumption for all these four states are discussed clearly and it is found out which state consumes the highest power and which consumes the least power. The power consumption in the erasing state is too low when compared to other states. In contrast, it is found out that the writing states consumes the highest amount of power. In this paper, they did not consider the power consumption of the holding state. This is because, in the holding state the current flowing through the device is negligible i.e almost 0. So this holding state power consumption is not included for the comparison. One important factor to consider here is the work function. When the work function is increased, the input characteristic curves are shifted to the right. This indicates that the gate voltage is being increased when the work function is increased. When the gate voltage is increased more and more, the operating current in the device is decreased which will directly lead to low power

consumption. So the work function is an important factor which will help us to design a low power memory device. In this paper, with the help of simulations, it is observed that the power consumption is reduced by 20.5% when the work function is increased while writing 1 in to the device. The power consumption is reduced by 24.6% when reading 1 and 75% while reading 0. It is observed that the most power is consumed when we are writing 1 to this device. So it is very important for a low power memory device to reduce the power consumed during this writing state. [11][12]

X. CONCLUSION

Applications for the analog/RF and logic circuits have also been discussed and vertical transistors can give upto 78% of area decrease in memory cells and has ended up being helpful in numerous other analog and logical applications. 3D heterogeneous compromise and heterogeneous structures are plausible responses to guarantee consistent advances in CMOS ICs as Moore's Law is wrapping up. Vertical semiconductor applications have conveyed various progressions alongside the difficulties in recent times. It has contributed towards better limits all through the latest couple of years. [12]

We have discussed what challenges are we seeing in the memory's. An important factor which can help reduce the power consumption in the memory device is discussed in this paper. By the simulations results discussed in papers, we have seen how the power consumption is varied for different operating states. By adjusting the work function, we have seen how the power consumption in the device is reduced for different states. This can be used in the low power applications.

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