DESIGN OF 7 LEVEL MULTILEVEL INVERTER WITH REDUCED SWITCHES

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Abstract

A Multilevel inverter is a force electronic gadget that is utilized for high voltage and high force applications and has numerous favourable circumstances like, low exchanging pressure, low absolute consonant twisting (THD). Thus, the size and cumbersomeness of detached channels can be diminished. This work proposes another geography of a 7-level fell staggered inverter with decreased number of switches than that of traditional sort which has 12 switches. The geographies comprise of circuit with 7 switches for a similar 7-level yield. Hence with less number of switches, there will be a decrease in door drive hardware and furthermore not many switches will lead for explicit timespans. The SPWM procedure is executed utilizing multicarrier wave signals. The circuit is displayed and recreated with the assistance of MATLAB/SIMULINK.

Keywords: *Cascaded Multilevel Inverter(CMLI), Diode Clamped Multilevel Inverter(DCMLI), Flying Capacitor, Pulse Width Modulation (PWM), Selective Harmonic Elimination*

1 INTRODUCTION

As of late, the requirement for high force mechanical assembly has been determined by various modern applications. Medium voltage engine drives and utility applications are a few models, since they require medium voltage and megawatt power level. Another application respects medium voltage matrices, where it is problematic to interface just one force semiconductor switch straightforwardly. Therefore, a few staggered power converter structures have been presented as an option in high force and medium voltage applications. Staggered converters accomplish high force appraisals, yet additionally empower the utilization of environmentally friendly power sources. This part examines about the kinds of staggered inverters and its preferences.

1.1 Multilevel Inverters

Multilevel converters not just create the yield voltages with low bending, yet in addition lessen the dv/dt stresses, henceforth electromagnetic compatibility (EMC) issues can be diminished. In addition, three diverse major staggered converter designs, for example, fell H-spans converter with isolated dc sources, diode clipped (nonpartisan clasped) and flying capacitors (capacitor braced) have been accounted for in the writing.

1.1.1 Cascaded Multilevel Inverter

A Cascaded Multilevel Inverter (CMLI) is a force electronic gadget intended to create an AC voltage from DC voltages of a few levels. This design of CMLI comprises of a progression of H-connect (single-stage full extension) inverter units in every one of its three stages. Every H-connect unit has its own dc source. Through various blends of the four switches, S1-S4, every converter level can produce three diverse voltage yields, +Vdc, - Vdc and zero. The AC yields of various full-connect converters in a similar stage are associated in arrangement with the end goal that the incorporated voltage waveform is the amount of the individual converter yields. Every H-connect unit creates a semi square waveform by stage moving its positive and negative stage legs exchanging time. Each exchanging gadget consistently leads for 180° paying little heed to the beat width of the semi square wave. This exchanging strategy causes current pressure of the whole exchanging gadgets as equivalent.

A three-phase CMLI topology is essentially composed of three identical phase legs of the series- chain of H-bridge converters, which can possibly generate different output voltage waveforms and offers phase-balancing for AC system. This feature is impossible in other VSI topologies utilizing a common DC link. Since this topology consists of series power conversion cells, the voltage and power level may be easily scaled. The dc link supply for each full bridge converter is provided separately.

$$V_{an} = V_{dc1} + V_{dc2} + \cdots\cdots\cdots + V_{dc(s+1)} + V_{dcs} \quad (1)$$

Operation of CMLI

A single-phase structure of an m-level cascaded inverter is illustrated in Figure 1.1. Each separate dc source is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, +Vdc, 0 and –Vdc by connecting the dc source to the different combinations of the four switches, S1, S2, S3 and S4. To obtain +Vdc, switches S1 and S4 are turned on, whereas –Vdc can be obtained by turning on switches S2 and S3. By turning on S1 and S2 or S3 and S4, the output voltage is zero.

The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs.

The phase voltage waveform for an 5-level cascaded H-bridge inverter with 2 separate dc source voltage and 2 full bridges is shown in Figure 1.2.

Thus the output voltage of a phase is given as

$V_{an} = V_{a1} + V_a$

Thus, the predominant lower frequency harmonics such as 5^{th}, 7^{th} , 11^{th} and 13^{th} harmonics are eliminated while using this configuration.

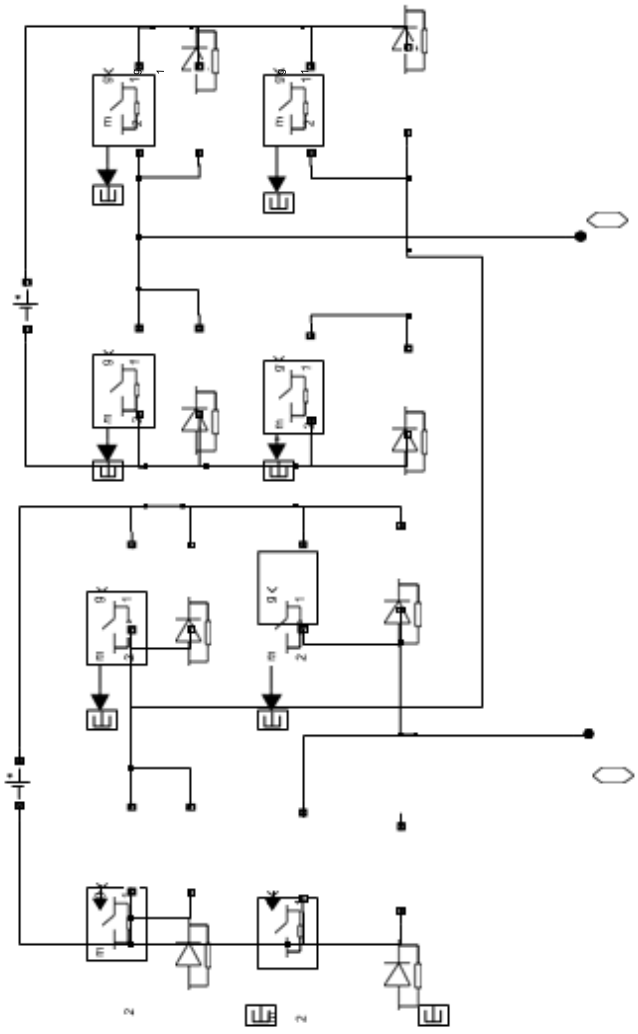

Figure 1 Topology of a cascaded multilevel inverter in one phase

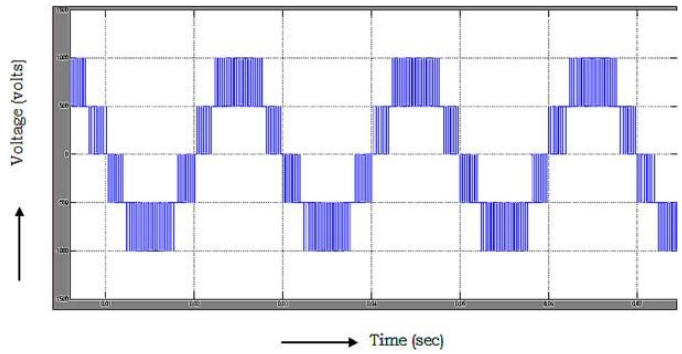

Figure 2 The output voltage waveform of H-bridge

Multilevel cascaded inverters have been proposed for the applications such as static var generation, an interface with renewable energy sources and for battery-based applications. Cascaded inverters are also proposed for use as the main traction drive in electric vehicles. Beside this, the applications of the cascaded inverters are as follows:

1. It is more suitable for high-voltage, high-power applications than the conventional inverters.

2. It generates a staircase voltage waveform approaching a sinusoidal output voltage thereby increasing the number of levels. It does not require any voltage balance circuits or voltage matching devices as it consists of a cascaded connection of many single-phase, full bridge inverter fed with a separate DC source.

1.1.2 Diode Clamped Multilevel Inverter

The general structure of the multilevel inverter is to synthesize a sinusoidal voltage from several levels of voltages typically obtained from capacitor voltage sources. A three level inverter, also known as a “neutral-clamped” inverter, consists of two capacitor voltages in series and uses the center tap as the neutral. Each phase leg of the three-level inverter has two pairs of switching devices in series. The center of each device pair is clamped to the neutral through clamping diodes. The output obtained from a three-level inverter is a quasi-square wave output if fundamental frequency switching is used. Multilevel inverters are being considered for an increasing number of applications due to their high power capability associated with lower output harmonics and lower commutation losses.

Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of AC load. The main multilevel topologies are classified into three categories: diode clamped inverters, flying capacitor inverters, and cascaded inverters. In a three-phase inverter system, the number of main switches of each topology is equal. Comparing with the number of other components, for example, clamping diodes and dc-link capacitors having the same capacity per unit, diode clamped inverters have the least number of capacitors among the three types but require additional clamping diodes. Flying capacitor inverters need the most number of capacitors. But cascaded inverters are considered as having the simplest structure. The diode clamped inverter, particularly the three-level one, has drawn much interest in motor drive applications because it needs only one common voltage source. Also, simple and efficient PWM algorithms have been developed for it, even if it has inherent unbalanced dc-link capacitor voltage problem. However, it would be a limitation to applications beyond four-level diode clamped inverters for the reason of reliability and complexity considering dc-link balancing and the prohibitively high number of clamping diodes. Multilevel PWM has lower dv/dt than that experienced in some two-level PWM drives because switching is between several smaller voltage levels. Diode clamped multilevel inverter is a very general and widely used topology. DCMLI works on the concept of using diodes to limit voltage stress on power devices. A DCMLI typically consists of (m-1) capacitors on the DC bus where m is the total number of positive, negative and zero levels in the output voltage. The phase a output voltage Van has five states: Vdc/2, Vdc/4, 0, - Vdc/4 and - Vdc/2.

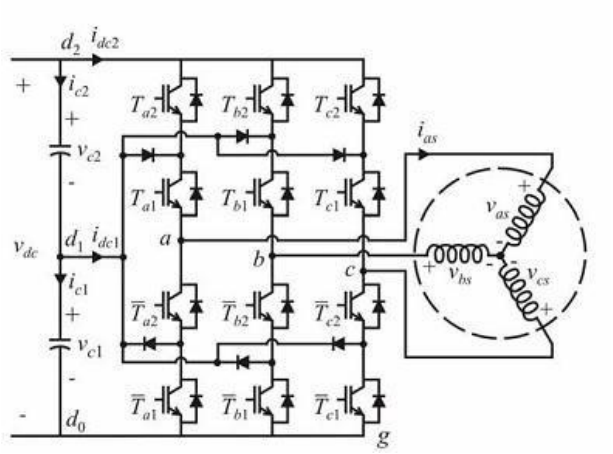

Figure 3 Diode clamped inverter topology

1.1.3 Flying capacitor structure

Another fundamental multilevel topology, the flying capacitor, involves series connection of capacitor clamped switching cells. This topology has several unique and attractive features when compared to the diode-clamped inverter. One feature is that added clamping diodes are not needed. Furthermore, the flying capacitor inverter has switching redundancy within the phase which can be used to balance the flying capacitors so that only one dc source is needed.

Figure 4 shows the three-level flying capacitor inverter. The general concept of operation is that each flying capacitor is charged to one-half of the dc voltage and can be connected in series with the phase to add or subtract this voltage.

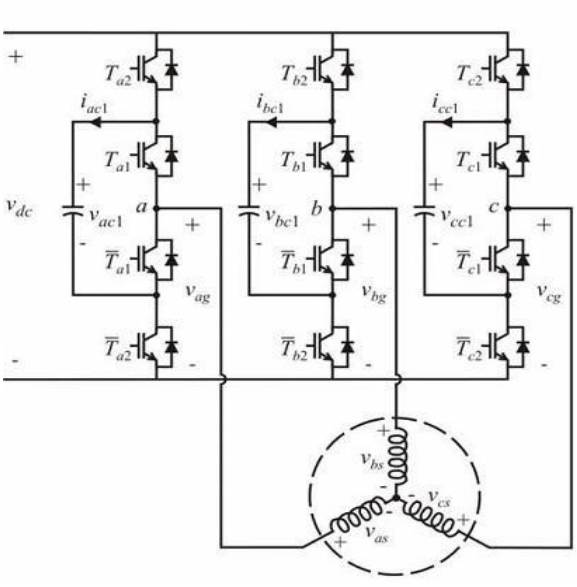

Figure 4 Three level flying capacitor topology

1.2 MODELING and CONTROL of MLI

A scheme for finite state model predictive control-fed five-level cascaded MLI has been established. This proposed method uses 19 voltage vectors out of totally 125 voltage vectors of the cascaded MLI. Since this inverter has many switches and reduces the average switching frequency which is a matter of great importance for high voltage applications, as they contribute to significant switching losses. Two schemes of Finite State Model Predictive Control (FSMPC) are proposed i.e. FSMPC-1 employing the current control of the cascaded MLI with 19 voltage vectors and FSMPC-2 aiming the control of inverter load current as well as reducing the average switching frequency using 19 vectors. The performance of the proposed schemes is compared with a conventional 61 voltage vector scheme of the cascaded inverter. The results

show that both the proposed schemes perform well for steady state and dynamic operating conditions (Razia Sultana et al. 2016).

A novel space-vector current-control strategy has been employed to maintain the desired number of voltage levels based on load current, in a newer five-level single-phase voltage source inverter. With the proper selection of the redundant inverter switching states, the deviation in neutral- point voltage is considerably minimized (Ammar Masaoud et al. 2014). To balance conduction losses in full-bridge and Multi-Level Cascade Inverters, a switching method has been proposed, and its effectiveness and validity have been examined (Hosseini Aghdam et al. 2008).

2.1 PWM STRATEGY

In 1999, Tolbert & Habetler found that the implementation of the existing control strategies for a DC-MLI impinges on the switch utilization, thus increasing the losses. In 2000, Mcgrath & Holmes obtained an analytical solution for PWM techniques and found that the harmonic components produced by APOD technique in DC-MLIs produce the same effect as that of the PSC in CHBMLIs. In 2001, Calais et al. reviewed the MCPWM methods. A few regular sampled control strategies apposite for MLIs are also available based on either solving complex equations or evolutionary computing. A general Space Vector PWM (SVPWM) method for MLI based on a generalization of dwell-times calculation has been achieved (Trabelsi et al. 2012).

The presented scheme is developed for CHBMLI in which the sectors are defined by two parameters serving for easy calculation of dwell- times. This paper introduced a new switching scheme for a new topology of MLI with reduced number of switches for interfacing fuel-cell with the grid. An unipolar PWM technique has been coined for the switching of MLI topology with reduced number of switches for interfacing fuel-cell with the grid (Kumar & Pal 2014). A level shifted PWM control string source-based MLI topology has been formulated. This topology works with the innovative PWM strategy in achieving the targeted output. In this case, the DC source is connected with controlled switch by level shifted PWM technique, which is connected across an anti-parallel diode and such types of controlled sources are placed in series (Subbarao et al. 2014).

The Third Harmonic Injection PWM (THIPWM) strategy of a seven-level Uniform Step Cascaded H-Bridge Asymmetrical Inverter (USCHBAI) has been detailed with the comparison of SPWM strategy (Taleb et al. 2015).

A single-phase modified H-Bridge seven-level inverter structure has been schemed suitable for stand-alone PV systems. Selective Harmonic Elimination (SHE) technique involving Newton-Raphson method has been used to solve the non-linear equations from the switching angles (Krismadinata et al. 2013). A Bacterial Foraging Algorithm (BFA) method is proposed for switching angle selection in PWM inverter. The problem of voltage harmonic elimination together with output voltage regulation is drafted as an optimization task and the solution is sought through the proposed method. Extensive simulations are carried out using MATLAB/SIMULINK environment under various operating points with different switching pulses per half cycle. To demonstrate the superiority of the proposed method, BFA results are compared with other existing techniques such as Genetic Algorithm (GA) and Particle Swarm Optimization (PSO) method (Sudhakar Babu et al. 2015).

A generalized Hybrid single-carrier sinusoidal modulation control for cascaded MLIs has been devised. This scheme combines the features of single-carrier sinusoidal and fundamental frequency modulations. The important characteristic of this modulation is better harmonic performance and reduced switching losses (Govindaraju & Baskaran 2011).

3.1 PULSE WIDTH MODULATION (PWM) STRATEGIES

Mainly the power electronic converters are operated in the “switched mode” state. Thus, the switches within the converter are always in either one of the two states - turned off or turned on condition. To control the flow of power in the converter, the switches alternate between these two states (i.e. on and off). This happens rapidly so that the inductors and capacitors at the input and output averages or filters the switched signal. This process is called Pulse Width Modulation (PWM), since the desired average value is controlled by modulating the width of the pulses.

For maximum attenuation of the switching component, the switch frequency *fc* should be higher than the frequency of the desired fundamental AC component.

This PWM can be realized using different techniques such as carrier based PWM, PWM with harmonics minimization and space vector PWM. The carrier PWM can be natural PWM, symmetric PWM and asymmetric PWM.

The most simple and well known PWM technique is the sinusoidal PWM. This technique uses a controller which determines the voltage reference of the inverter from the error between the measured current and its reference. This

reference voltage is then compared with a triangular carrier signal. The output of this comparison decides the switching function of the VSI. The choice of the ratio between the frequency of the reference signal and the frequency of the carrier signal is very important in the case of symmetric and periodic reference. As a consequence, in the case of sinusoidal reference, the ratio between the two frequencies must be integer to synchronize the carrier with the reference. It is preferable that the carrier frequency be odd to conserve the reference symmetry. In all cases this ratio must be sufficiently high to ensure the fast switching and to take the switching harmonics away from the fundamental produced by the inverter.

3.2 SELECTIVE HARMONIC ELIMINATION (SHE) METHOD

In this technique, the switching angles are computed offline and are calculated in such a way that arbitrary harmonics, usually low order, up to (a-1) harmonics are eliminated, where "a" is the number of switching angles. The switching angles must be lower than 90°. If the angles are larger than 90° than the actual output signal would not be achieved. Higher order harmonics can be filtered using additional filters between the inverter and the load.

This modulation operates at a very low switching frequency to reduce the semiconductor losses. To minimize harmonic distortion low frequency harmonics are chosen for elimination by properly selecting angles among different level inverters.

3.3 SPACE VECTOR MODULATION (SVM) TECHNIQUE

Each multilevel inverter has several switching states which generate different voltage vectors and can be used to modulate the reference. The reference signal is generated from its closest signals. SVM identifies each switching state of a multilevel inverter as a point in complex space. Then reference phasor rotating in the plane at the fundamental frequency is sampled within each switching period and the nearest three inverter switched states are selected with duty cycles calculated to achieve the same volt-second average as the sampled reference phasor. This directly controls the inverter line to line voltages and only implicitly develops the phase leg voltages (Massoud et al 2007a, Massoud et al 2007b, Massoud et al 2008).

Principle of Space Vector PWM

a. Treats the sinusoidal voltage as a constant amplitude vector rotating at constant frequency

b. This PWM technique approximates the reference voltage Vref by a combination of the eight switching patterns (V0 to V7)

c. Coordinate Transformation (abc reference frame to the stationary d-q frame): A three-phase voltage vector is transformed into a vector in the stationary d-q coordinate frame which represents the spatial vector sum of the three-phase voltage

d. The vectors (V1 to V6) divide the plane into six sectors (each sector: 60 degrees)

e. Vref is generated by two adjacent non-zero vectors and two zero vectors

3.4 CARRIER BASED PULSE WIDTH MODULATION TECHNIQUES

The carrier frequency is the same as the switching frequency. If the modulation were reduced to zero or a DC quantity, then the PWM spectrum would consist of the carrier and its harmonics alone. As the amplitude of the modulating waveform is increased, sidebands appear and increase in amplitude on either side of the carrier and its harmonics. As the frequency of the modulating waveform is increased, the sidebands spread away from the central carrier frequency.

The carrier frequency should be synchronous, that is an integer multiple of the fundamental frequency, if the pulse number is low (say $N < 21$). An odd multiple guarantees half and quarter wave symmetry and therefore no even harmonics occur in the carrier spectrum.

If the same carrier signal is used to generate all three phase leg PWM signals in a three phase inverter, the carrier spectral terms in the phase leg signals will also be identical. Thus the carrier spectral terms (but not the carrier sidebands or modulating terms) will be cancelled in the phase to phase waveforms. This is true regardless of the pulse number N. Although the phase relationship between the modulating and carrier waveforms can be arbitrary, it is suggested that the slopes of the triangular carrier and modulating waveform, if sinusoidal in character, should be of the opposite polarity at the coincident zero crossings, especially for low N. This has practical implementation advantages of preserving the

accuracy of the edges in analog implementations and easing the transition between different pulse numbers in systems where this may change during operation. Additionally this 180 degree phase difference (phase relative to the carrier period) results in the minimization of the harmonic losses in an inductive load. This 180 degree out-of-phase relationship can only exist for odd N. Further, the reduction in harmonic losses due to a specific phase relationship between modulating function and carrier is only significant for odd N. To achieve this phase relationship in a three phase inverter for all three phases requires N to be an odd multiple of three (N = 3, 9, 15, 21 . . .), if the same carrier is to be used for all three phases to achieve carrier cancellation in the phase-phase output.

In a multi-level converter with an integer pulse number, only one carrier can ever meet this requirement, as the other carriers are usually phase shifted relative to it. However, if a non-integer synchronous pulse number is used in a multilevel converter, this phase relationship once again becomes valid.

(i) Carrier Switching Frequency Sub Harmonic Pulse Width Modulation (CSFSHPWM)

For an m-level inverter, this technique uses (m-1) triangular carrier signals with the same frequency (fc), same peak-to-peak amplitude (Ac) and same phase which are disposed such that the bands they occupy are contiguous. The sinusoidal modulation waveform is centered in the middle of the carrier set and is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on and if the reference is less than a carrier signal, then the active device corresponding to that carrier is switched off. This method is also known as sinusoidal pulse width modulation (SPWM). In multilevel inverters, the amplitude modulation index ma and the frequency ratio mf are defined as given as

$$ma=Am/(m-1).Ac \quad (3.1)$$

$$mf=fc/fm \quad (3.2)$$

The CSFSHPWM control method along with carrier and modulating wave forms are shown in Figure 5.

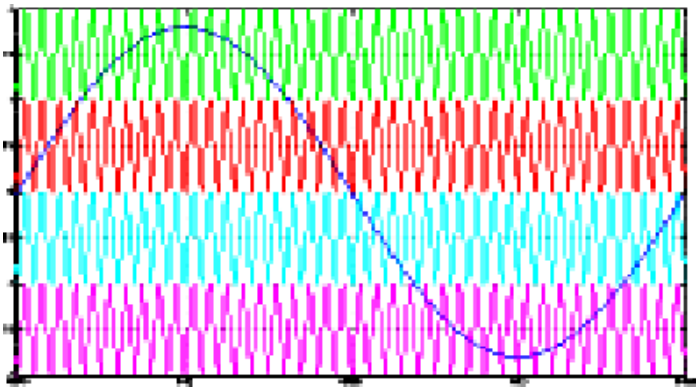

Figure 5 Waveform of CSFSHPWM

(ii) Carrier Switching Frequency Optimal Pulse Width Modulation (CSF-O-PWM)

Another carrier based method for multilevel applications is termed as switching frequency optimal PWM (SFO-PWM) and it is similar to SH-PWM except that a zero sequence (triplen harmonic) voltage is added to each of the carrier waveforms. This method takes the instantaneous average of the maximum and minimum of the three reference voltages (Va∗, Vb∗ and Vc∗) and subtracts this value from each of the individual reference voltages to obtain the modulation waveforms. The CSF-O-PWM control method along with carrier and modulating wave forms are shown in Figure.

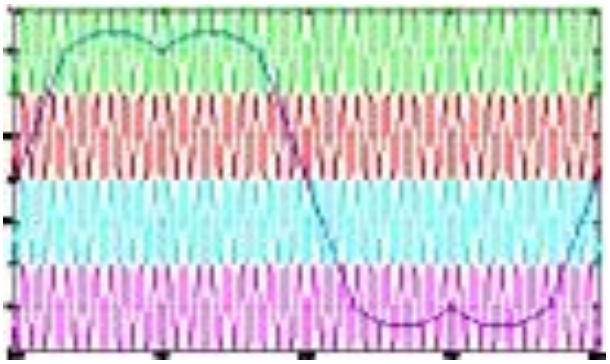

Figure 6 Waveform of CSF-O-PWM

(iii) Variable Switching Frequency Multi-Carrier Sub Harmonic Pulse Width Modulation (VSFMC-SH-PWM)

In this technique for a multi-level inverter, (m-1) carrier signals with different switching frequencies are used with sinusoidal reference signals.

(iv) Variable Switching Frequency Multicarrier Optimal Pulse Width Modulation (VSFMC-O-PWM)

For a multilevel inverter, if the levels are 'm' there will be '(m-1)' carrier set with variable switching frequency multi carrier pulse width modulation.

(v) Carrier Phase Shifted Sub Harmonic PWM (CPS-SHPWM)

In the phase shifted multicarrier modulation, all triangular carriers have same frequency and the same peak to peak amplitude but there is a phase shift between any two adjacent carrier waves. Gate signals are generated by comparing the modulating wave with the carrier waves. In this PWM method the equivalent switching frequency of the whole converter is (m-1) times the switching frequency of each power device. This means CPS-PWM can achieve a high equivalent switching frequency effect at very low real device switching frequency which is most useful in high power applications.

(vi) Alternate Phase Opposition Disposition (APOD) PWM

In this modulation, alternative carrier waves are phase displaced by 180°. The APOD-PWM control method along with carrier and modulating wave forms are shown in Figur. The rules for APOD method,

i) The converter switches to + Vdc / 2 when the reference is greater than all the carrier waveforms.

ii) The converter switches to Vdc / 4 when the reference is less than the uppermost carrier waveform and greater than all other carriers.

iii) The converter switches to 0 when the reference is less than the two uppermost carrier waveform and greater than two lowermost carriers.

iv) The converter switches to - Vdc / 4 when the reference is greater than the lowermost carrier waveform and lesser than all other carriers.

v) The converter switches to - Vdc / 2 when the reference is lesser than all the carrier waveforms.

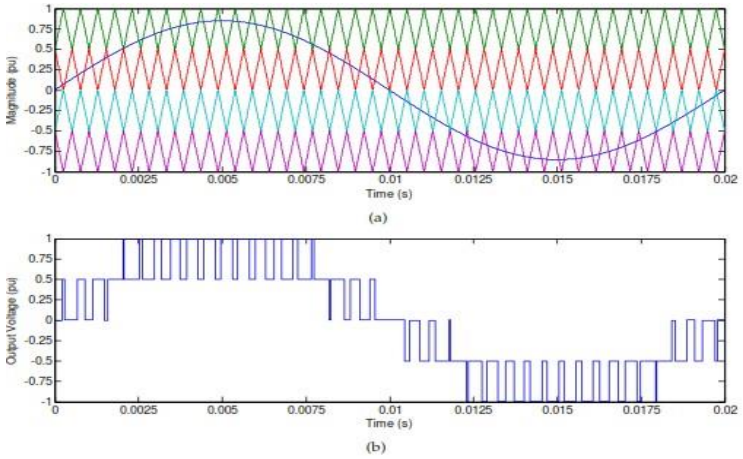

Figure 7 APOD-PWM technique: a) Reference and carrier signals, b) Output phase voltage waveform

(vii) Phase Opposition Disposition PWM (POD-PWM)

In POD-PWM control technique, the carrier signals which are above the zero level are in phase and the carrier signals which are below the zero level are in phase of each other and out of phase by 180° to above signals which is shown in Figure 3.4.

The rules for the phase opposition disposition method for a multilevel inverter are

i) The converter is switched to + Vdc / 2 when the reference is greater than both upper carrier waveforms.

ii) The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.

iii) The converter is switched to - Vdc / 2 when the reference is less than both carrier waveforms.

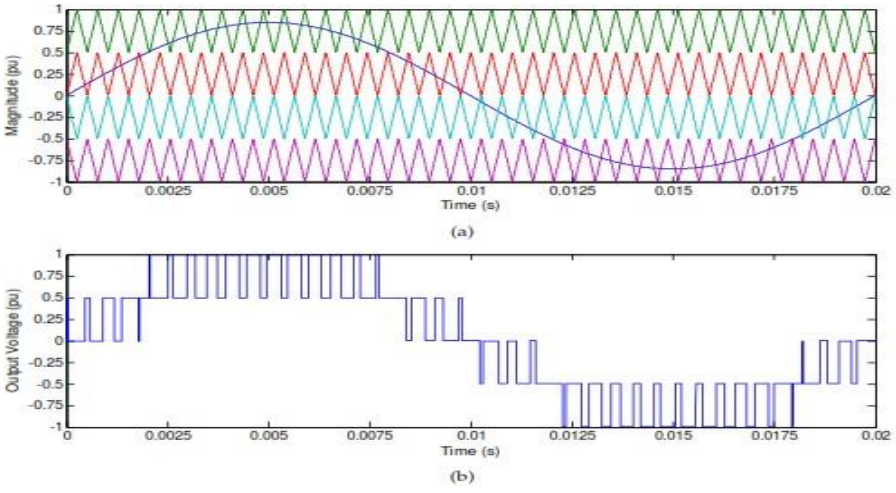

Figure 7 POD-PWM technique: a) Reference and carrier signals,b) Output phase voltage waveform

(viii) Phase Disposition PWM (PD-PWM)

In PD-PWM modulation, all the carrier signals are in phase. In this method, the major feature of the phase voltage spectrum is the significant first carrier harmonic. This feature gives the PD-PWM excellent line voltage performance, since this carrier harmonic is a common-mode component across the phase voltages of a three phase inverter and therefore cancels in the output line voltage reducing harmonics in line voltage. This technique is similar to APOD except the carriers are in phase as shown in Figure 3.5.

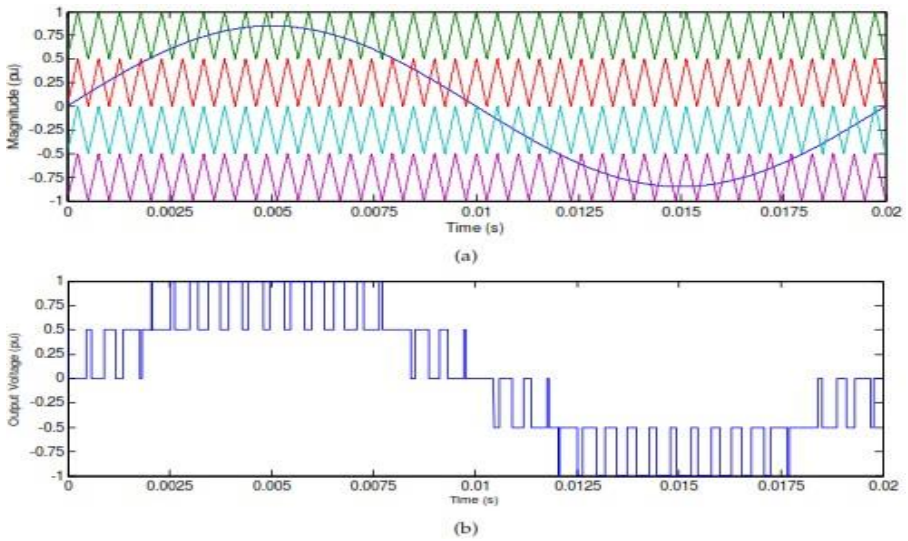

Figure 8 PD-PWM technique: a) Reference and carrier signals,
b) Output phase voltage waveform

4.1 ANALYSIS AND DESIGN OF 7 - LEVEL CASCADED INVERTER WITH 6 SWITCHES

Multilevel inverters (MLI) are being considered as the most popular method to synthesize almost sinusoidal waveforms using multi steps. Out of three conventional topologies cascaded H- bridge type of MLIs with different dc sources are proven to be more reliable in generating higher voltage with comparatively less harmonics due to its modular nature. These types of MLIs are also very suitable for solar applications as the separate dc sources requirement is naturally available. However, there are certain drawbacks of these MLIs such as the use of large number of switches and the related gate drive circuit design as required by the corresponding semiconductor switches which create more complexity in electrical and mechanical design of the inverters.

4.1.1 PROPOSED 7-LEVEL CONFIGURATION

The design of cascaded MLIs can be made simple by designing a simple gate pulse generation scheme. The cascaded MLIs use bridges cascaded with each other. For a five level inverter, two bridges are required, for a seven level inverter three bridges are required and for a nine level inverter four bridges are required and so on. One bridge consists of four semiconductor switches, so the number of switches increase with the level and voltage steps. Hence the switching losses and the cost of the MLIs also increase accordingly. Therefore, an initiative is taken to reduce the number of semiconductor switches and hence the cost of MLI and a simpler switching technique is developed to control the MLIs. In this section, a method is developed to reduce the switches for a seven level inverter by using 6 switches.

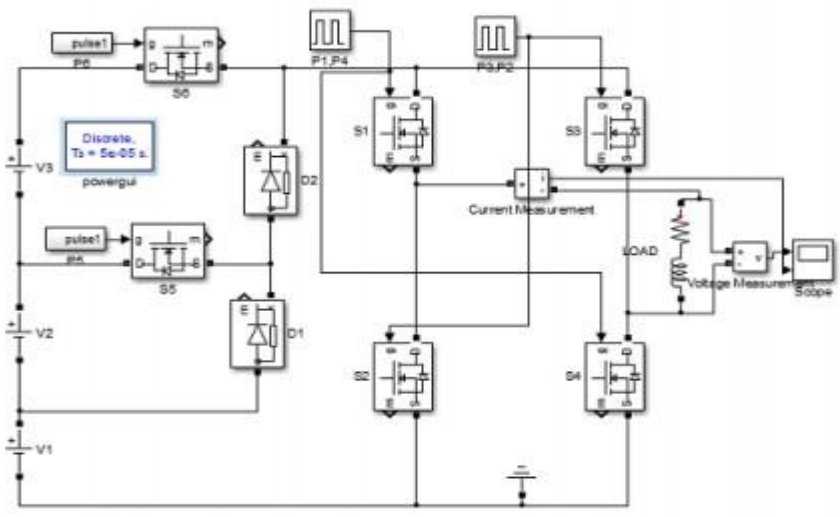

Figure 9 Seven Level Inverter with Six Switches

In this topology six MOSFETS are used. Four MOSFETS are used in H-bridge for changing the polarity and two MOSFETS are used for level generation. Two diodes are used to generate voltage ±V. The switching scheme is given in Table-1. It has 7 output voltage levels that is 3V, 2V, V, 0, -V,-2V, -3V. For 3V output voltage, MOSFETS S1, S4 & S7 are switched on and others are switched off. For 2V output voltage, MOSFETS S1, S4 & S6 are switched on and others are switched off. For V output voltage, two MOSFETS S1and S4 are only switched on and others are switched off. For 0 output voltage all the MOSFETS are switched off . For -V output voltage, two MOSFETS S2, S3 are only switched on and others are switched off. For -2V output voltage, MOSFETS S2, S3 & S6 are switched on and others are switched off. For -3V output voltage, MOSFETS S2, S3 & S7 are switched on and others are switched off. It can be observed that the switching devices for the proposed seven level seven switch inverter at the time of conduction are three and for seven level six switch inverter is 2 or 3. So switching loss is greatly reduced. Table 4.1 represents the switching scheme of the proposed topology

Table 1 Switching scheme for 7-level 6-switch topology

SL no.	S1	S2	S3	S4	S5	S6	Output voltage
1	OFF	OFF	ON	OFF	ON	OFF	+Vdc
2	OFF	ON	OFF	OFF	ON	OFF	+2Vdc
3	ON	OFF	OFF	OFF	ON	OFF	+3Vdc
4	OFF	OFF	OFF	OFF	OFF	ON	0
5	ON	OFF	OFF	ON	OFF	OFF	−Vdc
6	OFF	ON	OFF	ON	OFF	OFF	−2Vdc
7	OFF	OFF	ON	ON	OFF	OFF	−3Vdc

4.2 PWM GENERATION

The pulse generation is essential in order to trigger the switches with appropriate pulse pattern to produce the desired 7-level output. It is inevitable to analyse which PWM suits the new topology. The simplest PWM technique is the carrier-based PWM (CBPWM) technique. It can be further categorized into level and phase shifting CBPWMs, respectively. Since the phase shifting CBPWM yields more harmonics comparatively, the level shifting CBPWM is preferred over it.

The reference signal comparing with carrier generating pulse which is then modified feeding to logic gates in order to get the required pattern to trigger the switches at the proper instant. For examples switches S1 needs to have a pulse so as to obtain +Vdc and −3Vdc and S2 requires +2Vdc and −2Vdc. S3 conducts +3Vdc and −Vdc. Also, switches S5 and S4 conduct positive and negative half cycles, respectively. Figure 4.2 represents the CBPWM technique proposed in this work.

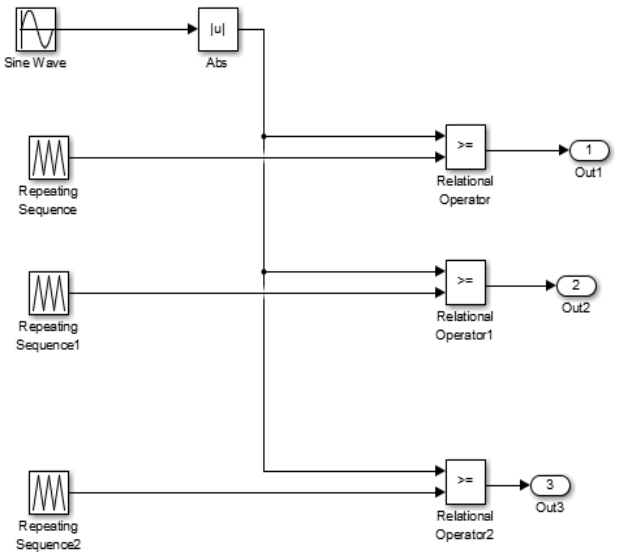

Figure 11 PWM generation scheme

5.1 EXPERIMENTAL RESULTS

The simulation result and THD of the proposed topology is shown below. Here the input voltage is about 77V and the resistive load is taken. Figure 4.3 shows the output voltage waveform of the 7 level symmetrical CHB configuration. The magnitude of the voltage is is about 230 volts. The total harmonic distortion (THD) for the output voltage wave form is measured 17.98% and is shown in figure 4.4.

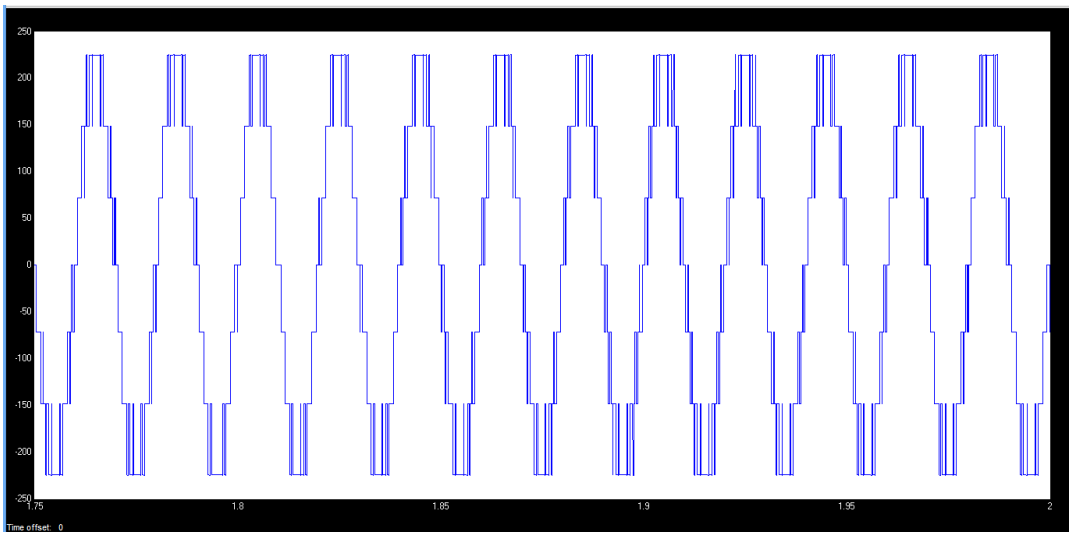

Figure 12 Output Voltage

Table 2 : THD results obtained for conventional & modified 7 level inverter configurations

Symmetric conventional cascaded 7-level MLI	**Proposed (7-level, 6 switches)**
24.26	17.98

Simulation results presented in table 2 (reveals that the total harmonic distortion is reduced to 17.98%)

Table 3 Voltage stress in proposed topology across switches

Parameter	**Conventional CMLI**	**Proposed topology**
Voltage stress	5V (All switches)	3.33V (S3) 13.3V (S2) 23.3V (S1)

Table 4 Comparison of proposed 7-level with other topology

Inbuilt structure	**Flying capacitor**	**Diode clamped**	**Cascaded 7-level**	**7-level, 6 switches**
No. of capacitors	14	6	—	—
No. of diodes	—	≥8	—	—
No. of switches	10	10	12	**6**
No. of dc sources	—	—	3	**4**

6.1 CONCLUSION

In this chapter, the overall conclusion along with the suggestions for future work is presented. In recent days MLI has drawn large interest in high power industry. They present a latest set of aspects to facilitate and utilized in reactive power compensation. The unique arrangement of multilevel voltage source inverters allow them to achieve high voltages with the low harmonics not including the utilization of transformers or series connected synchronized switching devices.

The Diode clamped, Flying capacitor, Cascaded H-bridge inverter are the three main different multilevel inverter structures which are used in industrial applications with separate dc sources. In flying capacitor and diode-clamped inverter there is a problem of capacitor voltage balancing and this problem is overcame by cascaded H-bridge inverter. However, the main drawback in Conventional cascaded is that when levels are increasing it requires more number of semiconductor switches. As a result some alternations are to be made in order to reduce the size and switch of the inverter.

A single phase 7 level reduced switch MLI topology is introduced and its various modes of operation are studied. A novel modulation approach is presented and utilized in the proposed topology. From the results, it is evident that this proposed system reduces switching losses with less THD. Thus, the overall cost reduction and effective reduction of total harmonics distortion is achieved.

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