International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 10 Issue: 08 | Aug 2023 www.irjet.net p-ISSN: 2395-0072

Design and Implementation of a Dual Stage Operational Amplifier

Saumya Mishra[1]

[1]*M.Tech Scholar, Department of ECE, Indira Gandhi Delhi Technical University for Women, Delhi, India*

Abstract - *In this paper, we have used Miller Compensation Technique to amplify the gain of a 2-stage Op-Amp. Below mentioned procedure follows the technique of developing a theoretical design followed by carrying out a simulation process by presuming some values for a particular operational situation (we've taken help of LTspice for that). The resultant CMOS Op-Amp was tested in a simulated parameter of VDD=1.8V in order to test the accuracy of theoretically concluded numbers. The CMOS technology used was 180nm with the help of LTspice tool. In the above mentioned environment; the following key factors were taken into observation: gain margin, phase margin, Output Power dissipation, output Noise and unity gain bandwidth.*

***Key Words*: Gain Margin, Phase Margin, Gain Bandwidth, Miller Compensation**

1.INTRODUCTION

The road for the expanding market of sophisticated electronics applications in mobiles and sensor applications was created by the recent development in CMOS scaling. The integration of complicated functionalities on a single chip (such as a SOC (System on Chip)), along with ongoing increases in operating speed and decreases in system power consumption, is what drives scaling.[1]

Transistor dimensions are getting smaller as a result of improvements in CMOS manufacturing techniques [1]. The advantages of adopting smaller dimension transistors typically result in lower power consumption, smaller device sizes, and higher performance at high frequencies. Transconductance and output resistance, two crucial analog properties of a transistor, will decrease as a result of the use of tiny CMOS technologies.

Analog circuits frequently employ operational amplifiers (op-amps) with negative feedback to create amplifiers with a variety of desirable characteristics, including steady gain, good linearity, and low output impedance [2]. However, the negative feedback's significant phase lag causes a stability (STB) problem. The STB of the amplifier has been improved using a variety of approaches [3]-[5].

The gain of a single-stage opamp is derived by multiplying transconductance with the output impedance. The gain and other crucial parameters such as output swing, gain bandwidth, etc. offered by various topologies of a single-stage opamp such as Single stage Common Source Amplifier, Cascode Amplifier, etc. are insufficient for several applications. For instance, a modern op-amp must be able to deliver single ended output swings of up to 0.8 V while operating with input voltages as low as 0.9 V. When this happens, we turn to "two-stage" operational amplifiers, in which the first stage is responsible for providing high gain and the second stage provides large swings. A two-stage arrangement isolates the gain and swing requirements as opposed to cascode op amps [7].

There has been multiple research that produced a >140dB gain using the multi-stage amplifier technology, which has been around for a while. The stability of the opamps may be compromised by the close spacing of the poles caused by cascading many stages.

when we observe the second order system's time response with step input, we see that larger phase margin results in reduced oscillations in the output signal[12][13]. we prefer to have ringing as minimum as possible. A minimum of 45 degrees phase margin is desirable and a 60 degree PM is mostly preferred [12].

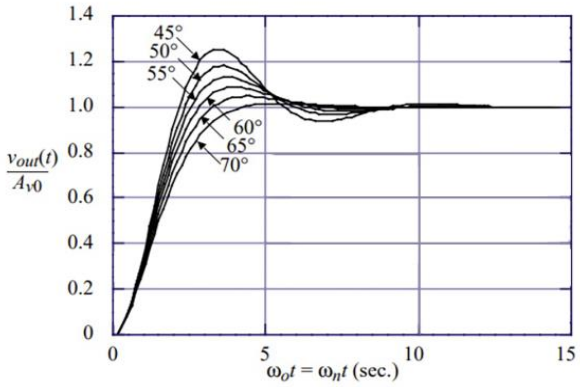

Fig -1: Time Response depiction of a second order System corresponding to different Phase Margins

Frequency correction must be carried out to improvise the stability and provide proper transient step responsiveness. Miller and cascode compensations are well-known approaches. Miller compensation is well known for its ability to increase bandwidth via pole splitting phenomenon. We will be employing miller compensation in our dual-stage opamp and observe the results with high gain and improved phase margin. Though miller compensation is used to enhance the gain bandwidth product, complexity has also risen as a result of interims of extra amplifier stages and capacitors. The stability is compromised by the right half

zero (RHP) that is introduced by Miller compensating with a nulling resistor.[6]

The paper has been organized as follows, section-2 deals with the theoretical description and Small signal dynamics of dual-stage opamp when it is uncompensated as well as with miller compensation. Section-3 describes the design procedure of dual stage opamp and section-4 summarizes the prototype results.

2. SMALL SIGNAL DESCRIPTION

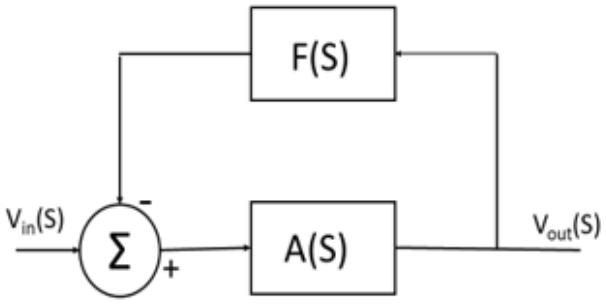

Fig -2: Block Diagram showing Negative Feedback Configuration

Opamps are usually configured in negative feedback mode as can be seen in above Fig. 1 Here A(s) is the gain of Amplifier , F (s) is the transfer function describing external feedback from the output of opamp to the input.

The loop gain L(S) is given by ,

$$L(s) = -A(s)F(s) \quad (1)$$

And, $$\frac{v_{out}(s)}{v_{in}(S)} = \frac{A(s)}{1+A(s)F(s)} \quad (2)$$

In order to have a stable feedback system, we need to have,

$$Arg[-A(j\omega_{0dB})F(j\omega_{0dB})] = Arg[L(j\omega_{0dB})] > 0° \quad (3)$$

Where, ω_{0dB} is,

$$|A(j\omega_{0dB})F(j\omega_{0dB})| = |L(j\omega_{0dB})| = 1 \quad (4)$$

A close loop system's time response can be used to understand the significance of good stability that is acquired with sufficient phase margin. Because it has been found that a larger phase margin reduces output signal ringing. Phase margins of at least 45 degrees are preferred, however in most cases, 60 degrees is recommended.

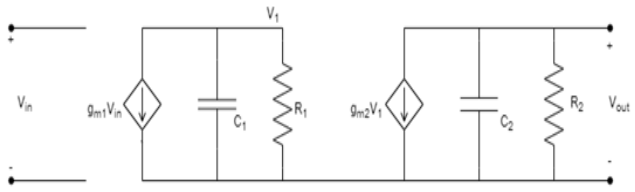

Fig -3: Small Signal Diagram of an Uncompensated Opamp

Fig.3 shows the small signal model of an uncompensated Opamp . The location of two poles of this model is given by,

$$P_1' = \frac{-1}{R_1C_1} \quad (5)$$

and,

$$P_2' = \frac{-1}{R_2C_2} \quad (6)$$

where C_1 and C_2 are the capacitances to ground observed from the first and second stages, respectively, and R_1 and R_2 are the resistances to ground as seen from the output of the first and second stages, respectively.

It was found that the phase margin observed is significantly less than 45 degrees when an open loop frequency response of negative feedback is computed using the mentioned opamp, even when considering the worst case scenario of stability (considering F(S) = 1). This suggests the need for compensation in the dual stage operational amplifier prior to it's utilization in a closed loop configuration[12].

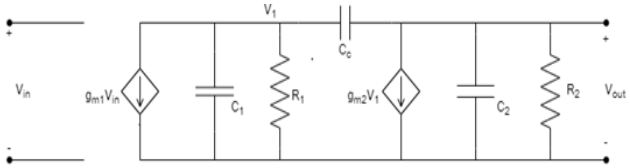

Fig -4: Small Signal Diagram of a Miller Compensated Dual Stage Opamp

Fig -4: Small Signal Diagram of a Miller Compensated Dual Stage Opamp. The location of Poles and Zeroes obtained by solving the small signal model equations of miller compensated dual stage operational amplifiers are-

$$P_1 = \frac{-1}{g_{m2}R_1R_2C_C} \quad (7)$$

$$P_2 = \frac{-g_{m2}}{C_c} \quad (8)$$

$$Z = \frac{g_{m2}}{C_c} \quad (9)$$

In this situation, the Miller effect results in making one pole dominant while weakening the other. Meaning, while one pole increases in frequency, the other decreases in

frequency. The Miller effect is frequently called as Miller compensation when this opposite motion (also known as pole splitting) is a required outcome [13].

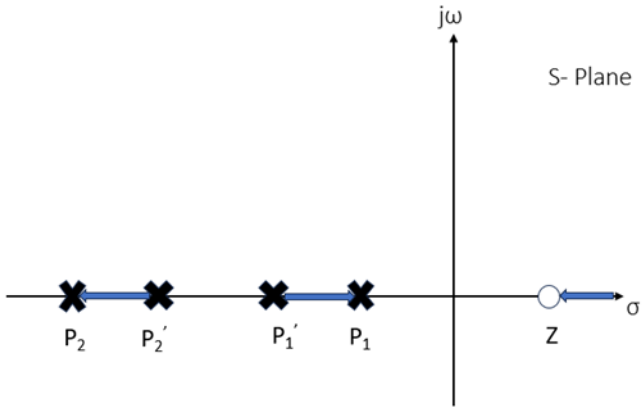

Fig -5: Pole -Zero Plot showing Miller effect on Opamp

In Fig. 5. the shift in the pole positions is depicted as they transition from their uncompensated locations to the compensated positions on the complex frequency plane. A very popular technique of using a nulling resistor have been developed to overcome the drawback of the RHP zero introduced by the Miller effect [12].

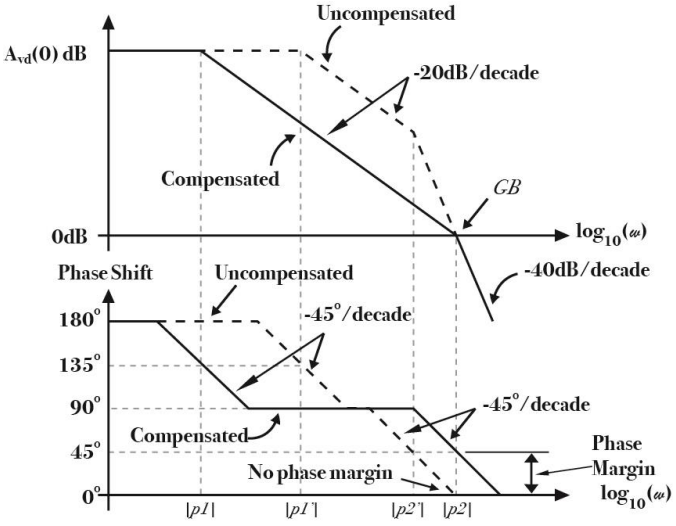

Fig -6: Shifting in Bode Plot from Uncompensated to Compensated System

Fig. 5. explains the shifting of bode plot from an uncompensated system to compensated system[12].

3. SCHEMATIC & DESIGN EQUATIONS OF DUAL STAGE OPERATIONAL AMPLIFIER

Table 1. shows the required opamp specification considering which the designing is done. Table 2. depicts the process parameters for CMOS 0.18um technology used in calculation of CMOS design parameters for designing a dual stage opamp.

Table -1: Design specification required to be met by opamp

Parameters	Conditions
Supply Voltage	1.8 V
Load Capacitance (C_L)	4pf
DC Gain	≥ 60 dB
Gain Bandwidth	≥ 30 MHz
I_{Ref}	50µA
ICMR(+)	1.6V
ICMR(-)	0.8V

Step 1) obtain the value of miller capacitance C_C.

$$C_C \geq 0.22C_L \quad (10)$$

From here we get the Value of $C_c = 0.88pF$

Let's assume $C_c = 1pF$

Step 2) Slew Rate, $SR = \frac{I_5}{C_c}$ (11)

Obtained Value is 33.33 $\frac{V}{\mu sec}$

Step 3) Designing of M1 & M2

Transconductance of M1 is given by-

$$g_{m_1} = GBW \times C_C \times 2\pi \quad (12)$$

By putting the values, we are getting $g_{m_1} = 281.74\mu$

Let's assume $g_m = 290\mu$

$$\left(\frac{w}{L}\right)_1 = \frac{g_{m1}^2}{\mu_n c_{ox}(2I_{D_1})} \quad (13)$$

Therefore, $\left(\frac{w}{L}\right)_1$ =5.606

Let's assume $\left(\frac{w}{L}\right)_1 = 6$

Since, $\left(\frac{w}{L}\right)_1 = \left(\frac{w}{L}\right)_2$ (14)

Therefore, $\left(\frac{w}{L}\right)_2 = 6$

Step 4) Designing of M3 & M4

$$V_{D1} = V_{DD} - \left[\sqrt{\frac{2I_3}{\beta_3}} + |V_{T3}|\right] \quad (15)$$

$$ICMR^+ \leq \left[V_{DD} - \left(\sqrt{\frac{2I_3}{\beta_3}} + |V_{T3}|\right)\right] + V_{T1_{min}} \quad (16)$$

$$\left(\frac{W}{L}\right)_3 = \frac{2I_{D3}}{\mu_p C_{ox}\left[V_{DD} - ICMR^+ - V_{T3_{max}} + V_{T1_{min}}\right]^2} \quad (17)$$

By putting corresponding values and solving above equations, we get

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 12 \text{ (approx.)} \quad (18)$$

Step 5) Designing of M5

$$V_{Dsat} \geq ICMR^- - \sqrt{\frac{2I_{D1}}{\beta_1}} - V_{T1max} \quad (19)$$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_{D5}}{\mu_n C_{ox}(V_{Dsat})^2} \quad (20)$$

Table -2: Process Parameter Values taken for Designing of Opamp

Process Parameters	NMOS	PMOS
V_{TH}(V)	0.37	-0.39
μ(cm²/V-sec)	273.809	115.689
T_{OX}(m)	4.10E-09	4.10E-09

By solving above equation we get, $\left(\frac{W}{L}\right)_5 = 12 \text{ (approx.)}$

Step 6) Designing of M6 & M7

For designing M6, first we will find trasconductance of M6,

$$g_{m6} \geq 10 g_{m1} \quad (21)$$

$$g_{m4} = \sqrt{\mu_p C_{ox}\left(\frac{W}{L}\right)_4 2I_{D4}} \quad (22)$$

$$\left(\frac{W}{L}\right)_6 = \frac{g_{m6}}{g_{m4}}\left(\frac{W}{L}\right)_4 \quad (23)$$

By putting corresponding values and solving above equation, we get,

$$\left(\frac{W}{L}\right)_6 = 136$$

For M7, $\left(\frac{W}{L}\right)_7 = \frac{I_7}{I_5}\left(\frac{W}{L}\right)_5$ (24)

Table -3: Obtained Aspect Ratio Values by Calculation

Aspect Ratios	Proposed Values
$(W/L)_{M1,M2}$	3μm/0.52μm
$(W/L)_{M3,M4}$	7μm/0.52μm
$(W/L)_{M5}$	12μm/1μm
$(W/L)_{M6}$	71μm/0.52μm
$(W/L)_{M7}$	69μm/1μm
$(W/L)_{M8}$	12μm/1μm

2. OUR DESIGN AND OBTAINED RESULTS

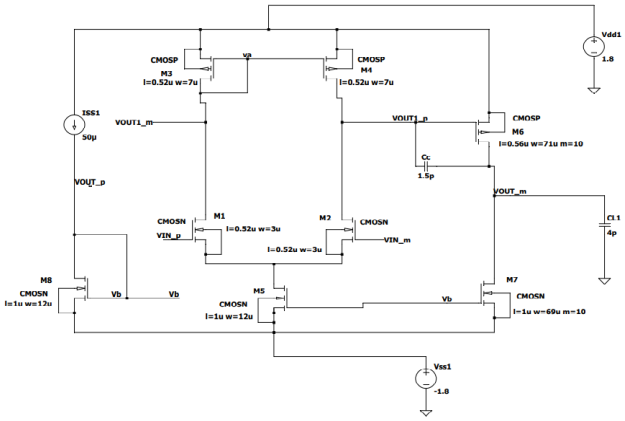

Fig -7: Dual Stage Operational Amplifier Schematic

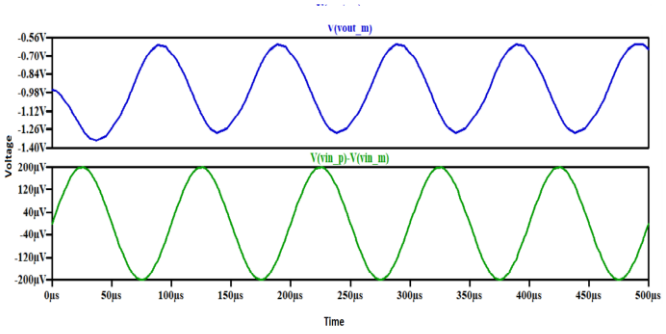

Fig -8: Transient Response

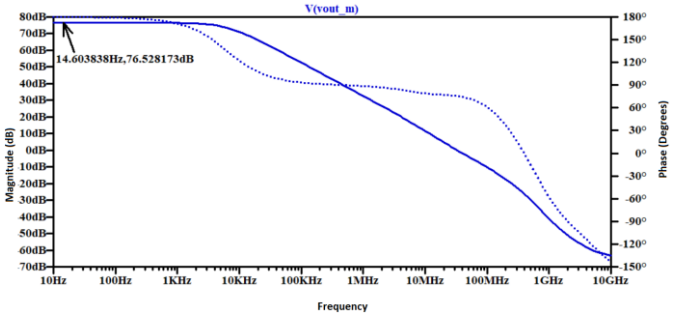

Fig -9: AC Analysis Response

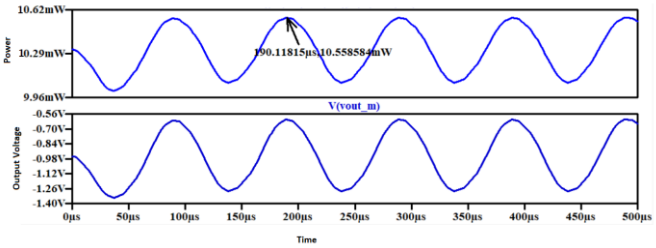

Fig -10: Power Dissipation in the Output

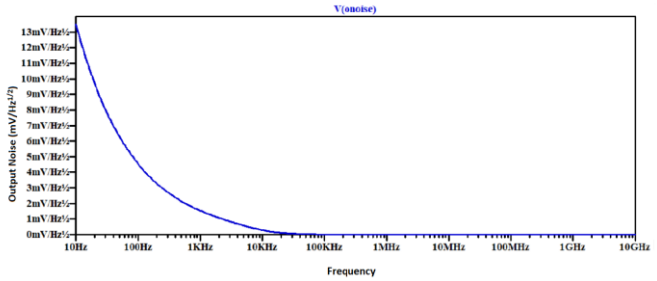

Fig -11: Output Noise

Table -4: Obtained Values of Designed Opamp

S.NO.	Name of Parameter	Observed Values
1.	Gain	76.34 dB
2.	Phase Margin	72.80 Degrees
3.	ain Bandwidth Product(MHz)	42.65 MHz42.65 MHz
4.	Power Dessipation	10.56 mW

3. CONCLUSIONS

The Paper reviews and highlights drawbacks of uncompensated two stage opamp design. It signifies the improvement brought out in two stage opamp design by using miller compensation and implements miller compensation in designing two stage opamp highlighting improved parameters. The aspect ratio values obtained from calculation shows better DC gain, Phase Margin and Gain Bandwidth Product of the implemented dual stage operational amplifier.

REFERENCES

[1] H. Iwai, "CMOS Scaling Towards Its Limits", *Solid-State and Integrated Circuit Technology 5th International Conference*, pp. 31-34, October 1998.

[2] H. Ju and M. Lee, "A Hybrid Miller-Cascode Compensation for Fast Settling in Two-Stage Operational Amplifiers," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 8, pp. 1770-1781, Aug. 2020, doi: 10.1109/TVLSI.2020.2986508.

[3] S. Liu, Z. Zhu, J. Wang, L. Liu and Y. Yang, "A 1.2-V 2.41-GHz three-stage CMOS OTA with efficient frequency compensation technique", *IEEE Trans. Circuits Syst. I Reg. Papers*, vol. 66, no. 1, pp. 20-30, Jan. 2019.

[4] R. G. H. Eschauzier, L. P. T. Kerklaan and J. H. Huijsing, "A 100-MHz 100-dB operational amplifier with multipath nested miller compensation structure", *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1709-1717, Dec. 1992.

[5] "Multi-stage amplifier with capacitive nesting for frequency compensation", Apr. 1984.

[6] R. Nagulapalli, K. Hayatleh, S. Barker, S. Zourob, N. Yassine and B. N. K. Reddy, "A Technique to Reduce the Capacitor Size in Two Stage Miller Compensated Opamp," 2018 9th International Conference on Computing, Communication and Networking Technologies (ICCCNT), Bengaluru, India, 2018, pp. 1-4, doi: 10.1109/ICCCNT.2018.8493494.

[7] Behzad Razavi, Design of Analog CMOS Integrated Circuits (1st. ed.), McGraw-Hill, 2000.

[8] Z. Yan, P. Mak and R. P. Martins, "Two Stage Operational Amplifiers: Power and Area Efficient Frequency Compensation forDriving a Wide Range of Capacitive Load", *IEEE Circuits and Systems Magazine*, vol. 11, pp. 26-42, 2011.

[9] Yao Libin, M. Steyaert and W. Sansen, "Fast-settling CMOS two-stage operational transconductance amplifiers and their systematic design", *Proc. IEEE International Symposium on Circuits and Systems*, 2002.

[10] P.R. Gray and R.G. Meyer, "MOS operational amplifier design-a tutorial overview", *IEEE Journal of Solid-State Circuits*, vol. 17, no. 6, pp. 969-982, Dec. 1982.

[11] S. I. Singh, "Design of low-voltage CMOS two-stage operational transconductance amplifier," *2017 International Conference on Electrical, Electronics, Communication, Computer, and Optimization Techniques (ICEECCOT)*, Mysuru, India, 2017, pp. 248-252, doi: 10.1109/ICEECCOT.2017.8284677.

[12] *Allen.P.E., and Holberg.D.R., "CMOS Analog circuit design" Third Edition, 2019, Oxford University Press*

[13] *The Miller Effect and Pole Splitting©2000 Thomas H. Lee, rev. October 17, 2003; https://web.stanford.edu/class/archive/ee/ee214/ee214.1042/Handouts/HO9POLESPLIt.pdf*