International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 10 Issue: 07 | July 2023 www.irjet.net p-ISSN: 2395-0072

Experimental Electrical Characterization Results of PLL Jitter

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Abstract - *In this letter, we aim to validate and check the electrical characteristic of Analog IPs embedded in SoCs. Analog blocks are more prone to the external behavior because the human world can talk and think in an analog manner. Hence, not easy to satisfy the requirement from an analog point of view compared to digital circuits which can be simulated and tested. Furthermore, when an analog comes into the picture, the noise insertion and its interface connections start creating problems in satisfying the actual specifications. Electrical characteristics validated on SoCs are single period and long-term Jitter for PLLs and their functionality according to the specifications. Further, our work will be based on improving the test bench with automated test environment, since automation helps to reduce human errors and make the testing process more reliable.*

***Key Words*: PLL, Jitter, Noise, Analog, SoC, Validation**.

1. INTRODUCTION

A phase-locked loop (PLL) is an electronic circuit that continuously modifies its voltage or voltage-driven oscillator's frequency to match that of an input signal. PLLs can produce, maintain, modulate, demodulate, filter, or recover a signal from a communications channel[1] that is "noisy" because data is being interrupted. PLLs (Phase-Locked Loops) are essential components in many wireless and radio frequency (RF) applications due to their ability to generate stable and precise frequencies. They play a crucial role in various communication systems and devices, including Wi-Fi routers, broadcast radios, walkie-talkie radios, televisions, and mobile phones. Here's a brief explanation of how PLLs are used in these applications, which further helps in low power and delay electronics device[8]. A PLL is used for clock generation inside SoC, and its working and application are pretty similar to a frequency synthesizer in a cellphone to match the cellphone frequency with desired frequency of reception of the message signal, then communication can take place. The core function of a PLL is to synchronize the phase and frequency of an output signal with that of a reference signal. This closed-loop feedback system allows the PLL to lock onto and track the phase and frequency of the reference signal, making it an essential tool in many applications. It is a system of analog and digital components connected in a "negative feedback" topology rather than a single component.

2. PLL AND ITS BASIC BUILDING BLOCK

A PLL consists of three key components:

1. **Phase detector** (a phase comparator or mixer). It compares the phases of two signals and generates a voltage according to the phase difference. It multiplies the reference input and the voltage-controlled oscillator output.

2. **Voltage-controlled oscillator** produces a sinusoidal signal whose frequency matches closely the low-pass filter's centre frequency.

3. **Low-pass filter**: the loop filter plays a crucial role in smoothing and shaping the control voltage that is applied to the Voltage-Controlled Oscillator (VCO). Its primary function is to attenuate the high-frequency alternating current (AC) components of the phase detector's output signal while allowing the low-frequency components (DC) to pass through relatively unattenuated. This action smoothens and flattens the signal, making it more DC-like or continuous.

To better understand the operation, let`s start with the basic building blocks of PLL

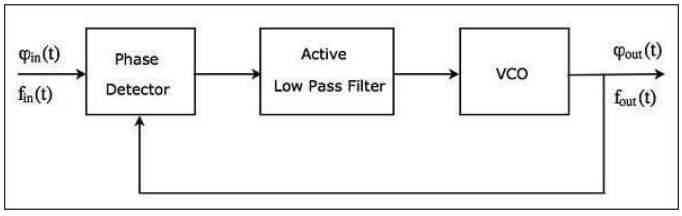

Figure 1: Basic Block Diagram of PLL

The phase detector (PD) compares the phase difference between the input signal's frequency (f_ref) and the feedback signal's frequency (f_out). It does not generate a DC voltage directly proportional to the phase difference, but rather it produces a voltage that represents the instantaneous phase error between these two signals.

The phase detector can be represented by a phase comparator or a multiplier. When using a multiplier as the

phase detector, the output signal will contain two frequency components:

The sum frequency: This component is equal to f_in + f_out. It arises because the phase detector multiplies the input and feedback signals, producing the sum of their frequencies as one of the output components.

The difference frequency: This component is equal to |f_in - f_out|, where the absolute value is taken to ensure it is a positive frequency. This component also appears in the output because of the multiplication process in the phase detector..

When no input is supplied to a VCO, it generates a signal at a specific frequency. A DC voltage can be applied to this frequency to move it in either direction. The frequency deviation is thus directly related to this. The voltage-controlled oscillator signal is compared to the input/reference signal by the PLL. The PLL can identify frequency and phase discrepancies in the signals because it is frequency and phase sensitive. It produces or generates an error signal that reflects the phase difference in the transmission. The low-pass filter(LPF) uses this difference, which is an error signal to remove high-frequency components and convert the error signal to changing direct current (DC) levels. The voltage-controlled oscillator is subsequently given this "feedback signal" in order to regulate its frequency.

3. JITTER AND ITS TYPES

Many of the signals inside a PLL, as well as those at the input and output, are binary signals. The jitter of binary signals is a frequent way to describe noise. An unwanted change or ambiguity in the timing of occurrences is known as jitter. Typically, the transitions in a signal are the events of interest.

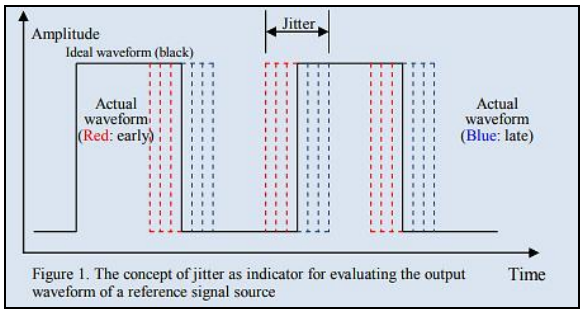

Figure 2: Jitter

Digital signal waveforms show up as a bright line on an oscilloscope. It is possible for this brilliant line, which should oscillate frequently, to appear thick at times. A jitter is indicated by the signal line expanding..

Figure 2 [2]depicts a single period, or cycle, of a signal containing numerous distinct periods. An ideal waveform exhibits a consistent and repetitive cycle. However, real-world waveforms vary in the time domain, with signal edges either rising or falling earlier (red) or later (blue) than expected. Jitter is introduced due to slight instabilities in electrical signal reading equipment and interference along signal-carrying paths. Excessive jitter can lead to interference between neighboring signals, resulting in a degradation of image and sound quality during transmission.

1. Types of Jitter :There are many types of jitter, including the following:
   - Period jitter (peak to peak)
   - RMS jitter
   - Random jitter
   - Deterministic jitter
   - Accumulated jitter (long-term jitter)

   We will be calculating period and long-term jitter.
   Period jitter (peak-to-peak jitter)

   1.1. **Period jitter** is observed as variation width. Epson expresses this variation using a peak-to-peak value.
   1.2. **RMS jitter** (1-sigma) The standard deviation (a) of the above measurement findings is used to calculate RMS jitter. This indicates a 68.26% chance that it exists within 12.5 p. Peak-to-peak jitter, on the other hand, only reveals a small percentage of states (many ms) in a crystal product that is typically used for an extended period of time and does not exhibit overall jitter. RMS jitter is only a meaningful measurement for an ideal normal distribution (Gaussian distribution); it is exceedingly unreliable for other distributions.
   1.3. **Random jitter** (RJ) As the name suggests, random jitter is a jitter component that cannot be predicted. Random jitter can occur spontaneously as it is influenced by a device's characteristics, thermal noise, etc. Random jitter is expressed using standard deviation, using the expressions "right RJ" and "left RJ."
   1.4. **Deterministic jitter (DJ),** Circuit design, electromagnetic induction, or the external environment can all induce bounded jitter. Actual measurement findings show that deterministic jitter is the part between right and left random jitter. To summarise the preceding jitter ideas, spontaneously induced jitter (RJ) and artificially induced jitter (DJ) are components of the overall jitter in a single cycle length. Reducing deterministic jitter is the key to decreasing jitter. When this component is optimized, the gap between the right and left RJ overlaps, allowing a perfect normal distribution to occur.

1.5. **Accumulated jitter** (long-term jitter) Accumulated jitter is a type of jitter that cannot be described as variations within a single cycle or period. Instead, it results from the cumulative effect of jitter fluctuations observed over numerous successive cycles. In this context, the horizontal axis of a jitter plot represents the number of measured cycles, while the vertical axis depicts the jitter's 1-sigma value for each cycle. Analyzing accumulated jitter allows us to observe the behavior of jitter over consecutive cycles. With accumulated cycles, there is a tendency for the 1-sigma jitter values to converge or stabilize starting from a certain cycle. This means that as more cycles are considered, the jitter fluctuations tend to reach a relatively consistent level, providing insights into the long-term stability and behavior of the jitter phenomenon. This enables the PLL circuit bandwidth and transient response characteristics to be determined[2].

Jitter has an impact on the setup and hold of the route elements because it alters the circuit's clock delay and the amount of time the clock is available at sync points. Depending on whether the jitter makes the clock run faster or slower in a system that otherwise has clean timing, setup hold or setup violations may happen. As a result, the chip's functionality or performance will degrade and, when analysing timing, the designer must take into account the jitter values of the clock signal.

4. VALIDATION METHODOLOGY OF PLL

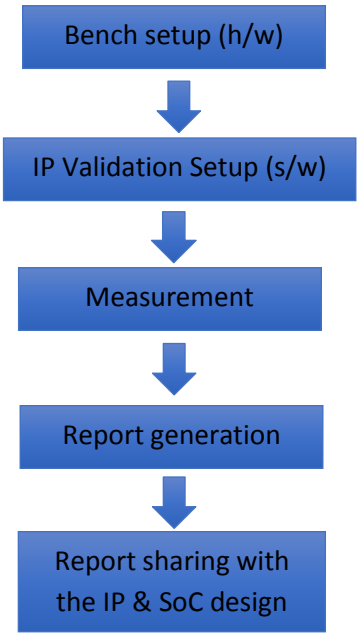

Figure 3: Validation Flow

PLL testing is an essential part of validation. Our primary focus is to use PLL inside the SoC to provide a variable frequency clock input to many blocks and the peripherals attached to SoC for their data transfer synchronization. In such architecture, PLL0 and PLL1 are connected in cascaded mode, and the source clock to PLL can be provided by any of the three available sources, i.e., IRC (16MHz), XOSC (40MHz), and externally by AWG.

The test execution is done in automation to avoid human errors. At the same time, it is also cumbersome for a human to collect so much data manually. All the bench instruments are connected together to the PC through the GPIB interface, an IEEE interface standard that allows control of the equipment remotely. The test automation is achieved through VBA (visual basic for application). A VBA script is written to control these instruments to change their voltage supply and temperature, capture the data through an oscilloscope and log them into the Excel report file and using pivot chart, we plot the graph to have the understanding of results .

4.1 Equipment Used to Perform Testing

1. 4GHz Oscilloscope

2. Precision Temperature Forcing System (PTFS)

3. Arbitrary Waveform Generator (80MHz) for applying external clock.

4. Lauterbach Debugger Hardware with JTAG connection interface.

5. Active probe. One end is connected to Oscilloscope, and another is connected to the PLL clock out probing point on Daughterboard.

4.2 Validation Condition for IPs

Temperature:

Table -1: Temperature required for testing the PLL

	T ambient	**T Hot**	**T Cold**
DUT Temperature	25	Max spec plus 5C	Min spec minus 5C

Power Supply:

Table -2: Maximum and Minimum Power supply Required for testing the PLL

V max	**V type**	**V min**
VDD+10%	VDD	VDD-10%

Number of Samples:

The number of trials should be done on three samples to avoid discrepancies. It could be extended to more if the result is not compliant with the expected to ascertain if a particular observed issue is really present on the IP or not.

4.3 Types of Test Codes for PLL

There are two types of test codes under which the PLL is tested, Quiet Mode Code and Application like Code(Run_Idd Mode).

In Quiet mode Code, all IPs present inside the SoC are not active, only the PLL under test is activated and a couple of other IPs are really needed for the SoC. Most of the IPs are kept under power down. At this time, fewer transistors are going through transitions, which means only a few are switching on - off. This assures that there is minimum noise generated inside the SoC, and PLL is minimally affected by the noise inside the SoC.

On the other hand, an Application like code (Run_Idd Mode) is used, and most of the IPs inside the SoC are enabled/activated. This way, the maximum number of possible transistors are going through transitions means getting switched on – off. This creates noise inside the SoC and is normally the actual use case under which PLL has to work.

We perform the Jitter test on both types of codes. The parameters we measured in validations are Short-Term (Single Period) Jitter and Long-Term Jitter on both the PLLs, which are embedded inside the 32-bit microcontroller architecture SoC.

4.4 Software Development

A unique software code has to be developed by configuring the PLLs under test to generate the desired output clock frequency as per the test cases.

5. EXPERIMENTAL RESULTS

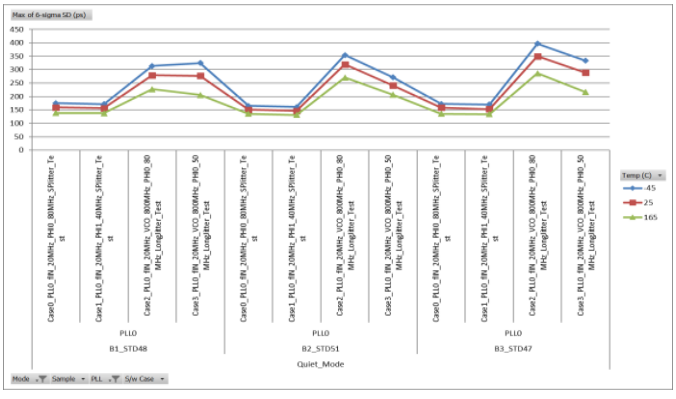

Chart-1: Single Period & Long Term Jitter PLL0: Quiet Mode

The above experimental results of consolidated Single Period Jitter and long term Jitter of PLL0 Quiet Mode which made us to conclude that the results are under the specification provided by the design team which are:

Case	Type of Jitter	Min. Value after testing	Max. Value after testing	Max. value specified by the designer
Case 0	Single period	93.708 ps	175.25 ps	200 ps
Case 1	Single period	89.448 ps	171.468	300 ps
Case 2	Long term Jitter	149.594 ps	397 ps	500 ps
Case 3	Long Term Jitter	127.746 ps	330 ps	500 ps

Table-1: Results of Single Period & Long Term Jitter PLL0 (Quiet Mode)

We can also conclude that the results of long term jitter are high as compared to single period jitter because of the obvious increased number of cycles used in long term jitter.

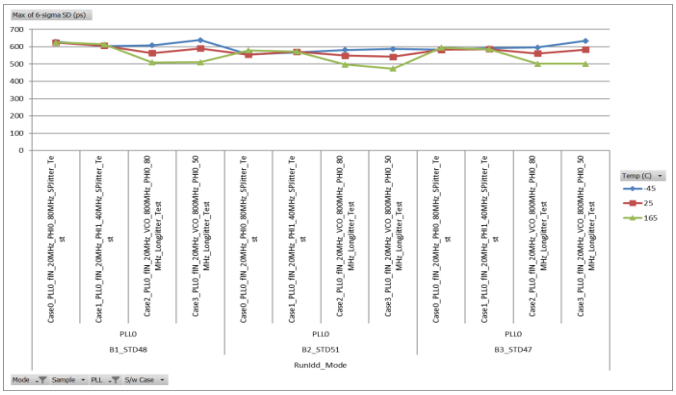

Chart-2: Single & Long Term Period Jitter PLL0: Run_Idd_Mode

The above experimental results of consolidated Single Period Jitter and long term Jitter of PLL0 Run Idd Mode which made us to conclude that the results are not under the specification provided by the design team which are:

Case	Type of Jitter	Min. Value after testing	Max. Value after testing	Max. value specified by the designer
Case 0	Single period	311.166 ps	628.950 ps	200 ps
Case 1	Single period	304 ps	613.632 ps	300 ps
Case 2	Long term Jitter	320.976 ps	607.854 ps	500 ps
Case 3	Long Term Jitter	257.796 ps	638.130 ps	600 ps

Table-2: Results of Single & Long Term Period Jitter PLL0 (Run_Idd_Mode)

The reason behind the results are not under the specification are in Run Idd mode is employed

- The majority of the SoC's IPs are turned on or activated. In this manner, the most transistors possible are switching on and off or passing through transitions.
- This causes noise inside the SoC and is typically the use case that PLL has to operate in.

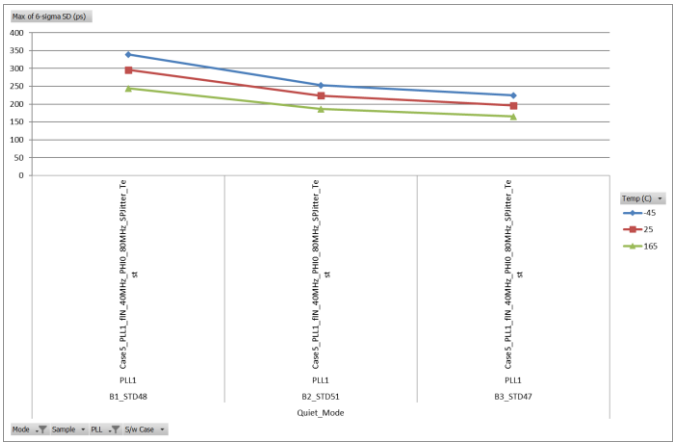

Chart-3: Single Period Jitter PLL1 :Quiet Mode

The above experimental results of Single Period Jitter of PLL1 Quiet Mode which made us to conclude that the results are under the specification provided by the design team, which is:

Case	Type of Jitter	Min. Value after testing	Max. Value after testing	Max. value specified by the designer
Case 5	Single period	105.522 ps	338.934 ps	500 ps

Table-3: Results of Single Period Jitter PLL1(Quiet Mode)

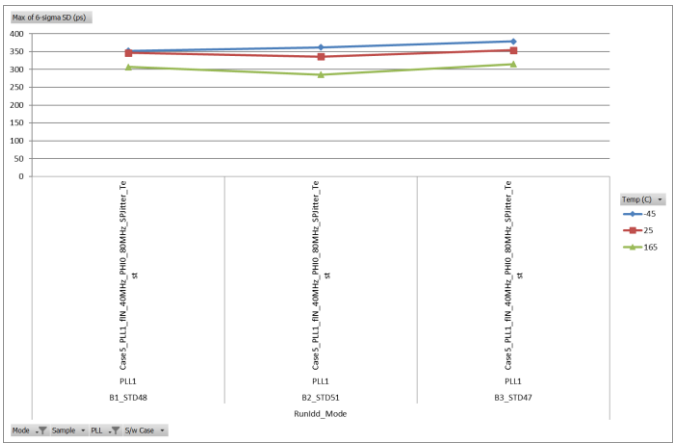

Chart-4: Single Period Jitter PLL1:Run_Idd_Mode

The above experimental results of Single Period Jitter of PLL1 Run Idd Mode which made us to conclude that the results are under the specification provided by the design team, which is:

Case	Type of Jitter	Min. Value after testing	Max. Value after testing	Max. value specified by the designer
Case 5	Single period	187.602 ps	378.474 ps	500 ps

Table-4: Results of Single Period Jitter PLL1(Run_Idd_Mode)

- All three samples(SoC) used during the testing of are following almost similar trend, which makes us to justify that the results we are getting are accurate and can be used.
- one thing we can observe in the graph that we are getting lower standard deviation at the temperature 165 C at the hottest.

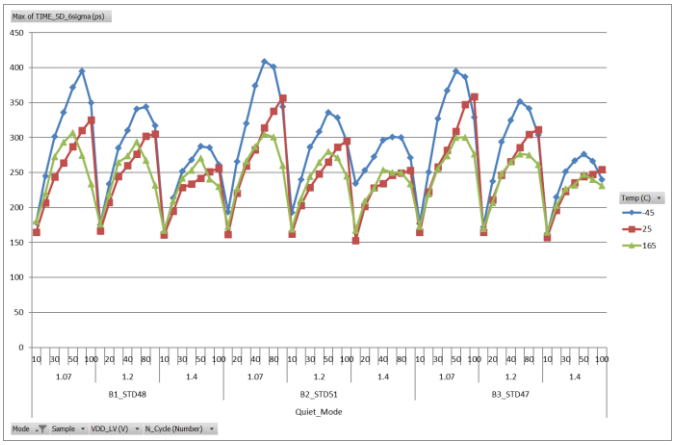

Chart-5: Long Term Jitter PLL0: Quiet Mode

The above experimental results of Single Period Jitter of PLL0 Quiet Mode which made us to conclude that the results are under the specification provided by the design team, which is:

Case	Type of Jitter	Min. Value after testing	Max. Value after testing	Max. value specified by the designer
Case 4	Long term Jitter	153.012 ps	408 ps	1000 ps

Table-5: Results of Long Term Jitter PLL0 (Quiet Mode)

- All three samples(SoC) used during the testing of are following almost having similar behaviour, which makes us to justify that the results we are getting are accurate and can be used.
- One thing we can observe in the graph that we are getting lower standard deviation at the temperature -45 C at the min temperature.

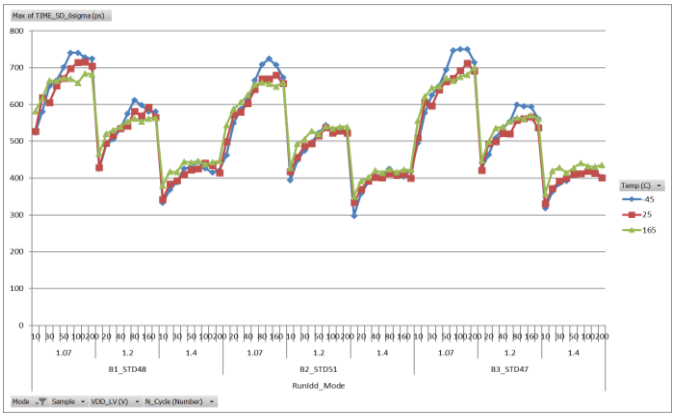

Chart-6: Long Term Jitter PLL0 (Run_Idd Mode)

The above experimental results of Long term Jitter of PLL0 Run Idd Mode which made us to conclude that the results are under the specification provided by the design team, which is:

Case	Type of Jitter	Min. Value after testing	Max. Value after testing	Max. value specified by the designer
Case 4	Long term Jitter	297.534 ps	750.456 ps	1000 ps

Table-6: Results of Long Term Jitter PLL0 (Run_Idd Mode)

- All three samples(SoC) used during the testing of are following almost similar trend, which makes us to justify that the results we are getting are accurate.

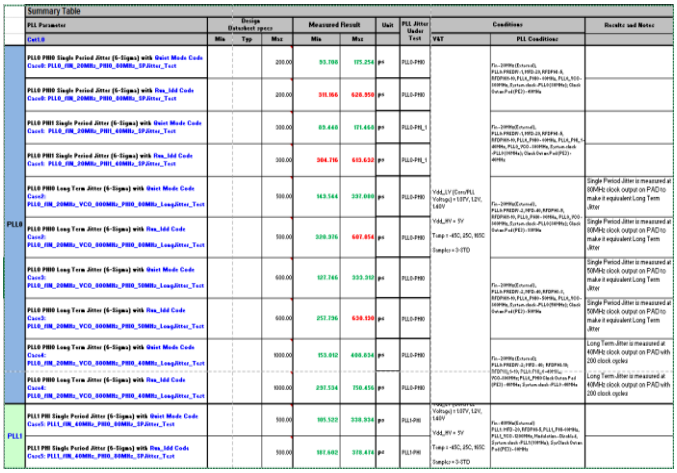

Chart-7: Results of PLL

6. CONCLUSIONS

Once the measurements are done, data is plotted, and the result is analyzed. After analyzing the plotted results, it's observed that all samples tested follow almost the same temperature and voltage variations trends. By checking their minimum & maximum values, we can conclude that the results are within the design specifications or not under the tested VT conditions.

It's observed that jitter with application like code (Run_Idd), is much higher with respect to the quiet mode code, because a lot more transistors are switching, creating more noise inside the SoC in the former case.

PLL Jitter also increases if unwanted noise is generated by any particular IP inside the SoC, affecting the PLL

Thermal noise, power supply changes, loading situations, device noise, and interference coupled with surrounding circuits also contribute to jitter.

Table -3: Results of the PLL

Test Overview	Condition	Results
The test aimed to check the single period and long-term jitter.	Temp: - 40C, 25C, 165C VDD-HV; 3V, 6V VDD-LV:1.07V, 1.2V, 1.40V Fin: 20/40MHz, Fref=Xosc VCO: 800MHz PLL0 PHI: 40/80MHz Clock out on Pad: 40MHz	Within specification Min Variation: -0.00215% Max Variation: +0.0125%

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