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Circuit Approaches for VLSI in Internet-of-Things Applications

KM Sandhya Bhashkar[1], Sushil Chandra Agrawal[2]

[1]M.Tech, VLSI, National Institute of electronics and information technology, U.P, India
[2]Principal & Technical Officer, Department of VLSI, National Institute of electronics and information technology, U.P, India

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Abstract - *IoT circuit designers confront problems and possibilities. Security and power management are essential for billions of devices that perceive, compute, communicate, and interact. The physically unclonable function (PUF) is becoming increasingly essential in hardware-security applications because it gives device variations an object-specific physical identity that is hard to disclose and replicate by adversaries. Creating a tiny PUF that can withstand voltage, temperature, and noise is tough. This thesis proposes PUFs with two ultra-small analog circuits that output absolute temperature. Two works demonstrate the proposed method: (1) an ultra-compact and robust PUF based on voltage-compensated proportional-to-absolute-temperature voltage generators, which takes up 8.3 less area than the previous work and twice the robustness of the most compact PUF design; and (2) a method to transform a 6T-SRAM array into a robust analog PUF with minimal overhead. This work uses a similar circuit design to convert an on-chip SRAM into a PUF, lowering size in (1) without sacrificing robustness.*

When battery replacement is expensive, an Internet of Things sensor node needs energy harvesting. EH, PMUs lose efficiency during voltage transfer from harvester to battery and battery to load. A capacitor buffers energy flow in an EH PMU with hybrid energy storage.

Key Words: VLSI Design, IoT Applications, Circuit Approaches, Low Power Design, Energy Efficiency, Ultra-Low Power.

1. INTRODUCTION

A VLSI circuit is like a tiny electronic puzzle made up of many small components called transistors. It is designed to perform specific tasks by controlling the flow of electricity. Think of it as a mini-orchestra conductor that guides the movement of electrons to create useful functions.

These circuits are made of a special material called silicon, and they are so small that you need a microscope to see them. Each transistor acts like a switch, allowing or blocking the flow of electricity. By arranging these switches in clever ways, we can make the circuit do different things, like adding numbers, storing information, or even playing music.

The VLSI circuit is all about making connections. It has pathways called wires that connect the transistors, allowing them to work together as a team. The design of these connections is crucial because it determines how well the circuit performs its tasks.

Just like how a puzzle needs to be put together in the right way to work, the VLSI circuit needs to be carefully designed and manufactured to function properly. Engineers use special computer programs to plan and create these circuits, making sure everything fits together perfectly.

Figure-1: VLSI Circuit

VLSI circuits are used in all sorts of electronic devices, from smartphones and computers to cars and home appliances. They are the building blocks of modern technology, making it possible for our devices to perform complex tasks quickly and efficiently.

In simple terms, a VLSI circuit is a small electronic puzzle made of tiny switches that control electricity. It is designed to do specific jobs and is used in many of the electronic devices we use every day.

1.1. Factor Affecting Performance of VLSI Circuit

Several factors can affect the performance of a VLSI (Very Large Scale Integration) circuit. Here are some key factors to consider:

1. Clock Frequency: The clock frequency determines the speed at which the circuit operates. Higher clock

frequencies generally result in faster circuit performance. However, increasing the clock frequency can also lead to higher power consumption and increased heat generation.

2. Transistor Size and Technology: The size and technology of the transistors used in the VLSI circuit have a significant impact on performance. Smaller transistors allow for higher packing density and faster switching times, leading to improved performance. Advanced semiconductor technologies, such as FinFET or nanoscale process nodes, offer better performance characteristics.

3. Interconnect Delay: The interconnects that connect different components in the circuit introduce delay. Longer interconnects and higher resistance can lead to increased signal propagation delay, impacting overall circuit performance. Design techniques like buffering, routing optimization, and interconnect scaling help mitigate interconnect delay.

4. Power Consumption: Power consumption affects the performance of VLSI circuits in multiple ways. Excessive power consumption can lead to increased heat dissipation, reliability issues, and reduced battery life in portable devices. Power optimization techniques, such as voltage scaling, clock gating, and power gating, are employed to balance power consumption and performance.

5. Circuit Design Techniques: Various circuit design techniques can impact performance. Design choices like pipelining, parallelism, and data path optimizations can improve throughput and latency. Additionally, efficient memory architectures, such as cache designs and memory hierarchy, play a crucial role in performance optimization.

6. Noise and Signal Integrity: Noise, including crosstalk, electromagnetic interference (EMI), and power supply noise, can degrade signal integrity and impact circuit performance. Proper shielding, signal isolation, and noise reduction techniques are essential for maintaining signal integrity and maximizing performance.

7. Process Variations: Variations in the manufacturing process can impact the performance of VLSI circuits. Process variations can lead to differences in transistor characteristics, interconnect resistance, and capacitance, affecting circuit speed and reliability. Design techniques like process corner optimization and statistical analysis help account for process variations.

8. Temperature: Circuit performance can be affected by temperature variations. Higher temperatures can cause increased leakage currents and degraded transistor performance, leading to slower operation and potential reliability issues. Thermal management techniques, such as heat sinks and thermal design optimization, are employed to control temperature and maintain performance.

9. Design Constraints: Design constraints, including area constraints, timing constraints, and power constraints, can impact performance. Balancing these constraints and optimizing the design within these limitations is crucial for achieving desired performance.

Optimizing performance in VLSI circuits involves a careful balance of these factors, considering the specific requirements of the circuit's application and the available design resources. Designers strive to achieve the best trade-offs between performance, power consumption, area utilization, and reliability to create efficient and high-performing VLSI circuits.

2. FULLY-INTEGRATED POWER MANAGEMENT CIRCUITS

In the vast realm of electronic enchantment, fully-integrated power management circuits emerge as the ethereal guardians of energy flow, gracefully orchestrating the dance between power sources and the multitude of hungry electronic souls they nourish.

These magical circuits, akin to miniature power sorcerers, possess the ability to harness and manipulate the elusive currents of electricity, ensuring they flow harmoniously to each component in need. Like a symphony conductor, they deftly balance the delicate art of power distribution, granting life to the electronic realm.

Within the depths of their intricate circuitry lies a tapestry of enchantments. Pulse-width modulation spells imbue them with the power to control energy levels, adjusting the flow to meet the needs of their charges. Voltage regulators, with their mystical incantations, ensure that the currents are stable and pure, protecting the delicate souls of the electronic kingdom.

These circuits possess a boundless versatility, adapting their enchantments to fit the needs of diverse realms. They gracefully dance alongside processors, sensors, and memory, empowering them with just the right amount of energy to thrive. Whether it be the fleeting whispers of a handheld device or the mighty roar of a high-performance system, these circuits bestow their magical energy upon all.

Fully-integrated power management circuits are the ever-vigilant custodians of efficiency and conservation. Their

spells of efficiency enchant, ensuring that no drop of energy is wasted, and the electronic realm flourishes sustainably. Energy-harvesting enchantments capture the ambient energies of the world, transforming them into precious fuel to power the ever-growing realm of devices.

As they weave their magic, these circuits also safeguard the electronic kingdom from harm. Protection spells guard against overvoltage, overcurrent, and overheating, shielding the delicate components from the ravages of electrical chaos. Their watchful eyes and lightning-quick responses shield the realm from harm, ensuring its longevity.

In this realm of electronic enchantment, fully-integrated power management circuits are the unsung heroes, working tirelessly to nourish and protect the electronic landscape. Their presence is often hidden, tucked away within the labyrinthine depths of devices, yet their influence is felt in every moment of operation.

Truly, these circuits are the keepers of the electronic flame, illuminating our lives with the magic of technology. With their delicate balance of power and protection, they breathe life into our devices, empowering them to weave their spells of connectivity, computation, and communication.

3. Analog PUF Architecture in VLSI Circuit

Analog Physical Unclonable Function (PUF) architecture in VLSI (Very Large Scale Integration) is a design approach that utilizes the inherent variations in analog circuits to create a unique identifier for each integrated circuit.

In analog circuits, some slight differences or variations occur during the manufacturing process. These variations can be caused by factors such as process variations, temperature fluctuations, or aging effects. Analog PUF architecture takes advantage of these variations to create a unique response that can serve as a digital fingerprint for each chip.

The architecture of an Analog PUF typically involves a challenge-response mechanism. A specific input, known as the challenge, is provided to the PUF. The PUF then generates a response based on the unique characteristics of the circuit. This response is specific to the individual chip and cannot be replicated, making it suitable for authentication or security purposes.

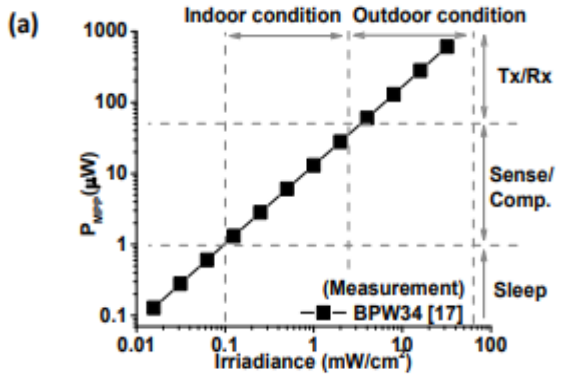
Analog PUFs offer certain advantages over digital PUFs. They are generally more resistant to modeling attacks and reverse engineering because the variations in analog circuits are complex and difficult to reproduce accurately. Additionally, Analog PUFs can be implemented using simple circuit elements, making them efficient in terms of area utilization and suitable for integration into VLSI chips.

However, Analog PUFs also face challenges. The variations that make each PUF unique can introduce some instability in the response over time or due to environmental conditions. To mitigate this, calibration and compensation techniques are employed to ensure the reliable and consistent operation of the PUF.

In essence, Analog PUF architecture in VLSI exploits the inherent variations in analog circuits to create unique and unclonable identifiers for individual chips. By leveraging these variations, Analog PUFs provide a reliable and unpredictable response that can be used for authentication, security, and other applications where uniqueness and trustworthiness are required.

4. PHOTOVOLTAIC POWER HARVESTING AND POWER LOSS IN IoT NODES UNDER DIFFERENT LIGHTING CONDITIONS

An alternate architectural arrangement has been suggested as a potential answer to the issue to avoid the need for a high-ratio conversion. This has been done to solve the issue. These two modes are known by their respective names. Despite this, it can operate in several various ways as well. This is something that may be considered a possibility. In the mode that is referred to as directly charging, it creates a connection between a PV cell and V_{Load} while at the same time keeping control over V_{Load} by storing any additional energy in the battery. This model is referred to as "direct charging." When the system is configured to function in the mode known as discharging direct, the load will get power from the battery through both the direct channel and the discharge route.



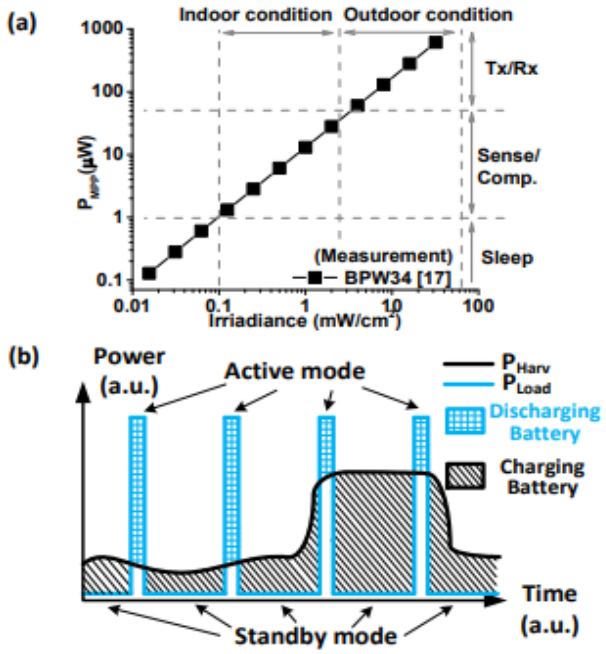


Figure-2: (a) Photovoltaic power harvesting and power loss in IoT nodes under different lighting conditions. b) End-to-end energy efficiency is lower when batteries are charged and discharged.

In the computations that were carried out to evaluate the trustworthiness of the cold-start strategy, both the Corner method and the Monte Carlo method were utilized as different approaches. As can be seen in Figure-3 and Figure-4, the predetermined threshold of the cold-start detection, which is denoted by the designation "Vtrip," varies by 110 mV depending on which process corner is being considered (a). The picture demonstrates this difference very clearly. It has been discovered that the power consumption of the EH PMU, which is measured in tens of nanowatts, does not have a significant impact on the effectiveness of the device.

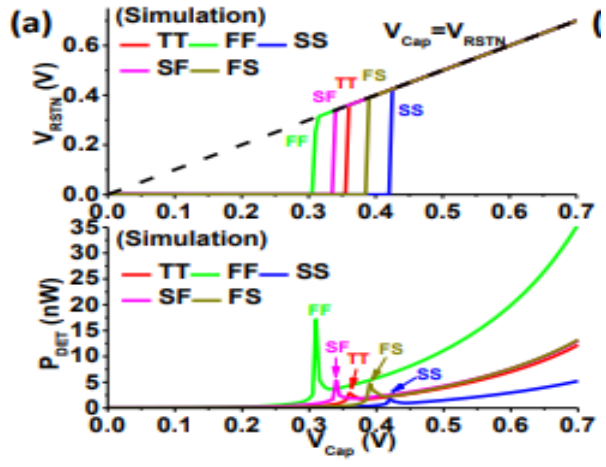


Figure-3: Corner-to-corner trip point voltage and cold-start sensing power.

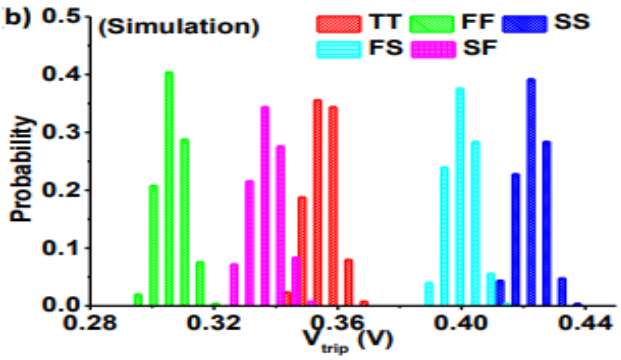


Figure-4: Monte-Carlo process corner trip-point voltage models.

Our ensemble observation Kalman filter (EOKF) makes use of regression spike rates as the state observation in a KF. This results in a 400-fold reduction in the amount of processing that is required in contrast to the conventional Kalman filter that is used for decoding (Table-1). The findings from DREAM indicate that at the higher velocity range, the performance of EOKF is superior to that of KF (Figure-5). Following that, these methods were included in circuits that measured 0.18 micrometers in size, had their leakage decreased to an ideal level, and had been optimized, respectively. The power dissipation of the NSP is at a level that is at an all-time low of 0.61 microwatts, which is remarkable for a system that has 96 channels (6.35 nanowatts per channel).

Table-1: The complexity of the calculation is cut in half thanks to EOKF.

KF Operations	# of Calculation (Mult./Add/Div.)	
	Standard KF	EOKF
A Priori Estimate	4/2/~	4/2/~
Posterior Estimate	80/80/~	46/46/~
Kalman Gain	32180/32060/1180	10/9/4
Post. Error Cov. Matrix	96/92/~	16/16/~
Total	32360/32234/1180	76/73/4 (*~400x less*)

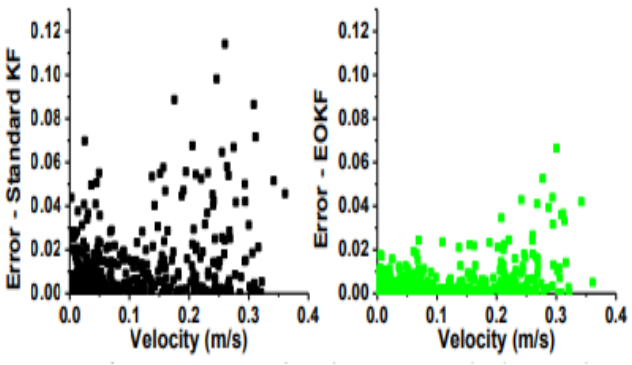


Figure-5: EOKF vs. KF performance.

5. CO-DESIGN OF THE PMU AND NSP FOR VLSI

PMU (Power Management Unit) and NSP (Noise Suppression Unit) are two critical components in modern VLSI (Very Large Scale Integration) design. The PMU is responsible for regulating the power supply to various components in the chip, while the NSP is responsible for filtering out noise from the power supply.

Co-design of the PMU and NSP is important because they are tightly coupled, and the design of one can affect the performance of the other. For example, the PMU must provide a stable power supply to the NSP, while the NSP must filter out any noise generated by the PMU.

One approach to co-designing the PMU and NSP is to use a mixed-signal design methodology. This approach involves combining analog and digital circuits to achieve optimal performance. The analog circuits are used for the PMU and NSP, while the digital circuits are used for control and communication between the two.

Another approach is to use a power-aware design methodology, which takes into account the power consumption of the PMU and NSP. This approach involves optimizing the design to minimize power consumption while still meeting the performance requirements.

The hybrid error- and replica-based control that it has is the first characteristic that differentiates it from other species. In-situ EDAC in the NSP quickly adjusts VDD when used in conjunction with a programmable SC-DC that has a 63-ratio ratio. With the implementation of a recent upgrade, the NSP EDAC now has expanded functionalities. We made advantage of the sparse insertion method to position the error detection latches (EDL) such that they were positioned between the queues and the sorters The process of body-swapping was able to aid in the correction of inaccuracies that were made in the individual's recall of their weight. We were able to conserve some power by just switching the memory bank body, which was all that was required of us (out of 16).

The regulation of gene expression by replica- and error-based mechanisms is shown in figure-6. If there is a problem with the timing, the PMU controller will alter the phase of the SC-DC to restore the output voltage. This is done to stop the output voltage from falling below a certain threshold. To provide sufficient power for body swapping error correction, the SC-fSC DCs go through a period of fast surge during the core clock cycle. If the issues are not resolved, the controller is programmed to lower the SC-DC CR, which will increase VDD. If the controller determines that the issues have not been fixed, this will take place.

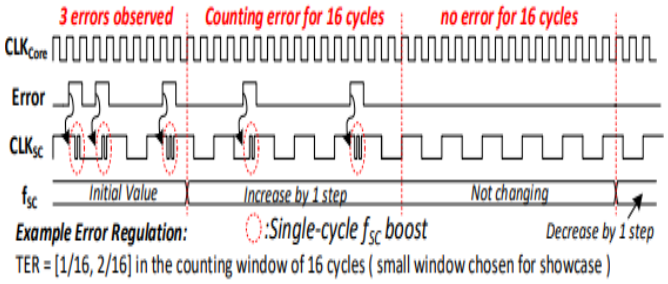


Figure-6: Waveforms for controlling errors.

6. CONCLUSIONS

The Internet of Things requires power management circuits. Energy harvesting is a viable option for battery replacement in low-power IoT nodes. Early EH PMU systems lost plenty of power during harvester-to-battery and battery-to-load voltage changes. The EH PMU with hybrid storage decreases energy loss from two voltage changes, which is good. We analyze design tradeoffs between efficiency and enhancing capacitor capacity, load, and harvester power profiles. The recommended architecture requires trade-offs since the two efficiency optimization techniques disagree. IoT nodes' low power needs challenge PMU designers. Such a semiconductor needs a high PCE, 100% integration, and an adaptive DVS. The system supports both. These regions require further investigation for the argument. Our control system automatically finds the SC-ideal DC configuration and switching frequency to eliminate the loss of components and increase V_{DD} margin and PMU PCE. The latest PUF artwork shows that robustness and compactness have improved over the previous decade, but there is always potential for improvement. But instability in weak PUFs like ours is the main problem. PUF analysis requires chip-stored error-correcting codes and bit masks. Thus, NVM bit mask tweaks may cause fault injection attacks. Thus, architectural data limits are unclear. "Powerful" PUF architectural designs typically employ "weak" circuit topologies. Effective PUFs need research into the micro voltage generator pair design. The EH PMU design has not been fully tested in a realistic harvester/load power consumption situation. One SC design may transmit power across several voltage domains, eliminating the need for many converters. PMUs and industrial equipment loads must account for time closure. Fix hold-time violations on timing arcs when the supply voltage is phased with the essential route.

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