International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 10 Issue: 06 | Jun 2023 www.irjet.net p-ISSN: 2395-0072

Study and Analysis of Low Power SRAM Memory Array at nano-scaled Technology

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Abstract - *The cache memory design of microprocessors makes use of Static Random-Access Memory (SRAM) cells. Their efficiency is crucial because they are an integral part of the central computer system. Only 10–15 percent of a modern system on a chip's (SoC) transistors are dedicated to logic, whereas the rest are used for cache memory, increasing the performance strain. On top of that, the AI-reliant nature of today's implantable, portable, as well as wearable electronic equipment highlights the need for a robust SRAM architecture for CIM. Modern mobile communication devices include ample storage space for users' extensive media collections. Here, we adapt the Multi-threshold CMOS design to create a low-power SRAM cell. Power usage and read/write cycle Access Time can be lowered by using CMOS transistors with various threshold voltages. This work proposes a novel approach to reducing leakage in the idle state to cut down on power usage. The power usage of an SRAM cell is affected by the temperature, size of the transistors as well as the voltage used in the test. Data storage is an important function of several electronic components, specifically digital ones. The overall power usage of an SRAM is heavily influenced by leakage current. The research utilized a 1-bit 6T SRAM cell to construct a 1 KB memory array using CMOS technology and 0.6 volts for the supply voltage. In this section, we use deep submicron (130nm, 90nm, and 65nm) CMOS technology and the six-transistor (6T) SRAM cell to analyze how varying topologies impact the performance of a 12T SRAM array.*

Key Words: Cadence, SRAM, CMOS, 7T SRAM Cell, Leakage Power.

1. INTRODUCTION

Several industries benefit greatly from artificial intelligence as well as machine learning [1]. Such techniques involve extensive data processing as well as calculation. Modifications to the hardware execution of AI technologies are essential for energy-efficient applications like the IoT [2]. One of the most promising approaches to enhancing energy efficiency is the use of in-memory computing. Multiple forms of in-memory multiplication, as well as logical operations, are already a reality. Khwa et al. [3] to perform ternary multiplication, a six transistor (6T) cell was employed in conjunction with a reference voltage generating column; Yin et al. [4] a PMOS substrate offset on a 12T cell proposed as a means of producing the same effect. On the other hand, such techniques need more room to implement the PMOS body bias or a reference voltage-generating array. In addition, columns are used to store the operands for the aforementioned operations [2][5][6][7], It is not how data is stored in standard SRAM (static random-access memory), and hence necessitates extra data movement. DRAM cells can operate without a steady stream of electricity. However, DRAM relies on periodic pre-charging of its storage capacitors. Choi et al. DRAM array cells as well as a sense amplifier (SA) worked together to complete the logic tasks [8]. Ali et al. a DRAM array that can-do vector addition [9]. Yu et al. made ternary multiplication possible with a 4T2C DRAM chip [10]. Yet, the read operation on many rows might lead to data corruption whenever IMC (in-memory computing) is implemented in DRAM. Therefore, this disadvantage necessitates the insertion of extra safety circuits.

2. LITERATURE REVIEW

Sudhakar Alluri et.al [11] In this study, we construct and simulate six-transistor FINFET-based static RAM cells then analyze the challenges inherent in their design as well as the metrics by which their success is measured. Minimizing SCEs, drastically reducing the maximum allowed duration, measuring the tremendous reliability of this process in a weak-power region, and so on. Power dissipation, leakage current, sub-threshold current, and static noise margin for FINFET and MOSFET 6 transistor static RAM were evaluated at the 45nm node. While modern SRAM cells have greatly reduced power consumption as well as leakage current, the identical technique is utilized. The performance of FINFET-based SRAM cells has been evaluated to that of conventional, advanced MOSFET-based Static RAM cells.

M.Srinivas et.al [12] Power loss during standby is mostly due to leakage currents, and they are unfortunately on the rise. Sub-threshold leakage increases as the threshold voltage is lowered because the gate current leaks more quickly. As the number of people who rely on mobile devices increases, so does concern over leakage energy use. If you rarely use your phone and instead leave it in standby, you can improve

battery life by minimizing leakage power consumption. Therefore, reducing power usage has grown into a priority during the CMOS circuit design process. An AND gate using the MOS parameter model, designed and simulated in 65nm CMOS technology at 27 0C, 0.70V supply voltage, provides confirmation of the proposed circuit. This is, of course, intended to be said aloud. Power loss during operation versus standby states, along with propagation time and dynamic dissipation, are contrasted with present MTCMOS and SCCMOS approaches.

Hemant Kumar et.al [13] Against every reason in this research, we show that 32 nm SRAM (RL-SRAM) is possible with Add 0.7 V and RL-SRAM with body bias. In reversible logic SRAM cells, the adiabatic approach allows the node capacitance energy to be utilized instead of dissipated as heat. On comparing CNTFET RL-SRAM as well as body-biased RL-SRAM to CNTFET SRAM cells, we find that the former improves latency by 60.72% & the latter by 65.20%. The CNTFET SRAM cell design greatly enhances the average power use, leakage power and delay time dissipation without degrading the overall performance, as shown by contrasting it with prior work. Butterfly curve as well as N-curve analyses are utilized to better check the longevity of the memory cell.

S Pousia et.al [14] One of the most challenging issues in modern engineering is designing low-power, high-speed CMOS devices. Static power usage is becoming more of a problem as technology develops. Sleepy keeper technique, sleep technique, leakage control transistor technique, stack technique, & sleepy keeper leakage control transistor technique are only a few of the various approaches for reducing leakage power. Low power usage and fast speed were both possible in the CMOS design because to the suggested power gating approach. In a low-power, fast-access design, this method is employed to determine the half adder, x nor gate, x or gate, and 6T SRAM cell. SRAM cells save 35.9% of power as well as 25.6% of delay compared to a half adder, while an x or gate saves 19.5% of power and 33.5% of delay. Compared to a standard gate, NOR gate reduces energy consumption by 12.5% and delay by 23.2%. The leakage power consumption and simulation time are drastically decreased using Tanner's EDA tool.

Hemant Kumar et.al [15] One of the most challenging issues in modern engineering is designing low-power, high-speed CMOS devices. Static power usage is becoming more of a problem as technology develops. The sleep method, the stack method, the sleepy stack method, & the sleepy leakage power strategy are only a few of the many ways available. As silicon technology continues to progress, power dissipation at the NANO scale has emerged as a critical problem. A digital system's power consumption can be decreased while its performance is increased. This study evaluates the operation of several low-power CNTFET SRAM cells fabricated using Cadence Virtuoso 32 nm technology. Leakage Feedback, Sleep, Sleepy Keeper, Zigzag, & Stack are some of the low-power strategies used by the CNTFET SRAM cell in this study. Sleepy keepers have been shown to lower power consumption by as much as 84.26% (81.13 %) on average, 38.12% (43.01%) in delay, and 9.15% (20.80%) in leaky power consumption. The suggested CNTFET SRAM cells' memory cell stability is evaluated using a butterfly curve using an analytic N-curve method. Since the SRAM cell's performance indices improves considerably, increasing system efficiency even as cell size grows.

Shalini Singh et al. [16] SRAM memory was used for constructing a 1KB memory. A 7T SRAM cell with an average latency of 21 ns and a minimal leakage current of 20.16 pA was used to realize the array structure. This was achieved by employing a 2D array constructed from the SRAM's building blocks. The pre-charge circuit, sense amplifiers, address decoder, and write driver were all designed utilizing the Cadence Virtuoso tool in 45 nm technology to accommodate the 32 x 32 array. The 1 KB SRAM-relying memory's writing, as well as reading operations, consumed 51.57 mW and 447.3 mW of power, correspondingly. Reducing the nominal voltage can have an effect on the PVT fluctuations, the noise margin, and the cell stability.

Read stability or periodic pre-charge during the read/write cycle is a major challenge in SRAM design. This research detailed how the new SRAM design developed by Alex Gong et al. [17], including a special emphasis on the reading operation, can address these two problems. The utilization of sense-amplifying cells allowed for the inversion of cellular nodes. It was hypothesised that by physically isolating the digital output bits from the data retention elements, a read-SNM-free SRAM cell might improve read resilience. Cadence design software was used to develop this in 0.18 m CMOS technology. The total power usage of this SRAM decreased within similar operating settings as its conventional analogue. The SRAM area needed for this technique is double that of 6T SRAM cells or 8 transistors per cell.

Rashmi Bisht et al. [18] created an SRAM array & all its ancillary parts, including the sense amplifier, write driver circuit, row decoder, pre-charge circuit. Noise was reduced by employing differential sensing amplifiers, which are capable of rejecting common mode voltage. Cross-coupled CMOS inverters were used to reduce the amount of static power lost. This design also features high noise immunity & low operating voltage. The superior stability of complete CMOS SRAM cells over resistive load SRAM cells at low supply voltages have been established. The total measured power draw of the SRAM array was 24.58 mW. The popular gpdk180 library (also known as the 180 nm technology node) was used during the design process.

Himanshu Banga et al. [19] showed off a 16x16 SRAM with less wasted space on the chip and less wasted power from leakage. As a consequence, the SRAM's functionality improved. The smaller peripheral utilised less power because the constraints on its size were loosened. This technique is helpful for low-energy applications if the size of the SRAM

memory is not an issue. Significant reductions in power consumption were achieved by employing sleep & forced transistor approaches in this investigation. Compared to the sleep method, the forced transistor was found to be 99.94% faster, and it also reduced overall power consumption by 56.92%. The 16x16 SRAM memory was designed, fabricated, and evaluated using the Cadence tool and the baseline UMC 180 nm technology library.

Improving performance as well as power consumption whilst fixing the problems of the standard SRAM cell, Shyam Akashe et al. [20] created a five-transistor SRAM cell with zero read static noise margin. They used the large bias towards zero in the bit stream of memory in typical programmes to design this one-of-a-kind cellular structure. The primary research discovery that informed this design was that cell leakage is quantified at the node wherein the transistor is disabled. When compared to the 6T SRAM cell, the projected cell area was 21.66% smaller while increasing speed by 28.57%, assuming identical design parameters. The suggested cell's longevity, that mimics 45 nm technology, was calculated with the use of proper read/write operations. The novel cell also has 70% shorter latency than a conventional six-transistor SRAM cell. Even while the suggested cell's memory cell access leakage current doubled for every 10 degrees Celsius above room temperature, it was still 72.10 percent lower than that of the 6T SRAM cell.

3. SRAM ARCHITECTURE

The block diagram of a typical SRAM has depicted in Figure.1. Bit-oriented and word-oriented layouts are both possible for SRAMs. Although each address in a word-oriented memory typically takes up n bits (preferred choices of n include 8, 16, 32, and 64), when using an SRAM that is bit-oriented, only one bit is needed for every address. Using column decoders or column multiplexers (YMUXs) directed to the Y address bits, two, four, or more columns can share a single sense amplifier. It is crucial to create a read-safe and write-reliable SRAM cell. Both of these requirements impose opposite ones on the estimation of the transistors in an SRAM cell. The transistor ratios in an SRAM cell need to be calculated for optimal reading and writing. The preceding provides the basic squares for SRAM construction.

1. SRAM cell.
2. Pre-Charge Circuit.
3. Write Driver Circuit.
4. Sense Amplifier.
5. Row decoder.

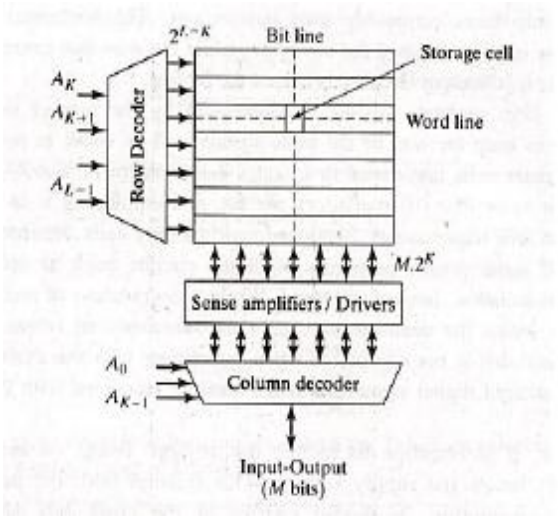

Fig -1: SRAM Block diagram

Memory Cells That Use SRAM Figure 3 depicts a typical SRAM cell, which has six transistors. Q and Qb are the internal nodes that store the bit value and its complement, accordingly. These vertices are lifted by PMOS transistors PU1 & PU2. Pulling down internal nodes is the job of NMOS transistors PD1 & PD2. The PG1 as well as PG2 pass transistors allow for read and write operations.

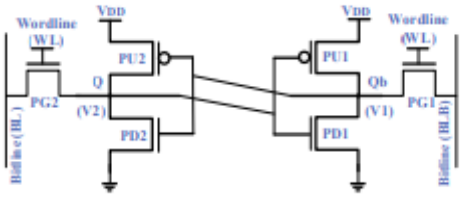

Fig -2: Conventional 6T-SRAM cell with: Pass gate, pull up, and pull-down transistors.

Hold, read, & write are the 3 methods of operation available to an SRAM cell. The cell retains its internal bit value when in hold mode because the WL (wordline) signal is low. The bitlines (BL and BLB) are conditioned by an initial conditioning circuit before every read or write operation. The stored value can be retrieved by applying the WL signal to both PG transistors throughout the read operation. As a result, the PG and PD transistors discharge one of the BLs whereas another BL remains high. The SRAM cell stores the bit as well as its complement on the BLs in this fashion. For a PD transistor to be able to discharge a BL, its matching PG transistor has to be weaker. The relative efficiency of these transistors is seen by Equation (1). For read operations to succeed, CR values must be more than one. The capacitive value of a BL is high because it links many individual cells. As a result, the discharge process is lengthy. Consequently, a sensing amplifier, that amplifies the comparatively small differential voltage across the BLs, is used to transmit the bit value to the external circuitry.

$$\text{Cell Ratio (CR)} = \frac{(W/L)_{PD1}}{(W/L)_{PG1}} = \frac{(W/L)_{PD2}}{(W/L)_{PG2}} \quad (1)$$

First, the value that is written upon the cell is used to determine which of the BLs will be pulled down by a powerful write driver. Since the design density has risen, more capacitance has been introduced to the WL assertion, making it slower. Initially, a PU transistor resisted the BL's pull on the storage node via a PG transistor. This imposes a rule of thumb called "write ability."

$$\text{Pull Ratio (PR)} = \frac{(W/L)_{PU1}}{(W/L)_{PG1}} = \frac{(W/L)_{PU2}}{(W/L)_{PG2}} \quad (2)$$

4. 7T SRAM CELL: PROPOSED DESIGN

The 7T SRAM Cell is introduced to help with leakage control. A schematic of a 7T SRAM cell is depicted in Figure 2. 7 transistors are employed in this design, as suggested by the name. Like a 6T SRAM Cell, but with an extra NMOS transistor connecting the pull-down transistors to the ground node. WL is the input of the extra NM5 transistor. Subthreshold leakage & gate tunneling are primarily caused by leakage currents.

The leakage power is related to the cell's capacity for storage. When the gate voltage of a transistor is less than its threshold voltage, a subthreshold current is flowing. Thus, the NM3 & NM4 access transistors are disabled in standby mode if WL is asserted low. Subthreshold leakage current passes through off transistors because of the stored value (logic 0) in the SRAM cell. It's possible that the supplementary bottom transistor NM5 will sever the ground connection. This lessens the likelihood of leaking occurring at the sources of SRAM cells. Bottom transistor NM5 switches on in active mode whenever WL is asserted high. Therefore, it functioned similarly to a 6T SRAM cell during write and read operations. The marginal gain in write access time caused by the extra transistor is insignificant. However, the size of the array grows, especially for larger arrays. 7T SRAM cells have dimensions that are comparable to 6T SRAM cells, with the NM5 channel width at 200 nm and the NM5 channel length at 120 nm both being taken into account.

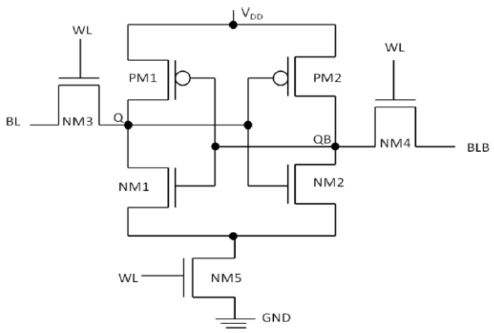

Fig -3: Circuit diagram of 7T SRAM Cell

4.1 Pre-charge Circuit

The core of each SRAM array is its pre-charge circuit. Figure 4 shows the charging circuit during the first stage of the process. Three PMOS transistors make up the pre-charge circuit. The third transistor performs the pre-charging duty, whereas the first two are used for equalisation.

Before any read or write operations can take place, the bitlines must be pre-charged to VDD = 0.7V using the pre-charge circuit. PMOS transistors are thought to have a width of 200 nm as well as a length of 120 nm. In the array, there is only one pre-charge circuit for every column.

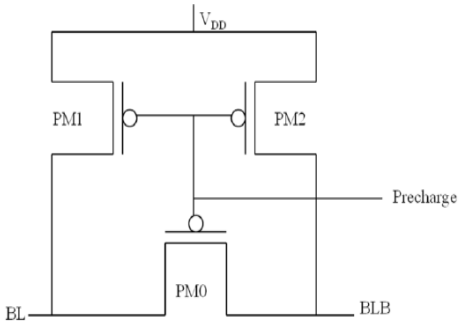

Fig -4: Circuit diagram of pre-charge circuit

4.3 Write Driver Circuit:

Discharging one of the bitlines is the main job of a write driver circuit. It is possible to activate the write driver by sending a Write Enable (WE) signal to it. Each array column just needs a single write driver circuit. Figure 3.3 depicts the write driver circuit. It has 4 NMOS transistors (NM0, NM1, NM2, & NM3) and two inverters (I1 and I2). For an NMOS transistor, 120nm of channel length and 200nm of channel width are typical dimensions.

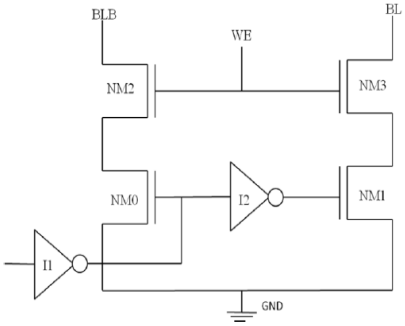

Fig -5: Circuit diagram of write driver circuit

4.2Sense Amplifier

An SRAM without a sense amplifier would be useless. The schematic for a Differential Type Sense Amplifier (DTSA) is

depicted in Figure 3.4. You may know it better by the name "voltage mode sense amplifier." The DTSA algorithm operates in a dynamic design mode, constantly monitoring the disparity among bitlines and adapting its output correspondingly. A sense amplifier's primary function is to provide dependable performance throughout a read operation; hence it must be able to withstand internal system noise without being affected. Several variations of sense amplifiers have been described in academic papers. DTSA outperforms other sensing amplifiers and is immune to system noise. The active current mirror load (PM0 & PM1) is comprised of a differential pair (NM1 and NM0) and a biasing current source (NM2). The drain of either the NM0 or PM0 is linked to the bitlines, while the input is the differential pair. A Sense Enable (SE) signal activates the Sense Amplifier during a read operation.

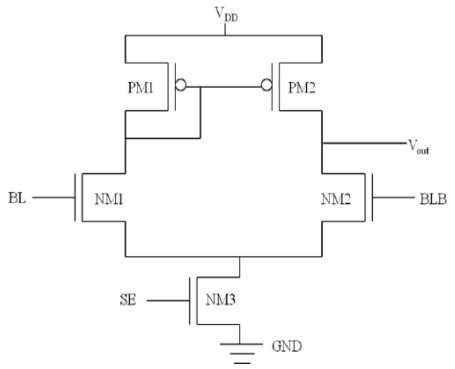

Fig -6: Circuit diagram of sense amplifier

4.4 Row/Column Decoder

Address decoders serve to translate a user's inputted address into a row or column activation in a memory layout. To access a specific WL or WE in an SRAM array, a row & column decoder is employed.

The block design of a decoder with 4 inputs (a, b, and c) and eight outputs (X0 through X7) is depicted in Figure 3.5. This study employs a decoder built on an AND gate.

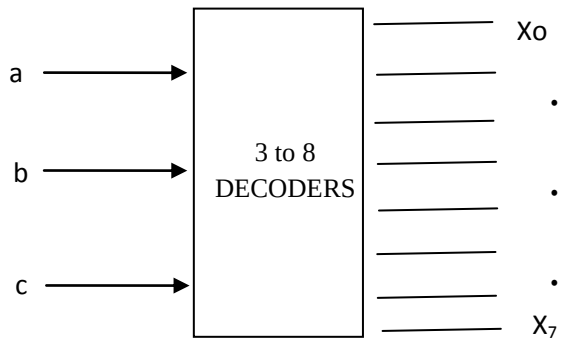

Fig -7: Block diagram of 3:8 decoder

Table -1: Performance Analysis of 6T to 12T SRAM Memory Array (MA)

Performance Parameter	6T SRAM MA	7T SRAM MA [21]	8T SRAM MA [22]	9T SRAM MA [23]	10T SRAM MA [24]	11T SRAM MA [25]	12T SRAM MA [26]
Read Dynamic Power(μW)	16.85	25.48	18.4	18.96	23.73	58.15	73.1
Write Dynamic Power(μW)	24.31	7.5	26.5	8.19	27.49	50.83	69.1
Read Access Time(ps)	3.06	9.18	16.04	17.23	36.9	91.2	103.5
Write Access Time(ps)	33.53	27.96	37.93	36.7	41.83	61.06	118.3
Leakage Power(nW)	5.6	6.3	5.98	6.13	5.99	2.26	7.69

5. CONCLUSIONS

All current high-performance VLSI circuits necessitate some sort of data storage solution. Today's businesses require the ability to store as well as retrieve massive amounts of data quickly. The maximum retention period is close to two years, making it possible to run the programme again. Using CMOS technology, this work examines a 1 KB SRAM array in bit orientation, ranging from 6T SRAM cells to 12T SRAM cells. It has a storage capacity of 1024 bits. The suggested 1 KB SRAM memory array is considered low leakage, has small feature sizes, with low power consumption. Taking into account all of the variables, it was found that the 1 KB-SRAM-based memory's power usage varied significantly between the read & write operations. The number of bits of data that may be stored in a given area is a crucial metric for any storage system's efficiency. Memory access time is another crucial indicator of performance. The speed of a memory array is set by its access time. It is possible to lessen power consumption & delay by using CMOS transistors with varying threshold voltages. This work proposes a novel strategy that minimizes leakage current in the idle state, hence decreasing power usage. When testing an SRAM cell, the amount of power used is highly dependent on the voltage provided, the operating temperature, and the transistor size. Information may be stored in the memory of many electronic components, particularly digital ones. Power consumption in SRAM is mostly driven by leakage current. In this paper, a 1 KB memory array was constructed utilising a 1-bit 6T SRAM cell and 0.6 volts of supply voltage using CMOS technology. The various possible combinations are displayed below. Here, we examine the performance of a twelve-transistor (12T) SRAM array versus a six-transistor (6T) SRAM cell implemented in deep submicron (130nm, 90nm, and 65nm) CMOS technologies.

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