

A Comparative Performance Analysis of Copper on Chip and CNTFET Nano Interconnects

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Abstract - The digital electronics industry has advanced quickly, which has led to the miniaturisation of semiconductor industries. Power consumption in the Deep Sub Micron domain has become a significant problem due to leakage current, hence researchers are always looking at different strategies to reduce it. There are other approaches available for the same thing, and using carbon nanotube technology is one of the methods that shows promise for effectively designing low power circuits. In this article, new methods for reducing leakage power are introduced. In this work, the primary performance metrics of the CNTFET and the Copper on Chip Nano-interconnect have been compared. By combining process variation in CU and CNT - Interconnects with tube variation at 32nm technology, we were able to quantify the effects of ION and IOFF current. We also examined how the performance of digital circuits changed as technology advanced. The various simulation results show that applying 10% deviation from the mean to various device characteristics parameters, including source and drain doping concentration with Cu and CNTFET interconnects for NFET and PFET with a range of tubes from 1 to 16, is effective. These parameters include length of gate (L-*Tube*), width (W*Tube*), threshold voltage (*V*_{th}), thickness (total), and source&drain doping concentration. All of the experimental results were obtained using the HSPICE simulator and the 32nm Berkley Predictive Technology module with the CU and CNT SPICE models at 27 °C temperature.

Key Words - I_{ON} and I_{OFF}, CNTFET, Mean, Standard Deviation, Power Consumption.

1. INTRODUCTION

Carbon Nanotubes possess invaluable electric as well as monotonous features. CNTs are an Interconnect material in VLSI technology. CNTs major classifications are single-walled (SWCNT) and multi-walled (MWCNT). Single-walled CNTs based devices have dimensions less than 1nm where as Multi-walled CNTs have device dimensions < 100nm [1-3]. Figure 1 represents three dimensional architecture of CNTFET.

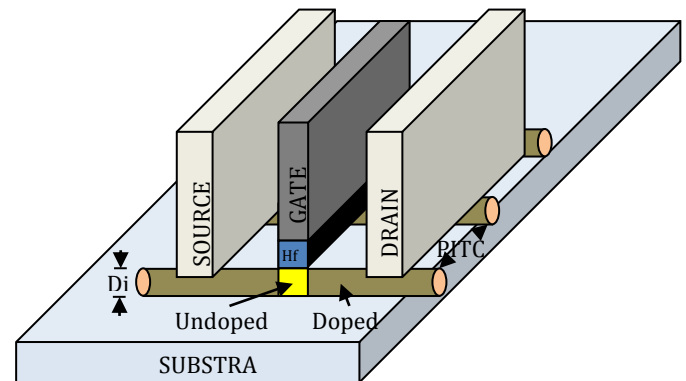


Figure 1: 3D Structure of CNTFET

2. CNTFET

CNTs are Hexagonal package of atoms known as benzene ring. This ring makes a Graphene sheet. Further, this rolled-up sheet constitutes CNTs. The roll with diameter of less than 1nm is classified as SWCNT. When such tubes placed in bundles, the bundles are known as MWCNT. The superlative monotonous electric as well as architectural features of CNTFET suggest as definite choice for Interconnect material for long terms. The CNTs functioning can be stated as in figure 2.

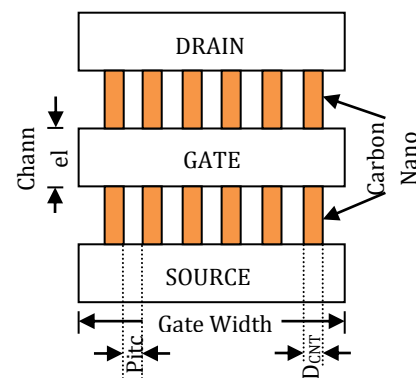


Figure 2: Top View of CNTFET

The CNTFET architecture is much similar to conventional MOSFET structure barring source-drain channel region being interchanged by CNTs. At the same time, source-drain channel is doped heavily, resulting in elevated

operating speed [4-5]. The inbred CNTs are manufactured circumambient flat metallic gate terminal having high- k constant dielectric strength as zirconium oxide (ZrO_2) and hafnium oxide (HfO_2). The under layer is completely masked with non-conducting husky Silicon-oxide slab. A heterogeneous CNTFET aqueduct is constructed with infuse significant numbers of nanotubes lined straight along the width of channel, in such arrangement centre to centre gap in neighboring tubes is known as pitch.

While simulating the CNT Source-Drain are doped by 0.78%, having HfO_2 as gate non-conducting material having thickness $3nm$ as well as SiO_2 clot having concentration $10\mu m$ [6-8]. CNTs have a feature i.e. energy bandgap, E_g is oppositely harmonious to bore size, hence allowing wavering of bandgap with the CNTs diameter [9-10].

The features of CNTFETs are:-

Arrangement of carbon atoms in CNTs possessing unparalleled features:

Electric features: It is having better conductivity of both metallic as well as semiconducting features.

Elasticity feature: Graphene sheet is constituted by Carbon atoms with durable bonding. The elasticity is greater as pressed the CNT is bent but returns to nominal if force released.

Thermal Conductivity: CNTFETs have much greater conductivity as C-C chemical bond providing much needed potency and firmness to counter strains. Greater thermal conductivity has greater scope in nano scale molecular sensing devices. Also CNTs are prominent election as made by its features flimsy weight, liteness superior electro mechanical features.

3. INTERCONNECTS

An Interconnect has linear as well as non-linear components such as RLC of figure 3 for discerning development procedures modeling of necessary demeanor. Here Cu is countered against CNTFETs Interconnects posing enormous scope for performance existing conditions [10-12].

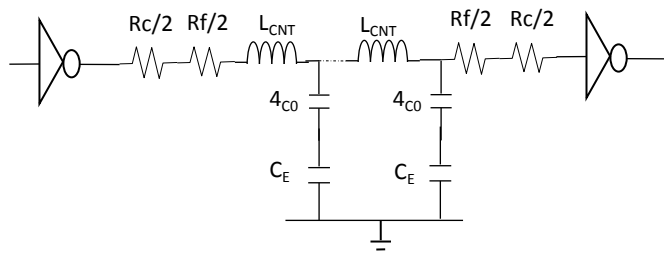


Figure 3: RLC Interconnects

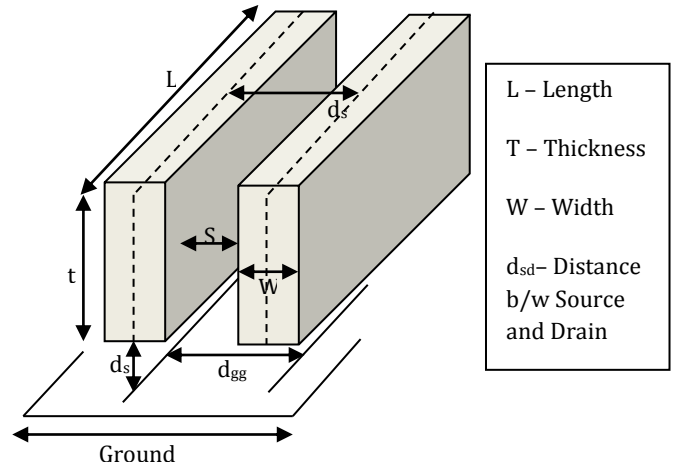


Figure 4: 3D Structure of Cu Interconnects

As figure 4 shows three dimensional sight for Cu Interconnects, for the quantification with centres Cu Interconnect along middle line to earth armanent is d_{sg} and d_{gg} CNT.

4. RESULTS AND DISCUSSIONS

Simulation results of 1, 4, 8, 16 CNT Interconnects suggest 11.05% deviation from WFF as average magnitude poses I_{OFF} current close to 112% has Tube-1 and 160% for Tubes 4, 8, 16 this gives greater mean regulation of I_{OFF} . Tubes fluctuations in domains that 9% of average magnitude for along length exhibits 43.09%, Range wide exhibits 37.88%, altitude 7.33%, WFF 115%, T-Tube depicts 38%, N have 34% sequential mean range fluctuation in I_{OFF} . It concludes Tubes and feature deviation exhibit larger I_{OFF} fluctuations in comparison to I_{ON} .

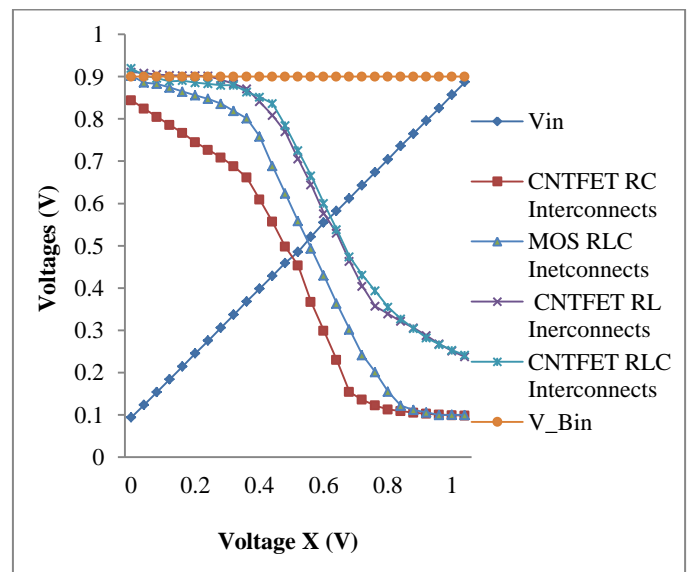


Figure 5: DC Characteristics of MOS and CNTFET Interconnects

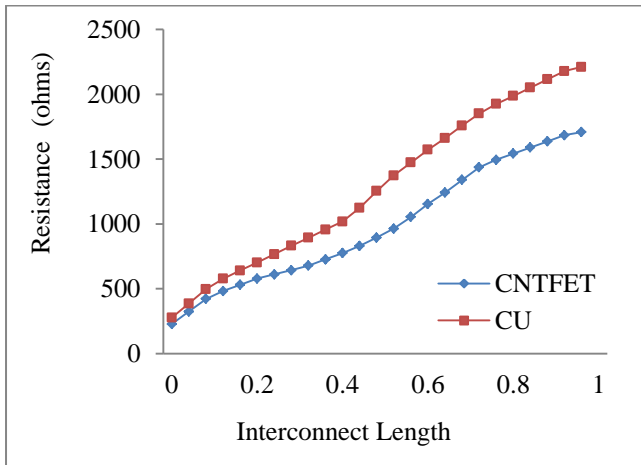


Figure 6: Resistance of Cu and CNTFET Interconnects

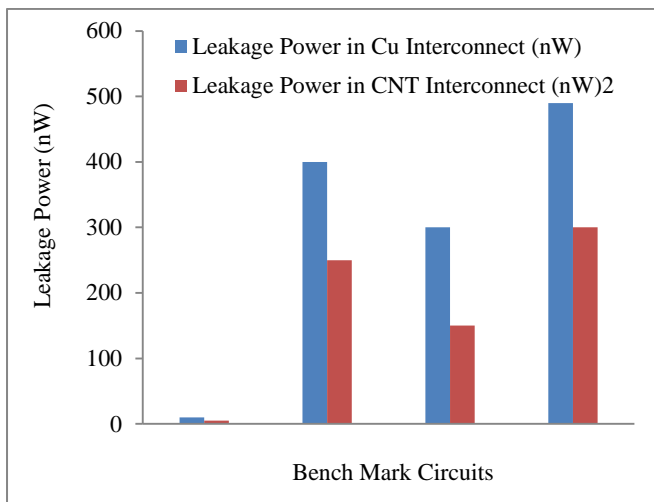


Figure 7: Leakage Power in Bench Mark Circuits using Cu and CNT - Interconnects

Figure 7 depicts leaking losses energy dissipation covering regulation yardstick criterion circuits comprising from Cu as well CNTFET Interconnects to agreement with affirmation of outcomes. Concluding Cu Interconnects dissipate larger energy as compared to C17 (ISCAS 85) conserves close to 46.86%, while B01 (ITC99) 40.9%, B02 (ITC 99) 48.9% and B06 (ITC99) 53.02%.

5. CONCLUSION

An idiosyncratic resemblance of Cu with CNTFET Interconnects for optimization has outcomes exorbitantly diminution of power dissipation. This work is suggesting PVT fluctuations of various features at elevated frequencies with diminished energy Interconnects usage. P-CNTFETs possess more of V_{th} , with scaling of current leakage while in futile idle phase. The outcome study suggests the CNT Interconnects coupled by CNTFET models consume energy more economically. CNT-Interconnect sustains ever changing energy about 90%, cuts down transmission

latency about 77% as well as percolation energy consumption diminishes 87.88% as while the scaling down device dimensions, smaller V_{DD} as well as entangled manifolds vector set, while as well various concerns reducing for retain identical electric field having maintain latest techniques, design developments and latest and recent EDA setup, with capabilities for handling issues pertaining to most recent fabrication methods including deviation demands.

REFERENCES

- Dadoria, A.K., Khare, K.: Design and Analysis of Low - Power Adiabatic Logic Circuits by Using CNTFET Technology, Circuit System and Signal Processing, Springer, **38**(2), 1-19 (2019).
- Dadoria, A.K., Khare, K; Gupta, T.K; Panwar U.: "Integrating Flipped Drain and Power Gating Techniques For Efficient FinFET Logic Circuits", International Journal of Numerical Modelling: Electronic Networks, Devices and Fields., JohnWiley, **31**(1), 1-8 (2018).
- Chandel, R; Kumar, A.: Design and Development of Dielectric based Electrostatic Micro actuators IETE Journal of Research Taylor & Francis, **46**(4), 261-264 (2000).
- Jadav, S; Vashistah, M; Chande, R.: RLC equivalent RC delay model for global VLSI interconnect in current mode signalling, International Journal of Modelling and Simulation, Taylor & Francis, **35**(1), 27-34 (2015).
- Stanford University CNFET Model.: (2014). <http://nano.stanford.edu/model.php?id=23>
- HSPICEvA-2008.03.: (2014). <http://www.synopsys.com/Community/Interoperability/HSPICE>
- Predictive Technology Model.: (2014). <http://ptm.asu.edu>
- Castro C, John; Pulfrey, DL.: Carbon nanotube transistors: an evaluation. Proceedings of SPIE: Device and Process Technologies for MEM's, Microelectronics, and Photonics III. Bellingham, Washington, USA; **5276**, 1-10 (2004).
- Khursheed, A; Khare, K; Haque, F.Z.: Designing high-performance thermally stable repeaters for nano-interconnects. Journal of Computational Electronics, Springer, **18**, 53-64, (2019).
- Pasupathy, K.R; Bindu, B.: Low power, high speed carbon nanotube FET based level shifters for multi-

VDDsystems-on-chips. *Microelectron Journal*. **46**, 1269-1274 (2015).

11. Girish Kumar, M; Chandel, R; Agrawal, Y.: An Efficient Crosstalk Model for Coupled Multi-Walled Carbon Nanotube Interconnects, *IEEE Transactions on Electromagnetic Compatibility*, **60**(2), 487-496 (2018)
12. Iijima, S.: Helical microtubules of graphitic carbon. *Nature*; 354 (6348), 56-58 (1991).