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FPGA Implementation of Accelerated Finite Impulse Response Filter for EEG Analysis

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Abstract — *Majority of the real time signal processing environments involve the processing of ample amount of data at a time. EEG Signal Processing is one such example, which demands the processing of EEG signals recorded over a larger time period for the study of brain activity. An electroencephalogram (EEG) is a test that measures electrical activity in the brain using small, metal discs (electrodes) attached to the scalp. The work presented in this paper is inclined towards the implementation of hardware accelerated Finite Impulse Response (FIR) filter for the processing of EEG signals. Discrete Wavelet Transform is used in the time-frequency analysis of EEG signals. The design is exported as an FPGA overlay which accelerates the processing of the EEG signal. We have used PYNQ –Z2 FPGA development board to implement the hardware accelerator.*

Keywords—Electroencephalography, EEG-Signal-Processing, PYNQ-Z2, Accelerated FIR Filter, Signal Processing.

I. INTRODUCTION

Signal processing, is a major engineering domain which is used to manipulate, analyses or synthesize various types of signals to extract out useful information. It is mostly done in a computer mainframe which has a generic DSP processor. The establishment of ASICs and FPGA prototyping aids in the development of dedicated hardware for a specific purpose. We have considered EEG signal processing in this paper and the implementation of the same in an FPGA development board, with an observation in the acceleration of processing speed by a factor of two (approx.)

Analyzing EEG data is an exceptional way to study cognitive processes. It can help doctors establish a medical diagnosis, researchers understand the brain processes that underlie human behavior, and individuals to improve their productivity and wellness.

There are commonly five sub-bands on the EEG signal: delta (0–4 Hz), theta (4–8 Hz), alpha (8–15 Hz), beta (15–30 Hz), and gamma (30–60 Hz). These individual frequency sub-bands may better represent brain dynamics than the EEG signal itself. Indeed, they contain more precise information on the neuronal activities and raise some alterations that do not appear in the raw EEG [1].

Hardware acceleration combines the flexibility of general-purpose processors, such as CPUs, with the efficiency of fully customized hardware (FPGA boards), such as GPUs and ASICs, increasing efficiency by orders of magnitude when any application is implemented in the digital computing systems

FPGAs are reconfigurable hardware chips that can be reprogrammed to implement varied combinational and sequential logic. Their programmability imparts excellent flexibility and the opportunity to quickly develop a prototype of a circuit keeping the same hardware this is due to the parallelism of FPGA accelerators which offer data, task, and pipeline parallelism, resulting in faster data process execution. A FPGA also complies with the high performance and low power operational needs of a given application, resulting in a high-performance ratio.

II. RELATED WORKS

Pari Jahankhaani et al. [2] proposed the DB4 algorithm or wavelet feature extraction method to classify the EEG signal into different small signals based on their frequencies for decision making. Hojjat Adeli et al. [3] investigated on discrete Daubechies and harmonic wavelets for analysis of epileptic EEG records. It is used to analyze and characterize epileptiform discharges. M. Popovic, M. Jankovic [4] proposed techniques to accelerate the actual program for optimum linear-phase FIR filter design. The time required for the design of these filters can be cut down by up to 2.5 times by utilizing these strategies independently. The execution time can be increased by up to 6 times when new methods are combined with other well-known approaches.

V.S. Lin et al. [5] has implemented FIR filter using dedicated hardware mapped onto a Xilinx FPGA board. For

more consistent and realistic results, the filter contains additional hardware that interpolates between adjacent coefficients. The identical filter is developed in MATLAB that has been optimized for software simulation. Another prominent technique used in contemporary communication systems is the fast Fourier transform (FFT). The FIR and FFT blocks' software simulation and co-simulation methods are contrasted in this paper.

Qi Li et al. [6] used FFT and Continuous Wavelet Transform (CWT) to improve the accuracy of EEG signal emotion recognition. Nitin Kumara et al. [7] uses bispectral analysis for emotion recognition while in this paper we use power spectral density method to find out the emotion. Paulo Possa et al. [8] used hardware accelerators to offload specific tasks from the CPU, improving the global performance of the system and reducing its dynamic power consumption. Harikumar Rajaguru and Sunil Kumar Prabhakar [9] have proposed the time frequency analysis (dBb2 and dB4) for epilepsy classification. In order to extract the features at level 4 from EEG signals, dB2 and dB4 wavelets are applied. The features are then categorized using a Linear Discriminant Analysis (LDA) Classifier.

III. PROPOSED METHOD

An EEG signal is a biological analog signal which needs to be handled in digital domain to extract out frequency specific information. The process flow of our system is shown in figure 1.1

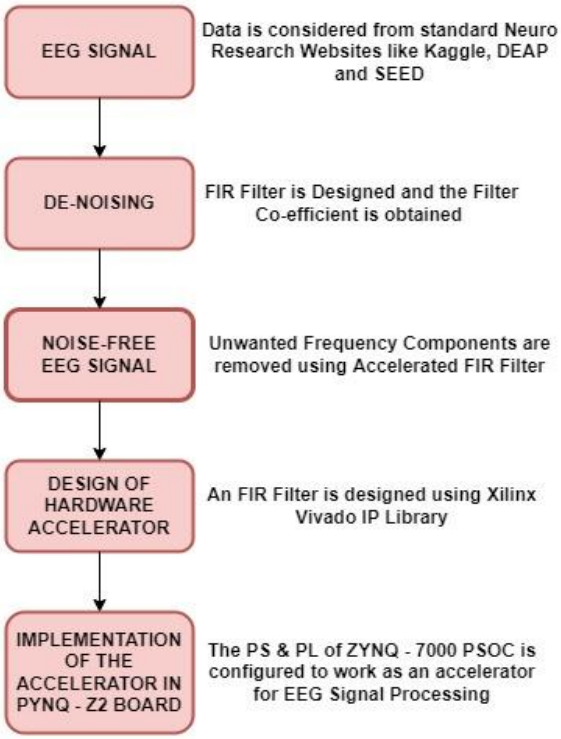

Fig 1.1 Process Flow

A. Process Flow

The required signal data is obtained from standard data libraries like Kaggle, SEED and DEAP. The dataset consists of numerous EEG signals recorded from various specimens for different amounts of time. For the testing and validation of our FIR accelerator, we have considered an EEG signal recorded for a duration of 30 minutes. The scaled down signal is showed in Fig1.8(a). This signal is heavily corrupted by noise and so needs to be denoised. EEG signals do not possess frequencies beyond 55 Hz. Thus, the signal is first bandlimited with a cut-off frequency of 60 Hz. Db-4 wavelet transform is used to extract out the approximations and details of the EEG signal in a staged approach.

An FIR filter is implemented as a soft IP in Xilinx Vivado and configured for the required frequency specifications. This IP is interfaced with the Zynq Processing System (PS) using Direct Memory Access (DMA). The design is dumped into the FPGA board and the FIR filter's time of execution is compared.

B. EEG Signals

The EEG signal data were taken from a renowned site called Kaggle (Kaggle, a subsidiary of Google LLC, is an online community of data scientists and machine learning practitioners). The data were collected and downloaded in CSV format.

C. Data Processing

The collected EEG signal data needs to be filtered and noise should be removed to get the useful information. We had several filtering techniques but the one we used for our project is the Daubechies 4 wavelet transform (db4). As we know that analysis can be done in the time domain or frequency domain, but EEG real-time bio signals have composite frequency components so we intend to process the signal simultaneously in both the domains which is known as the wavelet transform (db4).

We have four types of EEG signals and each one of them have varying frequency ranges in order to filter and then we need to have to do wavelet transform. Discrete Wavelet Transform (DWT) uses multilevel decomposition in order to convert the EEG signal into finer details. It allows finding the instant of any abrupt change. The concept of this wavelet analysis is the decomposition of the signal into two parts: approximations and details.

We used the Daubechies 4 wavelet transform (db4) to decompose the EEG signals into four levels. This wavelet decomposition yields five groups of wavelet coefficients (A4, D4, D3, D2, and D1) which correspond respectively to the waves: delta (0-4 Hz), theta (4-8 Hz), alpha (8-15 Hz), beta (15-30 Hz) and gamma (30-60 Hz).

This decomposition process is based on the successive application of high pass filter (HPF) and low pass filter (LPF). These two filters calculate the wavelet coefficients (details and approximations) at each level. To keep the same number of output and input samples, the product of convolution from the filters is down-sampled by a factor of 2. Only the output of the low pass filter, namely the approximation coefficients, is again processed by the two filters.

$$ED_i = \sum_{j=1}^{N} |D_{ij}|^2 \quad i=1,2,\ldots,l$$

$$EA_i = \sum_{j=1}^{N} |A_{ij}|^2 \quad i=1,2,\ldots,l$$

Where: -

l **:** decomposition level

$\mathbf{A_{ij}/D_{ij}}$ **:** wavelet coefficients

N : number of details or approximation co-efficient in each decomposition level

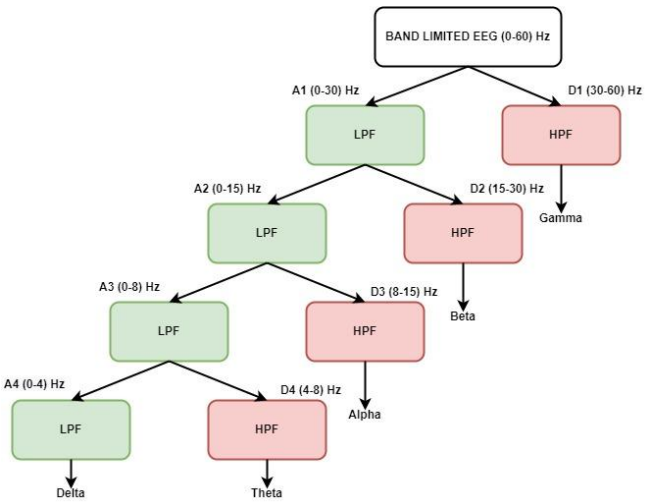

Fig 1.2 db4 Wavelet decomposition of EEG signal

IV. SYSTEM DESIGN AND IMPLEMENTATION

We implemented the hardware accelerator in the programmable logic fabric of the PYNQ-Z2 FPGA development board. It has the Zynq-7000 Programmable System on Chip (PSOC) which consists of a processing system (PS) and a programmable logic (PL). The PS is a hard Intellectual Property (IP) build using ARM Cortex-A9 dual core processor, which has Linux OS as the kernel. In the higher abstraction level, python scrips can be run on the Linux kernel to control the PS – PL Interfacing. The development of this project is done in three stages – developing a software-based FIR filter using python, developing a hardware prototype of the same FIR filter using Xilinx Vivado then implementing both designs and comparing the speed of execution.

A. Software Design

The afore-mentioned FIR filter for the db-4 wavelet transform algorithm is implemented in python which runs in the application layer of the PS part of Zynq-7000 PSOC. This software application uses the kernel running on the ARM Cortex A9 processor. The filter co-efficient are generated separately for each individual stage of the db-4 wavelet transform.

B. Hardware Design

The PL part is configured in this stage. Xilinx Vivado's IP integrator is used to develop the hardware design of the db-4 wavelet transform. FIR compiler (v7.0) from the IP repository is used to develop FIR filters with corresponding frequency specifications at each decomposition phase. Direct Memory Access (DMA) controller is utilized to bring data in and out of the PL. AXI (advanced extensible interconnect) is used to interface PS and PL. EEG signals are initially stored in the DDR of the PS part and then brought into the PL through DMA. The system clock provides necessary clock signals to the PS and the AXI bus.

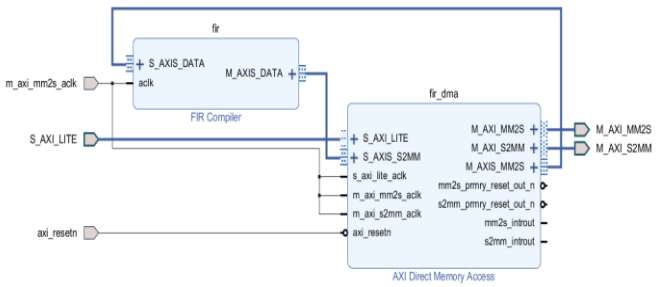

Fig 1.3 FIR Filter IP interfaced with DMA engine

C. Accelerating Function

FIR filter is implemented in python (PS) as well as in the FPGA fabric (PL). EEG signal is processed using both the filters and the time of execution is compared

D. Bitstream Generation

The block design is synthesized and implemented. The synthesis reports give information about the number of LUTs, BRAMs and DSP units utilized out of the available. The implementation reports show the power consumption of the entire design and the timing parameters. Finally, the bitstream is generated and dumped into the board.

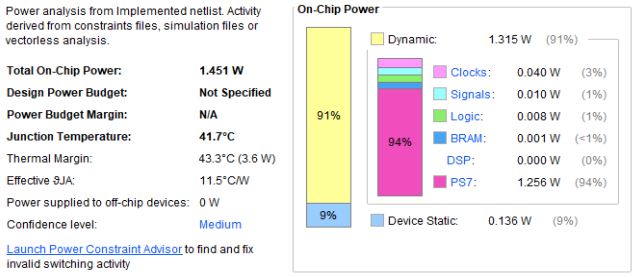

Fig 1.4 PYNQ Board Power utilisation

Site Type	Used	Fixed	Available	Util%
Slice	3126	0	13300	23.50
SLICEL	1861	0		
SLICEM	1265	0		
LUT as Logic	3314	0	53200	6.23
using O5 output only	0			
using O6 output only	2539			
using O5 and O6	775			
LUT as Memory	2895	0	17400	16.64
LUT as Distributed RAM	410	0		
using O5 output only	0			
using O6 output only	2			
using O5 and O6	408			
LUT as Shift Register	2485	0		
using O5 output only	384			
using O6 output only	1013			
using O5 and O6	1088			
LUT Flip Flop Pairs	4271	0	53200	8.03
fully used LUT-FF pairs	1806			
LUT-FF pairs with one unused LUT output	2310			
LUT-FF pairs with one unused Flip Flop	2321			
Unique Control Sets	296			

Fig 1.5 Resource utilisation of Accelerated FIR Filter

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	2	0	140	1.43
RAMB36/FIFO*	2	0	140	1.43
RAMB36E1 only	2			
RAMB18	0	0	280	0.00

Fig 1.6 Memory utilisation in FPGA fabric

Site Type	Used	Fixed	Available	Util%
DSPs	93	0	220	42.27
DSP48E1 only	93			

Fig 1.7 Utilisation of DSP units in FPGA fabric

V. IMPLEMENTATION

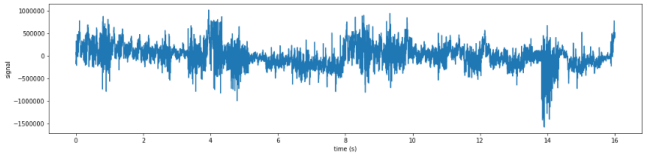

Fig 1.8(a) Input EEG signal

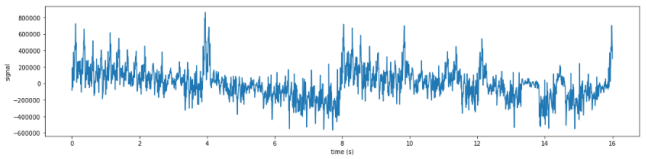

Fig 1.8(b) 60 Hz band-limited EEG signal

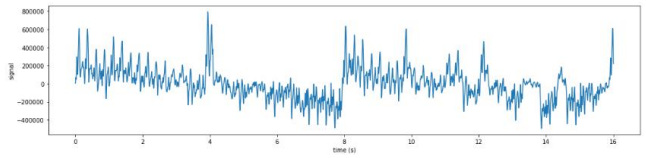

Fig 1.8(c) A1(0-30Hz)

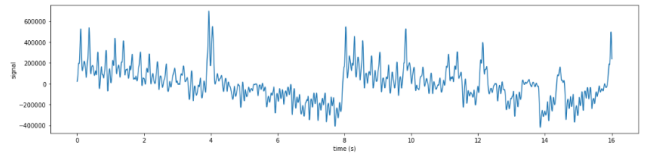

Fig 1.8(d) A2(0-15Hz)

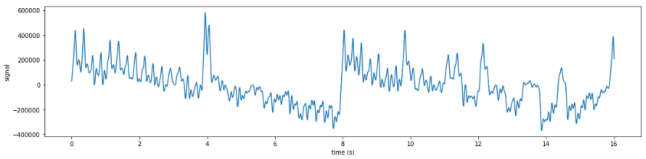

Fig 1.8(e) A3(0-8Hz)

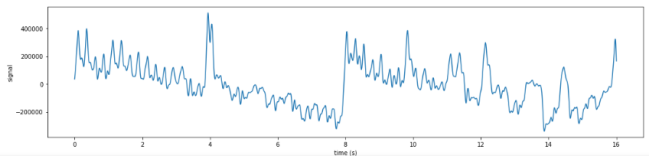

Fig 1.8(f) A4(0-4Hz)

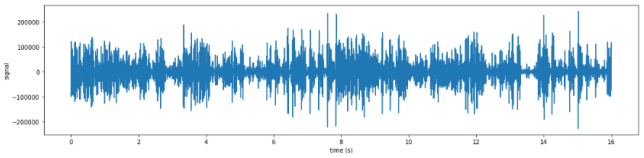

Fig 1.8(g) D1(30-60Hz)

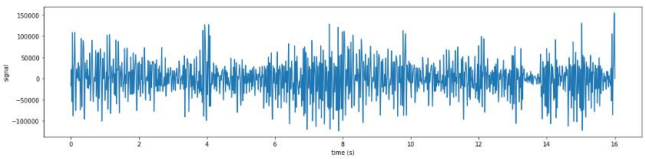

Fig 1.8(h) D2(15-30Hz)

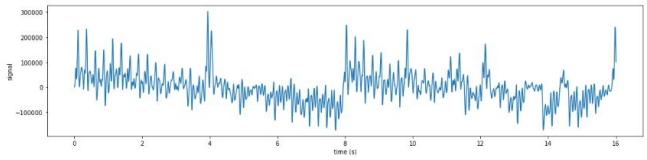

Fig 1.8(i) D3(8-15Hz)

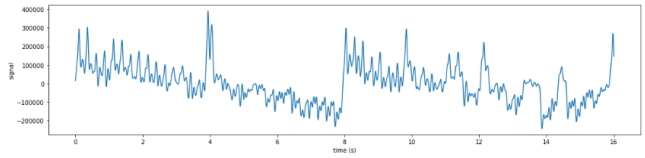

Fig 1.8(j) D4(4-8Hz)

A. Performance Comparisson

Hardware FIR execution time (ms) : 9.2634

Software FIR execution time (ms) : 19.3455

Hardware acceleration factor : 2.0883

Difference (ms) : 10.0821

VI. CONCLUSION AND FUTURE SCOPE

The main contributions of this paper are the Hardware acceleration of the FIR Filter. With the help of the PYNQ – Z2 FPGA development board the filtering results obtained were faster than the conventional method, an acceleration factor of 2 was achieved. This prototype can be used in the future and can be made as an ASIC. Furthermore, to improve this system Power Spectral Density (PSD) analysis can be added after the filtering process to find out the dominant frequency component in the considered EEG signal. A dedicated ML based design can be incorporated to assess the frequency and give the outputs based on the signal emitted from the brain.

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