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Performance analysis of NOR CAM cell using CMOS-HP, CMOS-LP and FinFET 16nm technology

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Abstract - *Content addressable memory (CAM) is used in many applications such as Network routers, Cache controllers and low power CPU design. It searches total memory array in one clock cycle. CAM cell contains memory cell and match circuit. Memory cell contains stored data and match circuit compares the input data and stored data. Search operation happens in parallel fashion, access time is less and power dissipation will be more. This paper presents functionality of NOR based CAM cell implemented using CMOS-LP, CMOS-HP, FinFET 16nm technology and power reduction in HSPICE tool.*

Key Words: NOR CAM; FinFET; CMOS-LP; CMOS-HP; HSPICE tool

1.INTRODUCTION

In present day scenario there is a need of better performance with respect to increase in speed with reduced power dissipation. The high frequency of CAM is achieved through scaling the transistors. Scaling of transistors leads to reduction in channel length. This will reduce the transit time of the charge carriers which increases the frequency of operation of the device [1]. In order to overcome short channel effects FinFETs has evolved. FinFETs has become an alternative because of its scalability and compatibility with planar CMOS [2].

Content addressable memory (CAM) is associative memory where data is given as input and address is given as output. The search operation in CAM happens in parallel fashion and hence CAM is faster which causes high power dissipation and less access time [3]. In the Fig 1, the data is sent to the search data register through searchlines to the memory cells. This input data is compared with the stored data. When the stored data is matched with the input data, the corresponding match line will be enabled. The address of the matched data will be considered as the output.

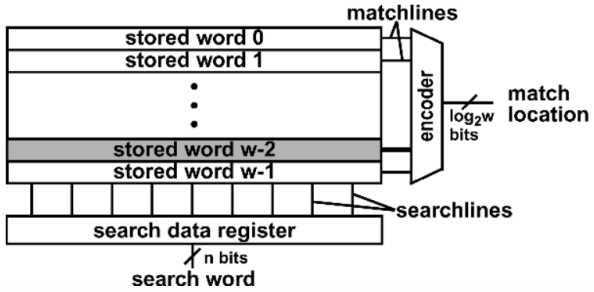

Figure 1. CAM conceptual diagram

1.1 CMOS

Both NMOS and PMOS has similar characteristics during on and off state and hence it is used in CMOS Technology to realize various logic functions. Over Bipolar or the previous popular NMOS technologies CMOS technology has extremely low power consumption in static conditions as they draw power only during switching operation. This allows integrating much larger number of logic gates on the VLSI IC when compared to Bipolar or NMOS technologies.

In order to implement CMOS-HP the VDD and Vth is kept lower in order to improve the speed in performance. Likewise, in order to implement the CMOS-LP the VDD and Vth will be high in order to reduce the power dissipation in transistor.

1.2 FINFET

FinFET is a three-dimensional transistor which is made on Silicon wafers (Bulk FinFET) or silicon on insulator (SoI FinFET). It is made of a thin fin material embedded on a substrate. Channel will be fully wrapped around by the gate of device, which have control over channel as shown in Fig 2 [4].

Continuous scaling of MOSFET to lower technology nodes has become very challenging aspect. Due to short channel effects and leakage current issues made a way to the evolution of FinFET technology.

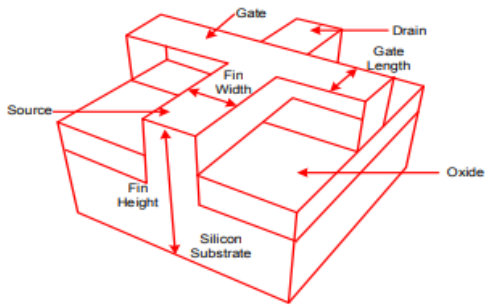

Fig 2. Structure of FinFET

Most widely used operating modes of FinFET are explained below. FinFET structure consists of two gates namely, front end(G1) and back end(G2) as shown in Fig 3.

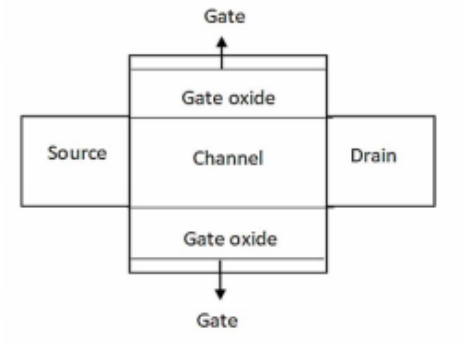

Fig 3. Cross section view of FinFET

A. Independent gate mode

The area consumption is more and the front gate and the back gate are operated individually.

B. Shorted gate mode

The switching speed is more and it has good resistance when compared to other modes, as both the front and back gates are shorted.

C. Reverse bias mode

In the reverse bias mode, in order to suppress the effects of sub threshold leakage current the back gate of FinFET is associated to a reverse bias voltage.

2. METHODOLOGY

A CAM cell has two basic functionalities: storing a bit in SRAM and comparison of a bit. NOR-type CAM cell is shown in Fig 5. The comparison between $\overline{D}$ and D which are stored in memory, and the search data is sent on the search line $\overline{SL}$ and SL. By using dynamic XNOR logic comparison circuit the output is drawn from matchline ML. The mismatch of D and SL activates the pulldown path, connects ML to ground. When there is a match in D and SL disables the pulldown path and ML remains in VDD [5].

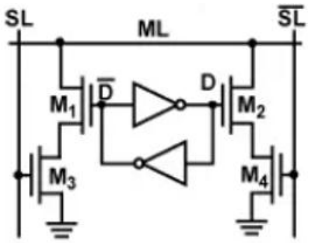

Fig 4. 10 - T NOR type CAM cell

3. CIRCUIT IMPLEMENTATION

A CAM is a special type of memory device which implements a look-up table function. A CAM is classified into two types, binary CAM and ternary CAM.

A. Binary CAM (BCAM)

Binary CAM will cache only '0' and '1'. It is used in applications which need exact match between the stored data and input data. Table1 represents truth table of the BCAM

Table 1. Truth table of BCAM

Store data	Search data	Outcome
0	0	1
0	1	0
1	0	0
1	1	1

B. Ternary CAM (TCAM)

Ternary CAM stores three states '0', '1' and 'X'. The 'X' state is additional state referred to as the "mask bit" or "don't care bit". TCAM is used for applications for both exact and partial matches. Table 4 represents truth table for TCAM [6].

Table 4. TCAM truth table

Store data	Search data	Outcome
0	0	1
0	1	0
0	X	1
1	0	0
1	1	1
1	X	1

X	0	1
X	1	1
X	X	1

4. WORKING

4.1. CAM cell with XNOR transistor logic

Fig 5. shows SRAM based BCAM cell using XNOR transistor logic circuit. The data is stored and read similar to SRAM at node Vx while searched data is sent to lines SL and SLB. When there is a mismatch between stored data and searched data, match line voltage is discharged to GND and mismatched outcome is presented.

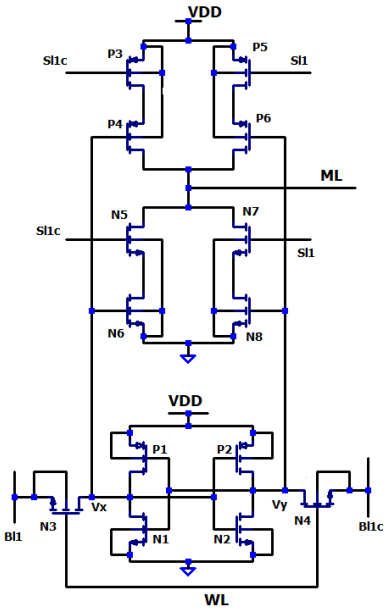

Fig 5. BCAM with XNOR transistor logic

Fig 6. shows SRAM based TCAM with XNOR transistor logic circuit as a compare circuit, where data is stored in node Vx at SRAM1 and Vy at SRAM2.

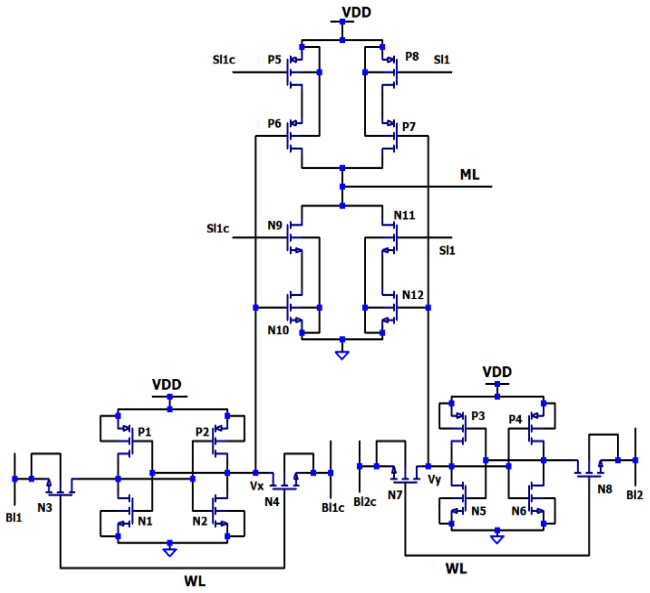

Fig 6. TCAM with XNOR transistor logic

Table 2 Truth table for BCAM XNOR with Transistor circuit

Vx	Vy	SL1c	SL1	PUP	PUD	ML
1	0	1	0	ON	OFF	1
1	0	0	1	OFF	ON	0
0	1	1	0	OFF	ON	0
0	1	0	1	ON	OFF	1

4.2. CAM cell with XNOR logic using transmission gate

Fig 7. shows SRAM based BCAM cell using XNOR transmission gate logic circuit. The CAM operation happens the same as discussed in previous sections. In BCAM XNOR transistor logic, the transistor count is more as we can see in Fig 5. Thus, transistor XNOR logic circuit is replaced with transmission XNOR logic circuit in match circuit. Fig 8. shows SRAM based TCAM with XNOR transmission gate logic circuit.

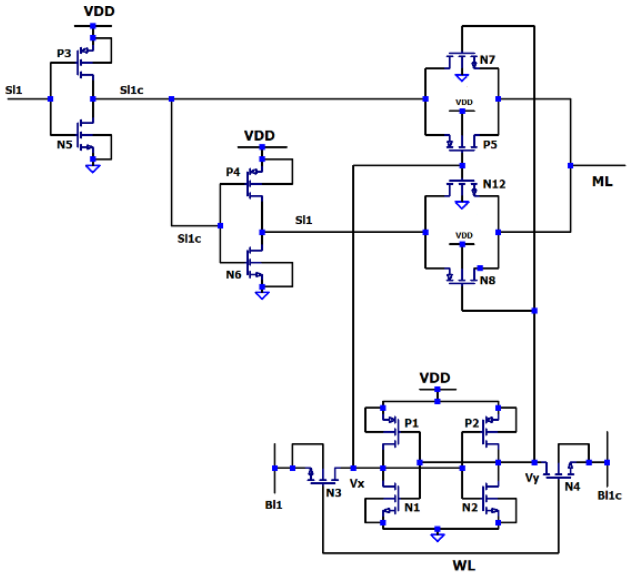

Figure 7. BCAM with XNOR Transmission gate logic

Table 2 Truth table for CAM XNOR with Transmission gate

Vx	Vy	SL1	SL1c	Pass1	Pass2	ML
1	0	1	0	0	1	1
1	0	0	1	0	1	0
0	1	1	0	1	0	0
0	1	0	1	1	0	1

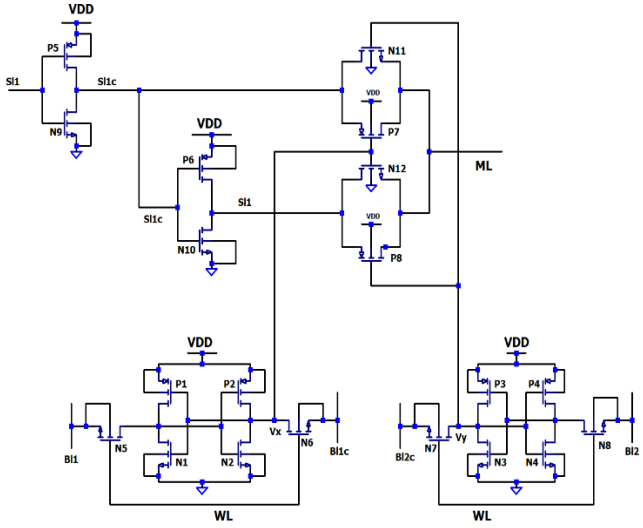

Fig 8. TCAM with XNOR transmission gate

4.3. CAM cell with XNOR logic using novel comparison circuit

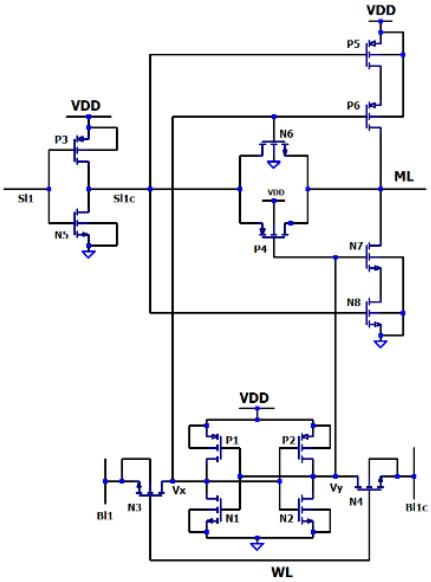

Figure 9. BCAM with XNOR switch stack logic

Fig 9. shows SRAM based BCAM cell using XNOR switch stack logic circuit. The operation of the CAM cell is discussed in the above section. In previous section 1.b. the power dissipation is more. Hence in this section the proposed circuit reduces the power dissipation. The working of this circuit is understood with the help of the truth table. Fig 10. shows SRAM based TCAM with XNOR transistor logic circuit.

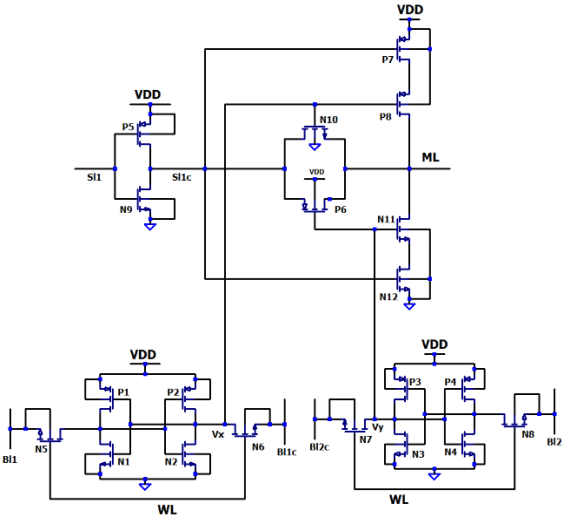

Fig 10. TCAM with XNOR switch stack

Table 3. Truth table for BCAM XNOR with switch stack logic

Vx	Vy	Sl1	Sl1c	Pass	P4	P5	N7	N8	ML
0	1	1	0	0	1	1	1	0	1
0	1	0	1	0	0	1	1	1	0
1	0	1	0	1	1	0	0	0	0
1	0	0	1	1	0	0	0	1	1

5. RESULTS AND SIMULATION

All the CAM operations is performed in 16nm technology by using CMOS-LP, CMOS-HP and FinFET. Power and delay values are compared for each of the circuit described above.

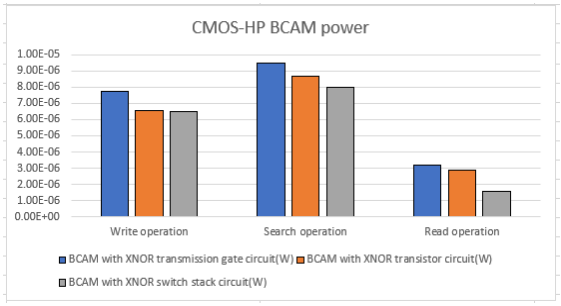

Figure 11. Power measurements of CMOS-HP BCAM

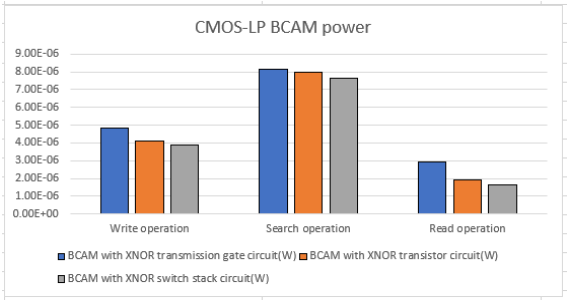

Figure 12. Power measurements of CMOS-LP BCAM

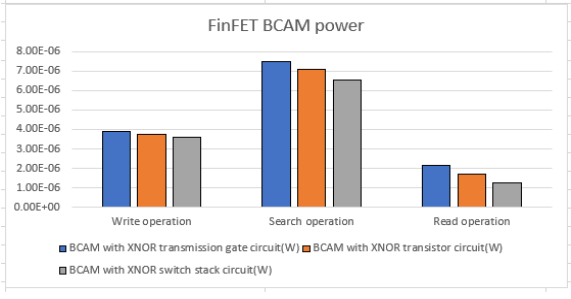

Figure 13. Power measurements of FinFET BCAM

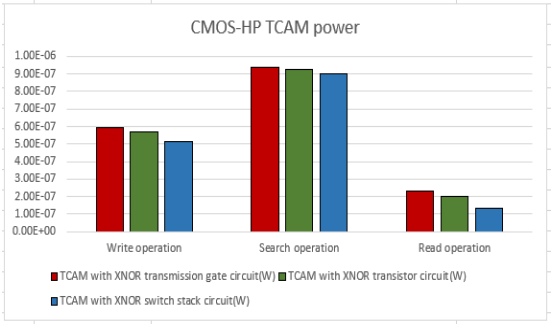

Figure 14. Power measurements of CMOS-HP TCAM

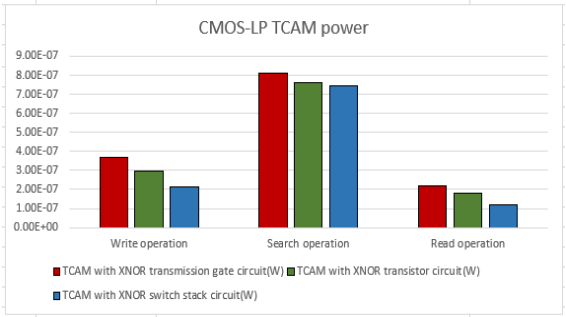

Figure 15. Power measurements of CMOS-LP TCAM

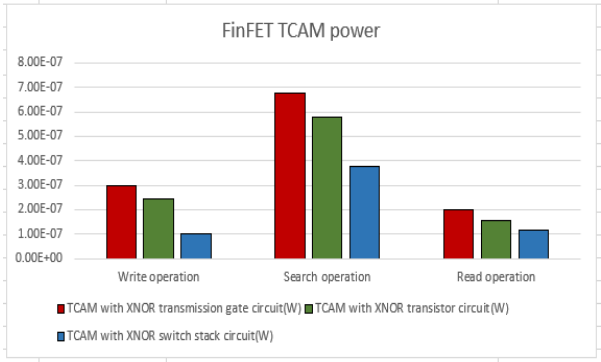

Figure 16. Power measurements of FinFET TCAM

Table 4. Average power of CAM (W)

	CMOS-LP	CMOS-HP	FinFET
BCAM	4.7281E-06	1.4406E-04	1.1597E-06
TCAM	1.0749E-03	4.7961E-05	4.0095E-05

By comparing the obtained values, we can see that there is 15% - 19% reduction in power dissipation in FinFET BCAM when compared other circuits. 19% - 25% if power dissipation in reduced in FinFET TCAM when compared with other circuits.

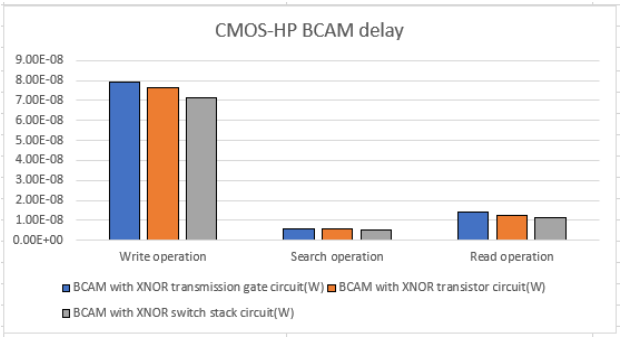

Figure 19. Delay measurements of CMOS-HP BCAM

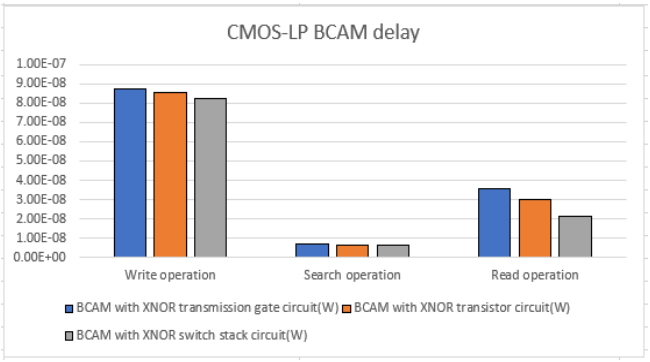

Figure 17. Delay measurements of CMOS-LP BCAM

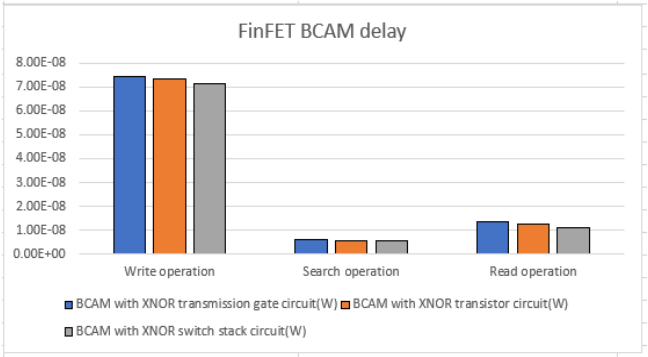

Figure 18. Delay measurements of FinFET BCAM

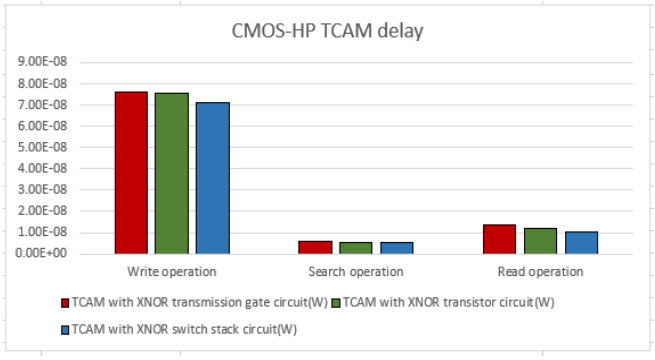

Figure 19. Delay measurements of CMOS-HP TCAM

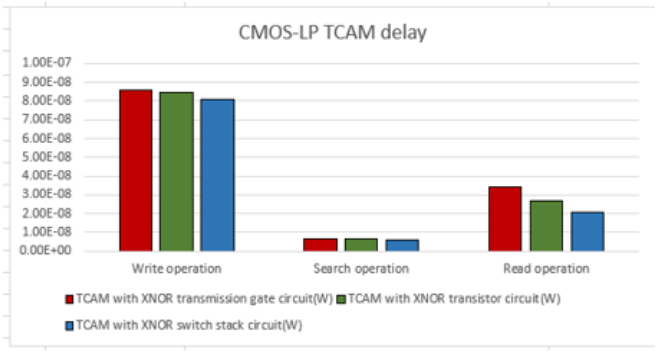

Figure 20. Delay measurements of CMOS-LP TCAM

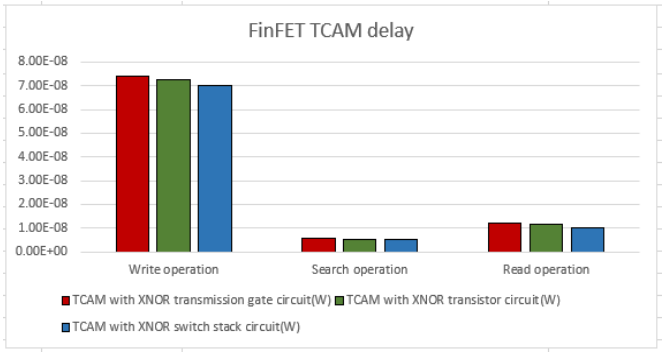

Figure 21. Delay measurements of FinFET TCAM

Table 7. Average delay of CAM (s)

	CMOS-LP	CMOS-HP	FinFET
BCAM	4.8487E-08	3.5348E-08	3.0531E-08
TCAM	4.0112E-08	3.1738E-08	3.0201E-08

From the obtained delay values, there is 20% - 24% reduction of delay in FinFET BCAM when compared other circuits. Around 27% - 37% of reduction in delay is seen in FinFET TCAM when compared to other circuits.

6. CONCLUSIONS

This project explains the design and working of CAM which consists SRAM as memory cell and XNOR as comparison circuit. By adopting different technologies, the performance of BCAM and TCAM are investigated. The CAM operations are carried out by using CMOS-LP, CMOS-HP and FinFET technology and obtained power and delay values are compared for different compare circuit. From the experiment, FinFET CAM cells with XNOR switch stack circuit gives better performance with less power dissipation and delay when compared to other logic circuits in all the technology nodes.

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