International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 10 Issue: 04 | Apr 2023 www.irjet.net p-ISSN: 2395-0072

Three Phase Seven-level Triple Voltage Booster Switched-Capacitors based Multilevel Inverter with Minimum Components

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Abstract: ***This research proposes an economically feasible 3-phase triple-gain switched-capacitor (SC) multilevel inverter (MLI) configuration. The proposed structure has one source and uses the fewest switching components possible to produce an output voltage waveform with seven levels from line to line. The newly proposed SCMLI configuration features a built-in capacitor voltage balancing capability and uses two switching capacitors per phase leg. Level shift pulse width modulation approach, operating theory, and structural description have all been discussed. To demonstrate the merits of the proposed work with the existing topologies, a fair comparison study has been provided. The simulation results show that the proposed SCMLI configuration is feasible and has been verified theoretically.***

Keywords: *Three Phase Multilevel Inverter; Seven Level MLI; Economically Feasible Inverter Design, SCMLI.*

1. Introduction

The population and industrialization are expanding quickly, which increases the usage of traditional energy sources and greenhouse gas emissions [1]. There has been a lot of focus on sustainable energy sources as a way to slow down the rate at which conventional energy sources are used up. However, electricity is produced by a variety of renewable energy sources, including solar photovoltaic, wind, and fuel cells. Solar and wind are the most widely used renewable energy sources due to their accessibility, environmental friendliness, and improvements in power semiconductor technology. Due to the relatively low output power from this source, it will not meet the requirements for power quality for applications like electric and fuel cell vehicles, grid connections, and industries. As a result, a transformer or boost converter must be used to increase the output voltage. The use of the transformer makes the system big and expensive. An extensive amount of study has been done on the converter to increase the output voltage. Among these converters, multilevel inverters are essential for power conversion owing to improved power quality, enhanced performance, and low, medium, and high-power applications.

The cascaded H-bride (CHB), the flying capacitor (FC), and the neutral point clamped (NPC) inverter are the three primary topologies of the conventional multilevel inverter [2]. Every topology has advantages and disadvantages. A modularity feature, for example, is present in the common CHB. However, the need for isolated DC sources is its principal drawback. For NPC and FC topologies, the availability of clamping diodes and capacitors, respectively, and the accompanying voltage balance concerns provide a difficult problem. The uses of conventional inverters are constrained by these undesirable characteristics. In this context, research has concentrated on designing MLIs topologies that use the fewest possible power electronic components while still producing improved voltage waveforms [3, 4]. The ability to increase voltage is a key worry with such topologies, though. Researchers from all over the world have looked into the switched capacitor (SC) concept as a way to lessen the aforementioned limit. Such MLIs structures based on SC display exceptional voltage boosting capabilities, capacitor self-voltage balancing, and a greater number of levels due to its modularity characteristic. Based on the SC principle, the topologies [5-7] have properties of modularity. These designs are, however, constrained by high voltage stress on the power switching devices. A basic cell unit can generate an output voltage waveform with seven levels using the topology described in [8]. Despite having a symmetrical voltage source, the topology is less desirable and more expensive due to the need for numerous sources and a polarity generator. The gain is lower and there are more switching components in the architecture [9-11]. Another seven-level topology [12] also employs more switching components while gaining less than unity. The arrangement [13] has seven levels and three times the input voltage source's voltage boosting capabilities, furthermore, its drawback is that it causes undesirable voltage stress across the switches. Voltage boosting is not possible with the designed structure for the topologies shown in [14-17]. An innovative ANPC inverter that may generate maximum voltage levels while maintaining unity or a higher voltage gain was explored in the structures in [18–21]. Moreover, the overall component count is decreased, and complex balancing controls are not necessary. In [22], a unique SC T-type inverter is presented that soft-charges its integrated switching capacitors to

minimize current spikes. A nine-level single-source design built on the SC principle is suggested in the article [23], but it has fewer components than traditional topologies. The amount of parts required to reach the appropriate level is still considerable, though. In order to accommodate the extra switches, driver circuitry must be added, which raises the system's cost and increases power loss. Neutral Point Clamped Inverters (NPCI), which generate three-level alternating current (AC) output in a single stage, are recommended for usage in boosting DC voltage to the required level [24, 25]. In the article [26], designing a single phase hybrid multilevel inverter for a standalone system that produces three levels of T-type leg and three levels of diode clamped leg using asymmetrical voltage input sources is discussed.

The majority of topologies, it has been shown through a survey of the literature, have a number of demerits, including increased power devices, high voltage stress across the switches, low voltage gain, and absence of enhancing ability. Therefore, the ideas in the aforementioned statements have been employed to develop the alternative SC-based inverter configuration that is discussed in the proposed work. The following are the primary characteristics of the recommended topology:

a) The magnitude of the voltage boosting capability is three.

b) The inbuilt ability of capacitors to balance their voltages.

c) It decreased the number of switching components.

d) Use of a single source,

e) Only about 50% of switching parts are functional at any voltage level.

2. The Proposed 3-Φ SCMLI Topology

A. Circuit Description

The 3-Φ SC MLI structural design is depicted in Figure 1. Six power switches (S_{Xi} i.e., 1, 2, ...,6) are used in each phase leg, together with a power diode (D_X), two capacitors (C_{X1} and C_{X2}), and a single DC source, where X ∈ the phase (R, Y, B). Any renewable energy source or battery can provide power to this voltage source. The proposed SCMLI can produce a seven-level voltage waveform across the load ends when the line-to-line voltage is taken into account (0, $+1V_{DC}$, $+2V_{DC}$, and $+3V_{DC}$), but when the pole voltage V_{RO} is taken into account, the proposed structure can only produce four levels: 0, $\pm V_{DC}$, $\pm 2V_{DC}$, and $\pm 3V_{DC}$. All the used power switches have peak inverse voltages (PIV) equal to that of the input supply voltage except for S_{X5} and S_{X6}. The proposed structure demonstrates symmetry in all three phases, thus focusing on only one phase leg (R) will help you better understand the analysis. Table 1 enlists all the appropriate switching modes. In the mentioned table, '1' and '0' stand for the switches ON and OFF states, respectively. Capacitor charging and discharging are represented by the letters 'C' and 'D'.

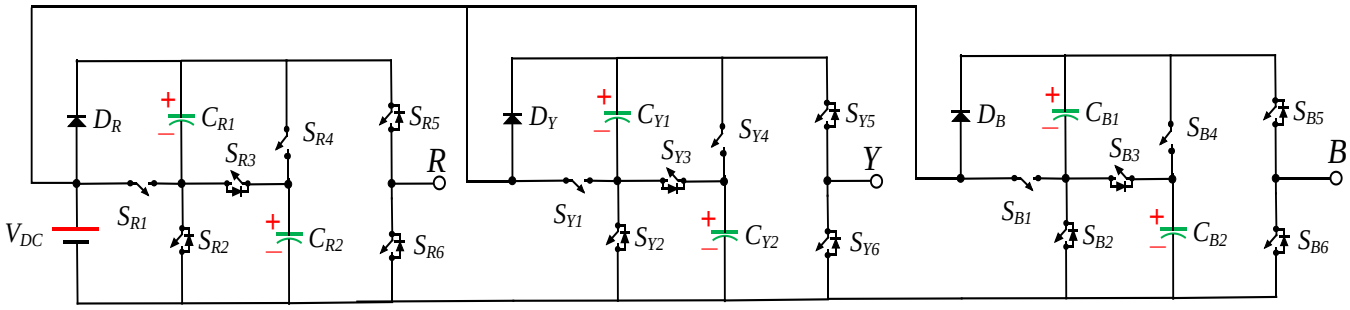


Fig.1. Proposed 3-Φ SCMLI topology

B. Different operational modes of the proposed topology

This section explains the basic operation of single phase. The remaining two phases can be analysed similarly. The techniques outlined below can be used to characterise Phase R:

Mode 1: In this mode, two switches are operated, causing output voltage levels across the R and n terminals to be zero (see Table 1). The capacitor C_{R1} is charged to v_{DC}, whose magnitude is equivalent to the input voltage source, as a result of the switch S_{R2} being activated. Fig. 2a depicts the analogous circuit for this device. The capacitor's charging path is depicted here in blue, while the current flowing through the load terminals is shown in red lines.

Mode 2: In this mode of operation, the switches S_{R2} and S_{R5} are turned on to provide this voltage level and to charge the capacitors C_{R1} to a level that is equal to the DC link source, as depicted in Fig. 2b.

Mode 3: The proposed topology generates a voltage level that is double the input voltage supply magnitude in this mode of operation ($2V_{DC}$). The following power switches S_{R1}, S_{R4}, and S_{R5} are turning on, which connects capacitor C_{R1} in series with the source of the input voltage and charges capacitor C_{R2} to $2V_{DC}$. As a result, the load terminals generate the output level of $2V_{DC}$, as shown in Fig. 2c.

Mode 4: In this mode, the source of the input voltage is linked in series with both capacitors: C_{R1} and C_{R2}, output voltage of $3V_{DC}$ is measured across the load terminals. The mode 4 operation for the indicated structure is shown in Fig. 2d.

Table 1 Switching states for pole voltage of phase leg 'R'

Mode	Active switch						$V_{RO}(t)$	Capacitors effect	
	S_{R1}	S_{R2}	S_{R3}	S_{R4}	S_{R5}	S_{R6}		C_{R1}	C_{R2}
I	0	1	0	0	0	1	0	C	-
II	0	1	0	0	1	0	$1V_{DC}$	C	-
III	1	0	0	1	1	0	$2V_{DC}$	D	C
IV	0	0	1	0	1	0	$3V_{DC}$	D	D

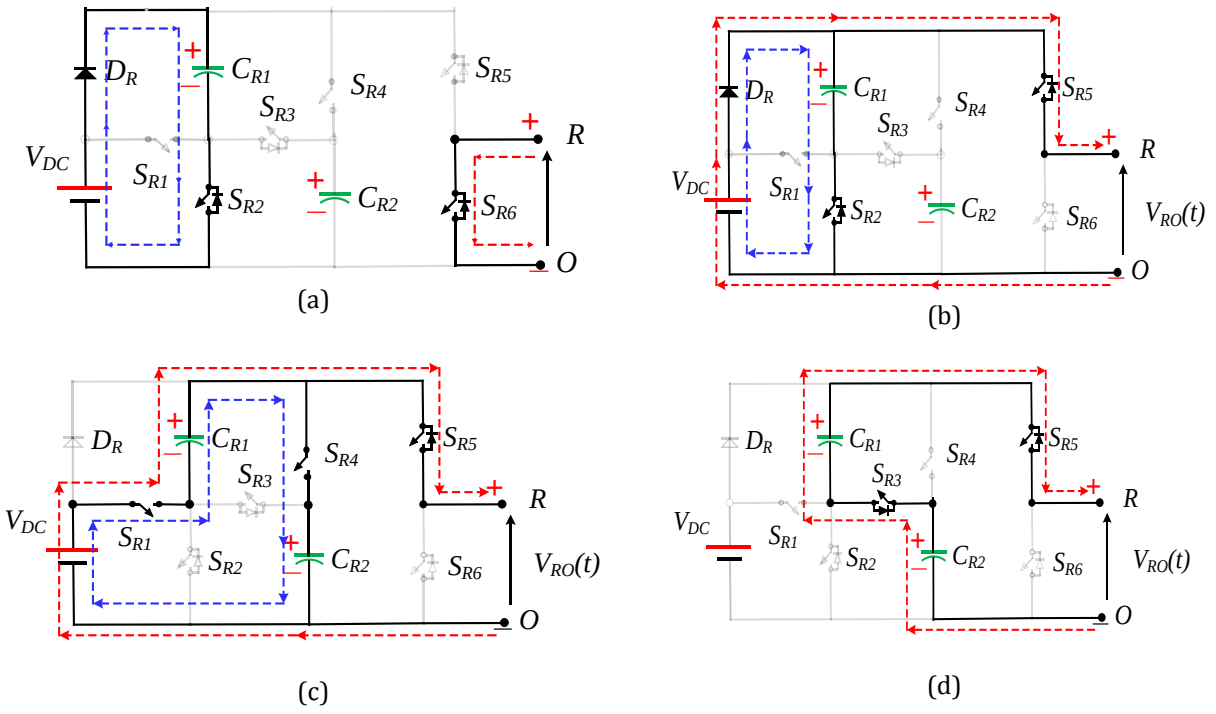


Fig. 2. Shows the different modes of operation of the pole voltage (a)$V_{RO}(t) = 0$ (b) $V_{RO}(t) = +1V_{DC}$ (c) $V_{RO}(t) = +2V_{DC}$ (d) $V_{RO}(t) = +3V_{DC}$

3. Switching methodology

Theoretically, high frequency switching techniques such as: multicarrier pulse with modulation, space vector pulse width modulation, etc. or low switching frequency schemes such as: active harmonic elimination, selective harmonic elimination, etc. can be used to modulate the proposed SCMLI configuration with the appropriate adaption [21–23]. A multicarrier PWM method as described in [24] is used in this paper to demonstrate how the suggested topology operates. Figure 3 depicts the scheme, while as carriers, six 2 KHz-frequency triangle waveforms are used. They are set up in an opposing phase configuration [25].

The reference signal is a sinusoidal waveform at 50 Hz frequency with a randomly selected modulation index of 0.95. The carrier signals and the reference signal are continuously compared. Comparators output '1' for carrier signals above the zero reference if the reference is greater than the associated carriers and '0' otherwise. Comparators output '0' for carrier signals below the zero reference if the reference is bigger than the associated carriers, and '-1' otherwise. The output signals from the comparator are combined to produce an aggregate signal (t). Furthermore, in order to generate switching pulses from signal a one-to-one relationship between the levels present in signal a(t) (aggregated signal) and the levels desired in the output waveform is used. This is done by comparing the signal a(t) to the constants. The signals thus acquired are applied to power switches succeeding to the level utilizing the mapping depicted in Fig. 3 to control the switches.

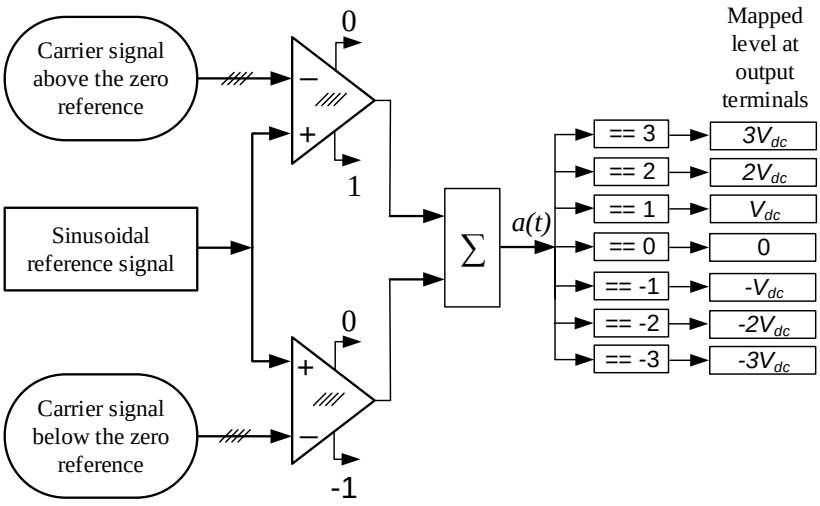


Fig.3. Switching scheme for the proposed 3-Φ SCMLI

4. Simulation results and discussion

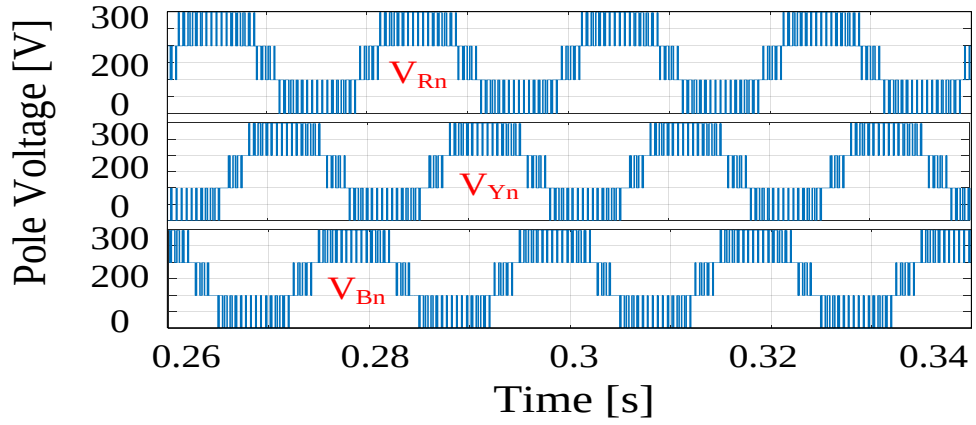
The proposed structure has been validated using the MATLAB/Simulink platform to confirm the broad conceptual concept. Using the technique outlined in the section above, high frequency carrier signals have been carefully chosen for modulation. Table 2 lists the circuit design parameters used on the Simulink platform for the verification of the proposed SCMLI structure.

The theoretical idea of the proposed topology is supported by simulation outcomes. Fig. 4 and Fig.5 show the outcomes of the simulation with RL-load. In Fig. 4a, the pole voltage is shown with four equal step sizes (0, + 100 V, + 200 V, + 300 V). Fig. 4b shows the three-phase line voltage. Line voltage has seven levels (0, 100V, 200V, 300V), as can be seen from the waveform. The resistive-inductive load current under step-change load conditions is shown in Fig. 5a. Fig. 5b illustrates the impact of the load change on line voltage, line current, and capacitor voltage for phase R for easier analysis. This reveals that even when the load varies, the capacitor retains its natural balance and that the line voltage's magnitude is unaffected.

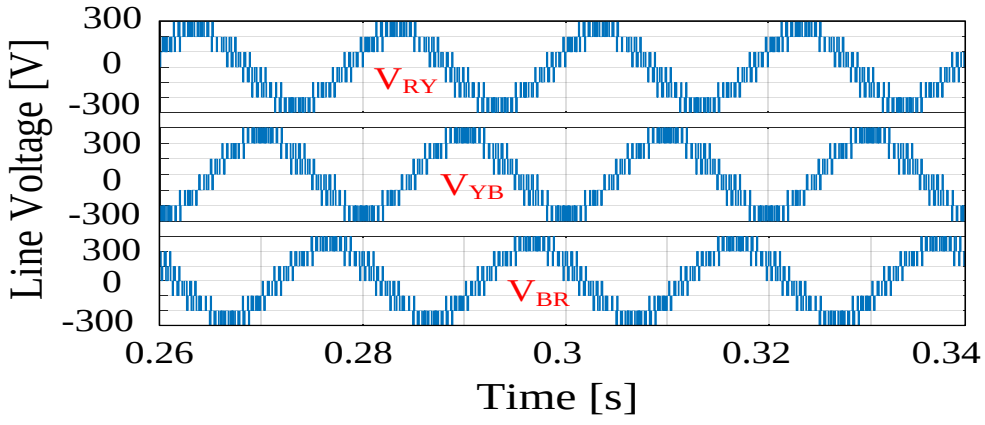
Table 2 Simulation parameters

Parameter	Specification
Input DC source(V_{DC})	100V
Output frequency(f)	50Hz
Carrier frequency($c_x(t)$)	2kHz
Resistive-Inductive Load	R=50Ω, L=80mH
Capacitors (C_{Xi})	C_{X1}=6000μF,C_{X2}=4700 μF
Power Switches	IGBTs
Modulation index (Ma)	0.95

The voltage stresses over various switches are shown in Figure 6a. When the R-L load of R = 50, L = 80 mH is taken into account, the FFT analysis of V_{RY} yields the highest magnitude of the fundamental voltage of 171.6V with 31.08% of total harmonic distortion (THD), as shown in Fig. 6b. Similar to this, the FFT analysis of i_{RY} yields a fundamental current peak magnitude of 1.775A with 1.45% THD as shown in Fig. 6c. It captures steady-state values of 100V and 96.5V over Cx1 and Cx2, respectively. It also mentions that C_{x1} and C_{x2} have peak-to-peak ripple values of about 2.5 V and 2 V, respectively.

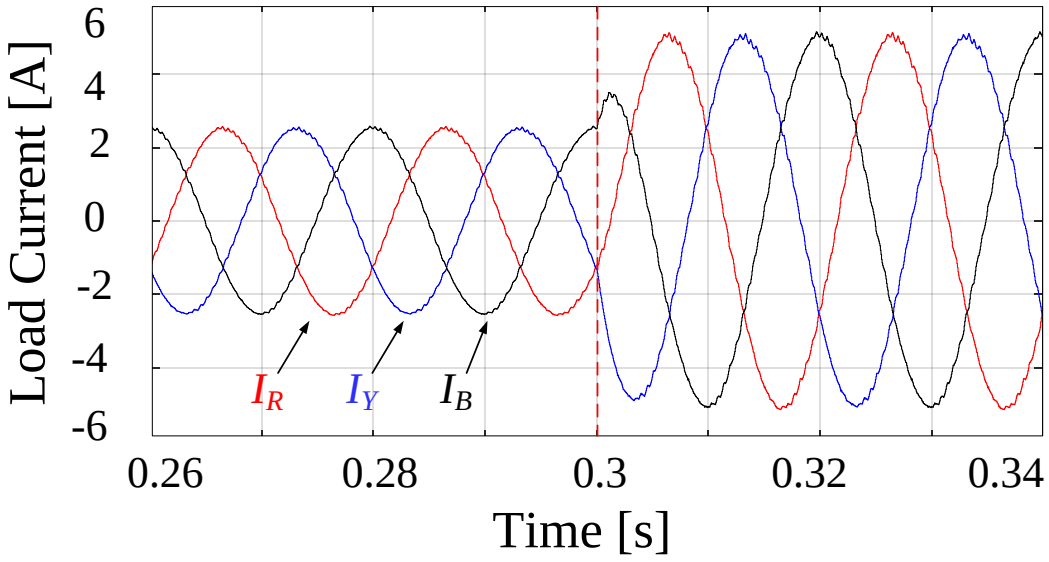


(a)

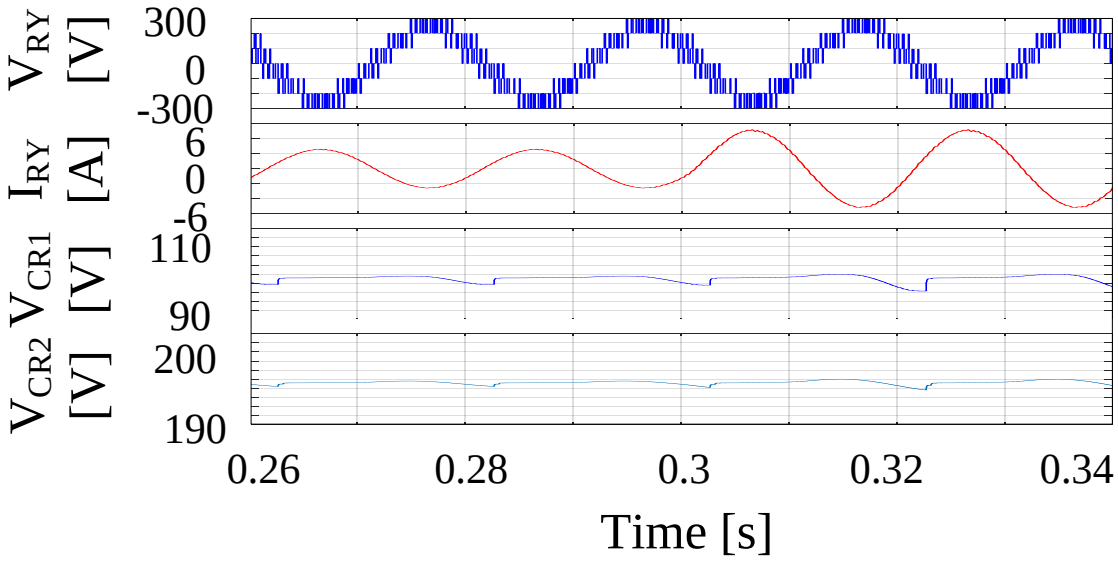


(b)

Fig.4. Simulations results for proposed 3-Φ SCMLI topology: (a) pole voltage, (b) line voltages

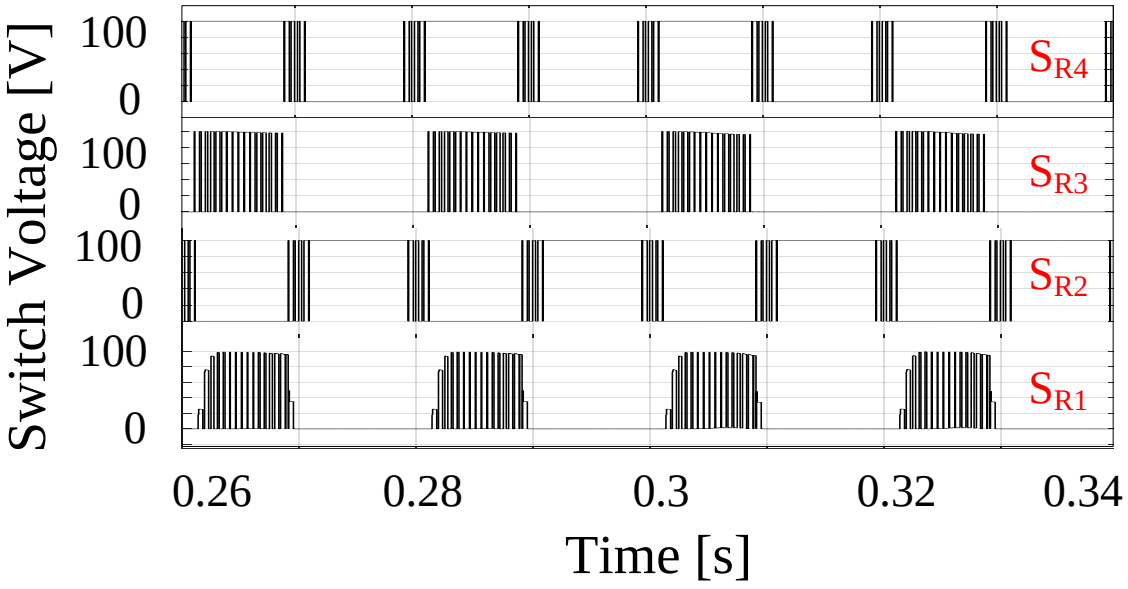


(a)

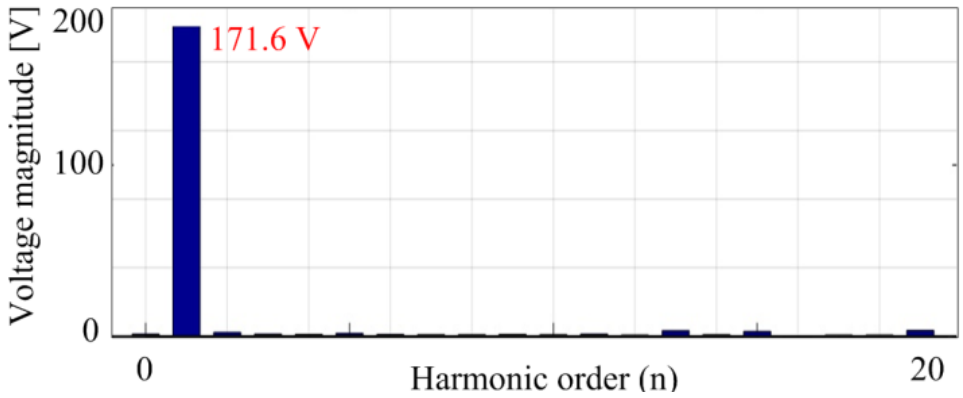


(b)

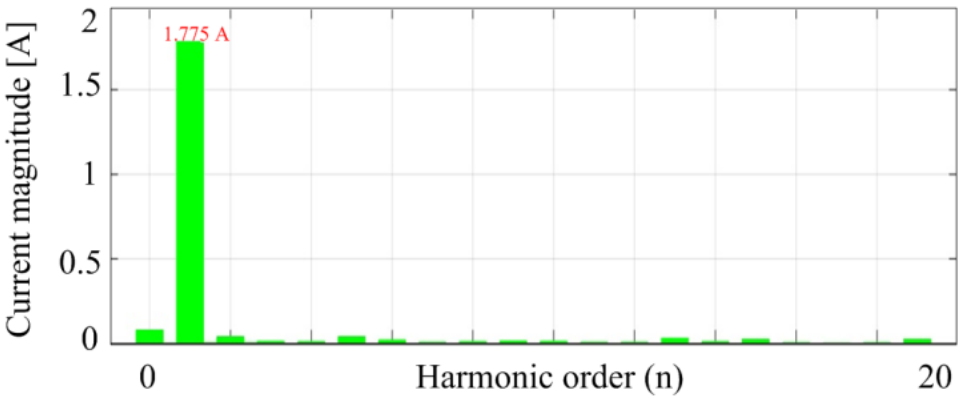
Fig.5. Simulations results: (a) load current (b) line voltage, load current and voltage across capacitors



(a)



(b)



(c)

Fig. 6. Simulation results of (a) voltage stress across switches (S_{R1}, S_{R2}, S_{R3} and S_{R4}), (b) Voltage waveform FFT analysis, (c) Current waveform FFT analysis.

5. Comparison of Proposed SCMLI with existing 3-Φ MLI topologies

The primary goal of the presented topology is to produce the highest number of output voltage levels with the fewest possible power devices and capacitors at the lowest possible cost. The Component to Level Factor ($F_{C/L}$) and the Cost Function (CF) are two variables that quantify the merits of the suggested topology in this context (CF). The equation below defines the cost function and the factor component to level factor ($F_{C/L}$).

$$F_{C/L} = \frac{N_{SW} + N_C + N_{AD} + N_{Dri} + N_S + N_{BD}}{N_{L1}} \quad (1)$$

And,

$$CF = \frac{(N_{SW} + N_C + N_{AD} + N_{Dri} + N_{BD} + \propto TSV) \times N_S}{N_{L1}} \quad (2)$$

Here, the notations represent number of power switches = N_{SW}, capacitors = N_c, auxiliary diodes = N_{AD}, sources = N_S, number of pole voltage level = N_P, driver units = N_{Dri}, pole voltage levels = N_{L1}, body diodes = N_{BD}, and line-to-line voltage levels = N_{L2}. α is the weight factor and number of the inductors = N_I.

For a certain number of pole voltage levels, Table 3 includes component count, cost function, total standing voltage, and voltage gain that compares the proposed topology to the existing 3-Φ SCMLI structures. Multiple isolated DC sources are present in the topologies described in Ref. [14, 15, 20] to raise the voltage level. The topology in reference [12, 14, 15, 17, 20] has a poor ability to increase. Despite having the potential to raise voltage, the topologies in ref [9–11] are only 1.5 times as effective as the proposed one. Additionally, the proposed topology has a lower CF than recent topologies. The least expensive topology, however, is [12, 17]. It requires a boosting circuit, which adds expense and complexity.

Table 3 Comparison of proposed SCMLI (P) with the recent MLI topologies

Sl.no	N_{L1}	N_{L2}	N_{SW}	N_S	N_{AD}	N_I	N_{BD}	N_{Dri}	N_C	TSV_{pu}	$F_{C/L}$	MBV	Gain	Boosting ability	CF/gain
[9]	4	7	10	1	-	-	10	9	4	6	8.5	1	1.5	Yes	6.5
[10]	4	7	9	1	-	-	9	8	3	5.33	7.5	1	1.5	Yes	5.72
[11]	4	7	10	1	-	-	10	9	3	5.33	8.25	1	1.5	Yes	6.22
[12]	4	7	8	1	-	-	8	8	3	4	7	1	0.75	No	10.33
[14]	3	5	4	2	-	-	4	4	-	5	4.66	2	1	No	11.33
[15]	4	7	6	4	8	-	4	6	-	17.33	7	3	0.75	No	23.73
[17]	4	7	8	1	-	-	8	8	4	5.5	7.25	1	1	No	8.387
[20]	3	5	4	2	-	-	4	4	-	5	4.66	2	1	No	11.33
[P]	4	7	6	1	1	-	6	6	2	4	5.5	3	3	Yes	2.08

TSV: Total Standing Voltage, **MBV**: Maximum Blocking Voltage

6. Conclusion

A three-phase SC inverter that boosts voltage effectively is described in this article. The suggested design is notable for having the fewest active and passive switching components per level, lower cost function values, and self-balanced capacitor voltage. Due to these aspects, it is envisaged that the suggested topology will mostly be employed for solar panels, fuel cells, and electric cars. The presented module synthesises seven levels using power switches that are all rated at the same voltage as the input dc source. The proposed module is determined and analyzed and its MATLAB/Simulink simulation is described in this paper. A fair comparison of the newly presented SCMLI structure with other switched capacitors-based topologies further demonstrates its superior performance and competence in terms of semiconductor requirements.

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