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Analysis of Vedic Multiplier using Different Adder Topologies

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Abstract — Vedic based maths multiplier has history and high speed. Adder is one of the main tools used in this technology. The use of a fast tone enhances the overall Vedic performance. In this work, a comparative study is done using different integration methods in the Design Process with standard libraries at 32/28 nm. Different adder topologies are used such as Ripple Carry Adder (RCA), Carry Select Adder (CSA), Square Root Carry Select Adder (SQRT-CSA), Common Boolean Logic (CBL) and Binary to Excess One Converter (BEC) used to compare area, delay and power. Designs for 8-bit, 16-bit, 32-bit and 64-bit Vedic multipliers are made using the above adders. 64-bit Vedic multiplier using SQRT-CSA integrator was found to be about 5% faster than RCA-CSA and BEC, 75% faster than CBL and RCA.

Keywords:-Vedic Multiplier, RCA, CBL, BEC, CSA, SQRT-CSA, Multiplicative multiplier, Power, Delay, Area.

I. INTRODUCTION

Amplification is widely used in digital signal processing applications, so high amplification is necessary. This paper presents a system design approach for a fast and efficient network based on Vedic arithmetic [1]. The Multiplier Architecture is based on the Vertical and Crosswise algorithm of ancient Indian Vedic arithmetic. The fixed block used in the Vedic multiplier is a major source of delay in the entire development process.

This is what this document looks like. Part-II describes the principle for operation based on Vedic Algorithm. Part-III deals with different topologies. Part -IV deals with Comparative Analysis of Vedic Multipliers using different constructions followed by conclusion and references.

II. VEDIC ALGORITHM BASED MULTIPLICATION

A detailed description of Vedic multiplicity is presented in [1]. The basic formula is 2x2 Multiplier. For N x N multiplication, divide the multiplier and the multiplier into two parts, namely (N to N/2-1) and (N/2 to 1) fractions. For example, if A=0000001010101101, divide 00000010 by 10101101. Likewise, if B=0010001110101011.

Then it is divisible by 00100011 and 10101011. Showing the divisions of A and AM and AL. For input B, it is divided into two parts BM and BL. A and B can be represented in AMAL and BMBL. The multiplication function between A and B can be expressed as:

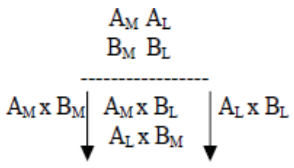


Figure 1: Cross Multiplication Representations [1]

These sub-sections can be manufactured and assembled as described in [1]. The block diagram for 16x16 Multiplication based on Vedic technology as proposed in [1] is shown in Figure 2. The first function is a set of four 8x8 Multiplier based on Vedic technology.

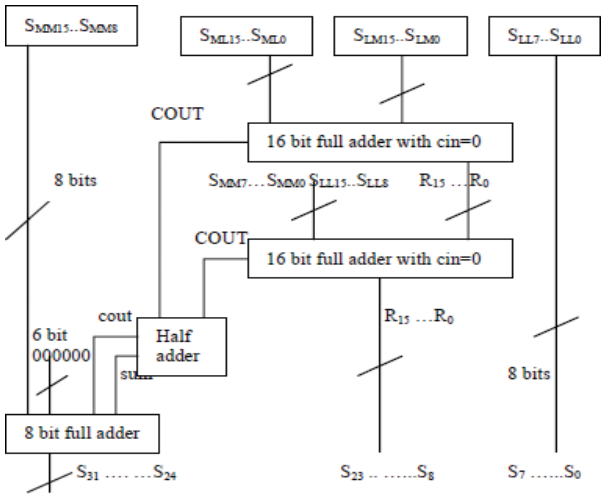


Figure 2: Block Diagram for 16-bit Vedic Multiplication [1]

As it is known that the connector will be used in the intermediate calculation, so the speed and efficiency of the design will improve the overall development process. In the next section, other adder topologies used to generate the Vedic multiplier for different lengths are discussed.

III. DIFFERENT TOPOLOGIES FOR ADDER

In the literature, various adders have been developed such as Ripple Carry Adder (RCA) [2, 3], CSA [2, 4-11], CBL [2, 7] and SQRT-CSA, Modification of SQRT-CSA [6] available. A brief discussion of the above components is provided below for clarity.

RCA is the common interface where the address chain is joined from one level to another. In CSA, each stage has two ripple carriers and a set of amplifiers. Based on the initial load input, the sum of current and load is calculated for the next step. As the length of the input data increases, so does the number of CSA levels. In the CSA line, the same number of inputs are used in all phases. Later SQRT-CSA was introduced where the bit size for different steps is always added. The SQRT-CSA distribution was found to be better than the linear CSA.

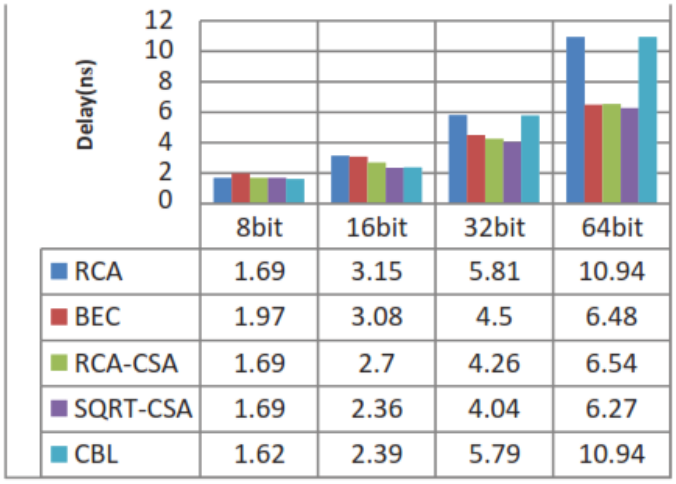
Later SQRT-CSA was modified to convert CSA with Cin = 1 and BEC (Binary to Excess-1 Converter) [5, 6].

Let's take a look at the std_cell where you can stop the synthesis in the cell. The Vedic multiplier is used in adder-like topologies.

IV. COMPARATIVE ANALYSIS OF VEDIC MULTIPLIERS USING DIFFERENT ADDER ARCHITECTURE

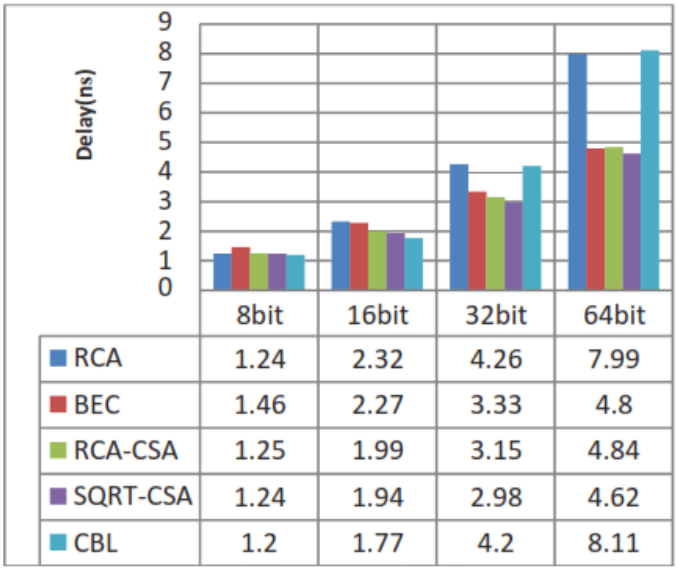
In this section, we present a comparison of the delay, power and area of the Vedic number using different numbers in the 32/28nm digital Standard Cell Library by Brief Design Compiler. Important digital design principles, such as area, strength, and flexibility are calculated by Design Design. For this, we need the HDL code of the design and the network file associated with the desired technical node. Libraries of various Standards are provided by Brief for educational purposes. The files are in three formats .db ,.lib and .v. In the design of the integrated format .db is required. The .lib format is a readable version of the .db format.

We calculated the area, power or delay for vedic multiplication using different numbers with input bit length. We generated HDL code for each module for the length of the input bit. Figures 3, 4 and 5 show the delay for the 32/28nm technology for HVT (High Voltage), RVT (Regular Voltage), and LVT (Low Voltage) for 8 different factories -bit, 16- bit, 32-bit and 64-bit components. RVT is the same as the standard power rating (units in Word-seconds).



	8bit	16bit	32bit	64bit
RCA	1.69	3.15	5.81	10.94
BEC	1.97	3.08	4.5	6.48
RCA-CSA	1.69	2.7	4.26	6.54
SQRT-CSA	1.69	2.36	4.04	6.27
CBL	1.62	2.39	5.79	10.94

Figure 3: Delay of Vedic Multiplier using different Adders for HVT



	8bit	16bit	32bit	64bit
RCA	1.24	2.32	4.26	7.99
BEC	1.46	2.27	3.33	4.8
RCA-CSA	1.25	1.99	3.15	4.84
SQRT-CSA	1.24	1.94	2.98	4.62
CBL	1.2	1.77	4.2	8.11

Figure 4: Delay of Vedic Multiplier using different Adders for RVT

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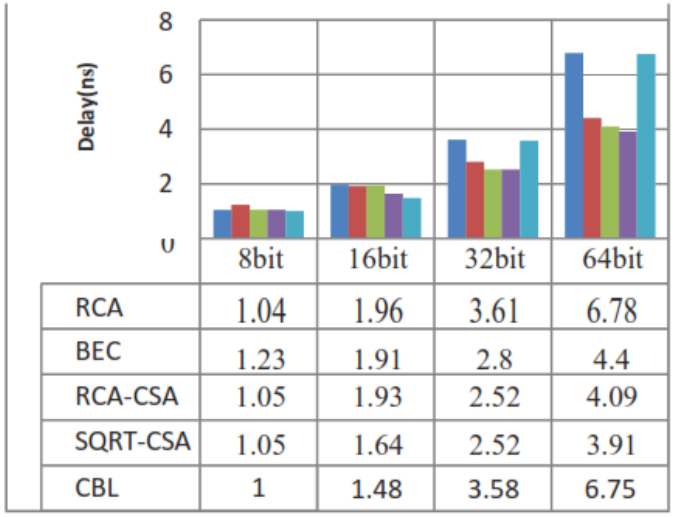
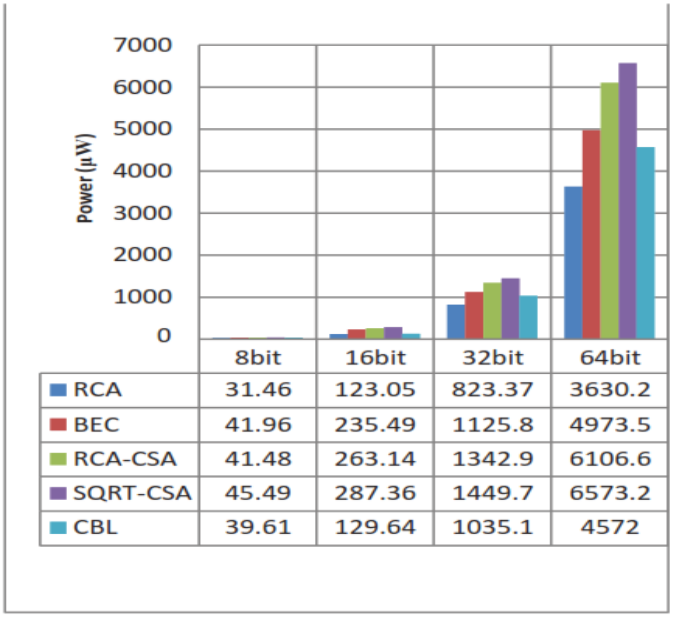


	8bit	16bit	32bit	64bit
RCA	1.04	1.96	3.61	6.78
BEC	1.23	1.91	2.8	4.4
RCA-CSA	1.05	1.93	2.52	4.09
SQRT-CSA	1.05	1.64	2.52	3.91
CBL	1	1.48	3.58	6.75

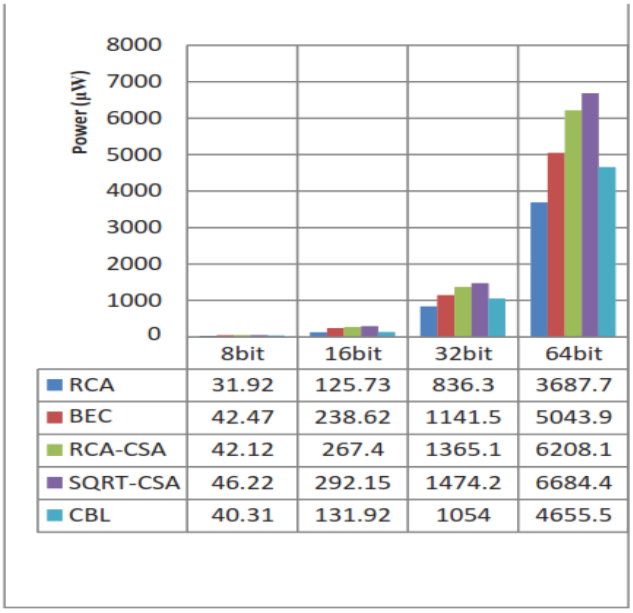
Figure 5: Delay of Vedic Multiplier using different Adders for LVT

From the point of view of delay, it can be stated that as the length of the input increases, the Vedic multiplier based on SQRT-CSA performs better in all cases. Figures 6, 7 and 8 show the power dissipation of the 32/28 nm technology for HVT, RVT and LVT (units in microwatts).



	8bit	16bit	32bit	64bit
RCA	31.46	123.05	823.37	3630.2
BEC	41.96	235.49	1125.8	4973.5
RCA-CSA	41.48	263.14	1342.9	6106.6
SQRT-CSA	45.49	287.36	1449.7	6573.2
CBL	39.61	129.64	1035.1	4572

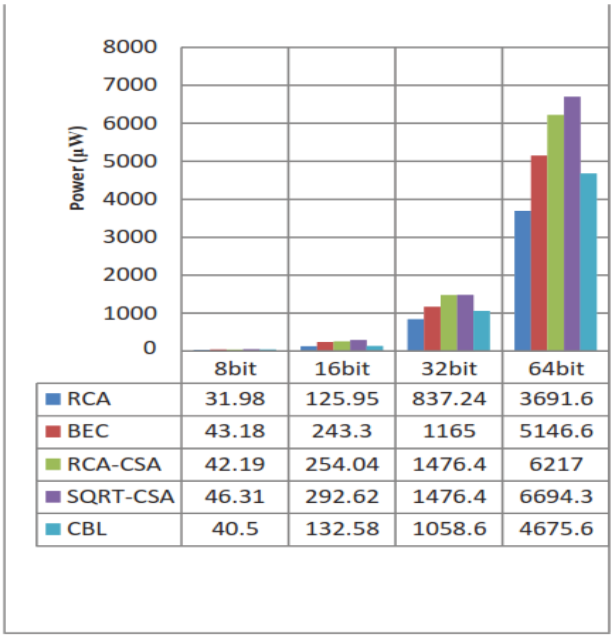
Figure 6: Dynamic Power Dissipation of Vedic Multiplier for HVT



	8bit	16bit	32bit	64bit
RCA	31.92	125.73	836.3	3687.7
BEC	42.47	238.62	1141.5	5043.9
RCA-CSA	42.12	267.4	1365.1	6208.1
SQRT-CSA	46.22	292.15	1474.2	6684.4
CBL	40.31	131.92	1054	4655.5

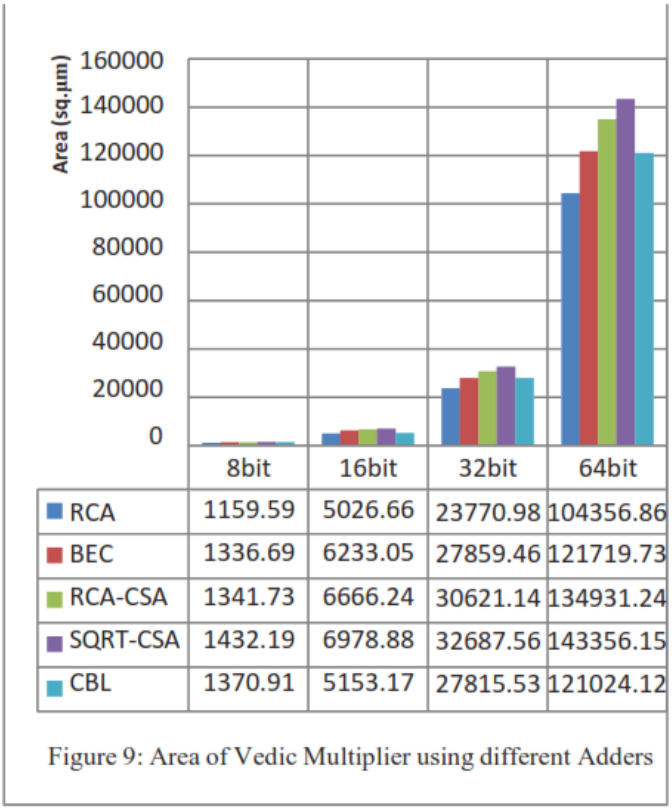
Figure 7: Dynamic Power Dissipation of Vedic Multiplier for RVT

From Figures 6,7, and 8, it can be concluded that as the input length increases, the RCA is followed by the CBL based Vedic multiplier.



	8bit	16bit	32bit	64bit
RCA	31.98	125.95	837.24	3691.6
BEC	43.18	243.3	1165	5146.6
RCA-CSA	42.19	254.04	1476.4	6217
SQRT-CSA	46.31	292.62	1476.4	6694.3
CBL	40.5	132.58	1058.6	4675.6

Figure 8: Dynamic Power Dissipation of Vedic Multiplier for LVT



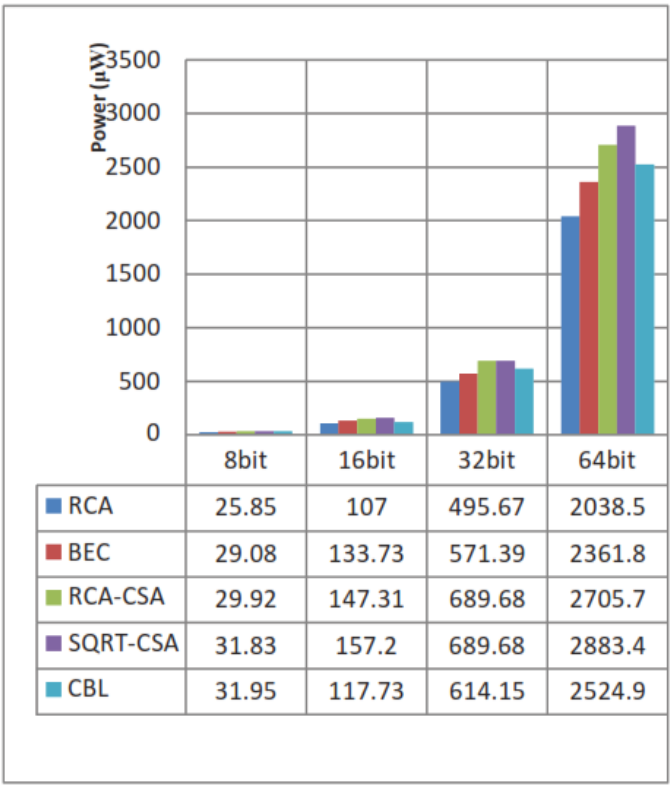
	8bit	16bit	32bit	64bit
RCA	1159.59	5026.66	23770.98	104356.86
BEC	1336.69	6233.05	27859.46	121719.73
RCA-CSA	1341.73	6666.24	30621.14	134931.24
SQRT-CSA	1432.19	6978.88	32687.56	143356.15
CBL	1370.91	5153.17	27815.53	121024.12

Figure 9: Area of Vedic Multiplier using different Adders

Figure 9 shows the amount of silk required to implement the design (units in square Micrometers).

From Number 9, it can be said as follows the longer the input, the more efficient the modified SQRT-based BEC is compared to other architectures of the integrator.

Power leakage analysis is shown in Fig.10 for different architectures of 8-bit, 16-bit, 32-bit and 64-bit adder (units in Microwatt). BEC performance is better than others such as CSA, CBL,SQRT-CSA.



	8bit	16bit	32bit	64bit
RCA	25.85	107	495.67	2038.5
BEC	29.08	133.73	571.39	2361.8
RCA-CSA	29.92	147.31	689.68	2705.7
SQRT-CSA	31.83	157.2	689.68	2883.4
CBL	31.95	117.73	614.15	2524.9

Figure 10: Leakage Power of Vedic Multiplier using different Adders

V. CONCLUSION

A comparative analysis of Vedic synthesis using different definitions is presented in this paper. The measurement parameters are delay, area and strength (tightness and leakage) using a standard digital database.

Regarding delay: 8-bit Vedic multiplier with CBL adder is about 5% faster than SQRT-CSA, RCA-CSA, RCA and 20% faster than BEC.

16-bit Vedic multiplier using CBL adder is about 10% faster than SQRT-CSA and RCA-CSA and 30% faster than BEC and RCA.

32-bit Vedic multiplier using SQRT-CSA integrator is about 5% faster than RCA-CSA and 10% faster than BEC, and 40% faster than CBL and RCA.

64-bit Vedic multiplier using SQRT-CSA adder is about 5% faster than RCA-CSA and BEC, 75% faster than CBL and RCA.

About power consumption: RCA uses about 20% less power than CBL, 35% less than BEC, 65% less than RCA-CSA and 80% less smaller than SQRT-CSA.

For Area: RCA should be about 10% less than CBL, 20% less than BEC, 30% less than RCA-CSA and 40% less than SQRT-CSA.

Leakage Capacity: 15% more than RCA or BEC, 25% more than CBL, 30% less than RCA-CSA and 460% more than SQRT-CSA.

So depending on the requirements we can choose to add accordingly. A different search can be done on different addresses for the same call on different technology nodes.

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